

SAMSUNG SEMICONDUCTOR INC.

1993

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DATA BOOK

SAMSUNG

LINEAR ICS • GRAPHICS • POWER MOSFETS
B I P O L A R T R A N S I S T O R S

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SAMSUNG SEMICONDUCTOR: AN OVERVIEW

Samsung Semiconductor is a unit of the Samsung Group, a worldwide, Korean-based *chaebol* conglomerate of 34 companies that enjoyed sales of \$48 billion in 1992. Sales of Samsung Electronics Co., Ltd., of which Samsung Semiconductor is a division, were more than \$7 billion in 1992. For 1992, its earnings made Samsung the world's 11st largest maker of semiconductors.

Semiconductor Capabilities

Since entering the semiconductor market in 1974, Samsung has grown to produce more than 3,000 product types, and compete with the world's most advanced companies. Keys to the firm's competitive position include outstanding proprietary product design, state-of-the-art CMOS and Bi-CMOS process technologies, and stable product supply.

Samsung now spends some 8% of total revenues on research and development—a greater percentage than is spent by many of the world's leading electronics firms—to assure continued leadership and competitiveness.

Much of Samsung's attention has historically gone to commodity and emerging-generation memory products. The firm is ranked by market research firms as the world's first-largest supplier of the 4-megabit DRAM. Large-scale production of 4-megabit SRAMs and 16-megabit DRAMs has been under way for some time, and the company holds a leadership position in 16-megabit DRAMs. In addition to these efforts, however, Samsung is also a supplier of leading-edge technology products.

These include ASICs, with standard-cell, gate array, and full-custom offerings now in development in 1.0 micron, 0.8 micron, and 0.6 micron process: Industry-leading FIFOs—both standard and program-mable-flag; DRAM controllers, including a proprietary chip developed with the cooperation of Motorola to support the 68040 microprocessor; Bi-CMOS ultrafast SRAMs; a emerging family of graphics products, including RAM DACs and video RAMs.

Fabrication Facilities

Fabrication of many of these products is done at our facilities in San Jose, California. Worldwide, Samsung Semiconductor runs a total of some nine advanced R&D and manufacturing facilities. The Class1, 8" wafer-fabrication line at Kiheung, Korea, dedicated to DRAM

technology, has been in operation for several years and remains among the largest and most advanced facilities ever built.

Throughout the industry and across all of its product lines, Samsung has become known for a rigorous commitment to quality and reliability.

Microproducts

Microproducts covered in this data book include Bipolar Transistors, an area in which Samsung's broad line makes it the world's Number Two producer, Power MOSFETs noteworthy for their ruggedness characteristics and breadth of line, with parts available of all types, for all applications; Linear ICs—one of the broadest lines on the market; a number of Graphics Products, including many that support high performance; and a full range of Computer Products—many of them leaderships parts, all of them noteworthy for quality and reliability.

Additional or updated information on microproducts or any other Samsung product is available from:

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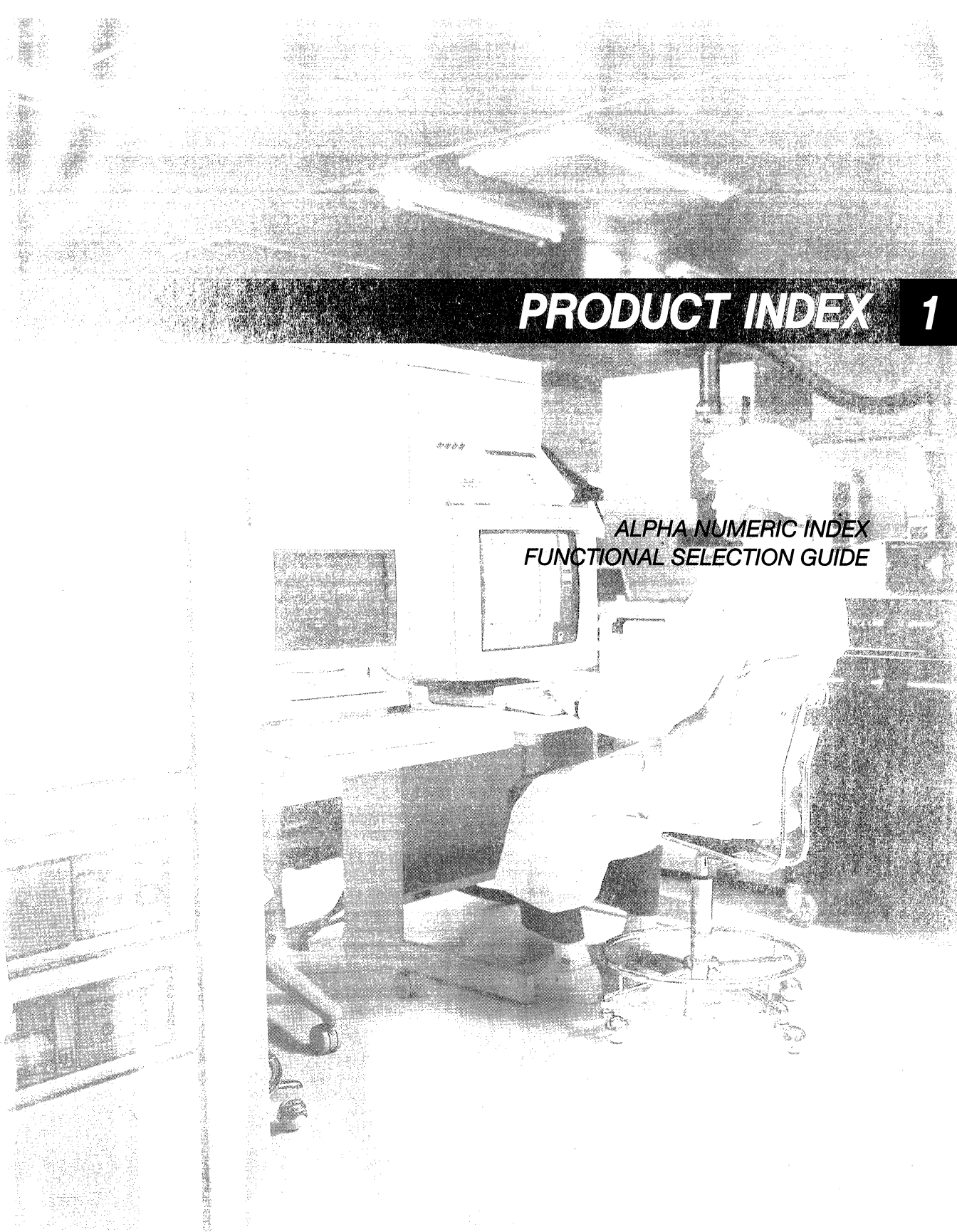
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TR : Transistor, LI : Linear, FET : MOSFET, MPR : Microprocessor Peripherals, T&R : Tape & Reel

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TR : Transistor, LI : Linear, FET : MOSFET, MPR : Microprocessor Peripherals, T&R : Tape & Reel

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TR : Transistor, LI : Linear, FET : MOSFET, MPR : Microprocessor Peripherals, T&R : Tape & Reel

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IRFSZ34	FET, 60V, 0.05R, 18.7A, 35W, N-CH, TO-220F	390
IRFSZ35	USE IRFSZ34	390
IRFSZ30	USE IRFSZ34	390
IRFSZ32	USE IRFSZ34	390
IRFSZ44	FET, 60V, 0.028R, 34A, 65W, N-CH, TO-220F	395
IRFSZ45	USE IRFSZ44	395
IRFSZ40	USE IRFSZ44	395
IRFSZ42	USE IRFSZ44	395
IRFU010	FET, 50V, 0.20R, 8.2A, 25W, N-CH, I-PACK	280
IRFU012	USE IRFU010	280

TR : Transistor, LI : Linear, FET : MOSFET, MPR : Microprocessor Peripherals, T&R : Tape & Reel

* See Supplement 1

PRODUCT INDEX

Standard MOSFET (Continued)

PART NO.	DESCRIPTION	PAGE
IRFU014	USE IRFU010	280
IRFU015	USE IRFU010	280
IRFU020	FET, 50V, 0.10R, 15A, 42W, N-CH, I-PACK	285
IRFU022	USE IRFU010	285
IRFU024	USE IRFU010	285
IRFU025	USE IRFU010	285
IRFU120	FET, 100V, 0.27R, 8.4A, 42W, N-CH, I-PACK	295
IRFU121	USE IRFU120	295
IRFU210	FET, 200V, 1.5R, 2.7A, 25W, N-CH, I-PACK	300
IRFU212	USE IRFU210	300
IRFU220	FET, 200V, 0.80R, 4.6A, 42W, N-CH, I-PACK	305
IRFU222	USE IRFU220	305
IRFU310	FET, 400V, 3.6R, 1.5A, 25W, N-CH, I-PACK	310
IRFU312	USE IRFU310	310
IRFU320	FET, 400V, 1.8R, 2.7A, 40W, N-CH, I-PACK	315
IRFU322	USE IRFU320	315
IRFU9010	FET, 50V, 0.5R, 5.3A, 25W, P-CH, I-PACK	325
IRFU9012	USE IRFU9010	325
IRFU9014	USE IRFU9010	325
IRFU9015	USE IRFU9010	325
IRFU9020	FET, 50V, 0.28R, 9.9A, 42W, P-CH, I-PACK	330
IRFU9022	USE IRFU9020	330
IRFU9024	USE IRFU9020	330
IRFU9025	USE IRFU9020	330
IRFU9120	FET, 100V, 0.60R, 5.9A, 42W, P-CH, I-PACK	335
IRFU9121	USE IRFU9020	335
IRFU9210	FET, 200V, 3.00R, 2.0A, 25W, P-CH, I-PACK	340
IRFU9212	USE IRFU9210	340
IRFZ14	FET, 60V, 0.20R, 10A, 36W, N-CH, TO-220	400
IRFZ15	USE IRFZ14	400
IRFZ24	FET, 60V, 0.1R, 15A, 40W, N-CH, TO-220	405
IRFZ25	USE IRFZ24	405
IRFZ34	FET, 60V, 0.05R, 30A, 90W, N-CH, TO-220	410
IRFZ35	USE IRFZ34	410
IRFZ44	FET, 60V, 0.028R, 35A, 150W, N-CH, TO-220	415
IRFZ45	USE IRFZ44	415
SSH10N70	FET, 700V, 1.2R, 10A, 150W, N-CH, TO-3P	420
SSH10N70A	USE SSH10N70	420
SSH20N50	FET, 500V, 0.35R, 20A, 150W, N-CH, TO-3P	425
SSH20N50A	USE SSH20N50	425
SSH20N45	USE SSH20N50	425
SSH20N45A	USE SSH20N50	425
SSH60N10	FET, 100V, 0.03R, 60A, 150W, N-CH, TO-3P	430
SSH60N10A	USE SSH60N10	430
SSH60N06	USE SSH60N10	430
SSH60N06A	USE SSH60N10	430
SSP1N60	FET, 600V, 12R, 1A, 40W, N-CH, TO-220	435
SSP4N60	FET, 600V, 3.0R, 4A, 75W N-CH, TO-220	438

TR : Transistor, LI : Linear, FET : MOSFET, MPR : Microprocessor Peripherals, T&R : Tape & Reel

* See Supplement 1

PRODUCT INDEX

Standard MOSFET (Continued)

PART NO.	DESCRIPTION	PAGE
SSP4N55	USE SSP4N60	438
SSP4N70	FET, 700V, 3.5R, 4A, 125W N-CH, TO-220	443
SSP4N70A	USE SSP4N70	443
SSP6N60	FET, 600V, 1.8R, 6A, 125W N-CH, TO-220	448
SSP6N55	USE SSP6N60	448
SSR1N60	FET, 600V, 12R, 1A, 40W N-CH, D-PACK T&R	453
SSR1N55	USE SSR1N60	453
SSR2955	FET, 60V, 0.3R, 12A, 42W P-CH, D-PACK T&R	456
SSR3055	FET, 60V, 0.15R, 12A, 42W N-CH, D-PACK T&R	461
SSU1N60	FET, 600V, 12R, 1A, 40W N-CH, I-PACK	453
SSU1N55	USE SSU1N60	453
SSU2955	FET, 60V, 0.3R, 12A, 42W P-CH, I-PACK	456
SSU3055	FET, 60V, 1.15R, 12A, 42W N-CH, I-PACK	461

TR : Transistor, LI : Linear, FET : MOSFET, MPR : Microprocessor Peripherals, T&R : Tape & Reel

* See Supplement 1

Logic Level FET

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IRL510	FET, 100V, 0.75R, 4A, 43W, N-CH, TO-220, LOGIC LEVEL	466
IRL511	USE IRL510	466
IRL520	FET, 100V, 0.4R, 7.9A, 42W, N-CH, TO-220, LOGIC LEVEL	471
IRL521	USE IRL520	471
IRL530	FET, 100V, 0.2R, 13A, 75W, N-CH, TO-220, LOGIC LEVEL	476
IRL531	USE IRL530	476
IRL540	FET, 100V, 0.11R, 24A, 125W, N-CH, TO-220, LOGIC LEVEL	481
IRL541	USE IRL540	481
IRL610	FET, 200V, 2.4R, 2A, 43W, N-CH, TO-220, LOGIC LEVEL	486
IRL611	USE IRL610	486
IRL620	FET, 200V, 1.2R, 4A, 42W, N-CH, TO-220, LOGIC LEVEL	491
IRL621	USE IRL620	491
IRL630	FET, 200V, 0.6R, 8A, 75W, N-CH, TO-220, LOGIC LEVEL	501
IRL631	USE IRL630	501
IRL640	FET, 200V, 0.22R, 16A, 125W, N-CH, TO-220, LOGIC LEVEL	506
IRL641	USE IRL640	506
IRLR014-TF	FET, 60V, 0.3R, 6.7A, 25W, N-CH, D-PACK, LOGIC LEVEL, T&R	511
IRLR010	USE IRLR014	511
IRLR024-TF	FET, 60V, 0.3R, 0.15A, 25W, N-CH, D-PACK, LOGIC LEVEL, T&R	516
IRLR020	USE IRLR024	516

TR : Transistor, LI : Linear, FET : MOSFET, MPR : Microprocessor Peripherals, T&R : Tape & Reel

* See Supplement 1

PRODUCT INDEX

Logic Level FET (Continued)

PART NO.	DESCRIPTION	PAGE
IRLR110-TF	FET, 100V, 0.75R, 4A, 30W, N-CH, D-PACK, LOGIC LEVEL, T&R	521
IRLR111	USE IRLR110	521
IRLR120-TF	FET, 100V, 0.4R, 7.9A, 42W, N-CH, D-PACK, LOGIC LEVEL, T&R	526
IRLR121	USE IRLR120	526
IRLR210-TF	FET, 200V, 2.4R, 2A, 25W, N-CH, D-PACK, LOGIC LEVEL, T&R	531
IRLR211	USE IRLR210	531
IRLR220-TF	FET, 200V, 1.2R, 4A, 42W, N-CH, D-PACK, LOGIC LEVEL, T&R	536
IRLR221	USE IRLR220	536
IRLU014	FET, 60V, 0.3R, 6.7A, 25W, N-CH, I-PACK, LOGIC LEVEL	511
IRLU010	USE IRLU014	511
IRLU024	FET, 60V, 0.15R, 14A, 42W, N-CH, I-PACK, LOGIC LEVEL	516
IRLU020	USE IRLU024	516
IRLU110	FET, 100V, 0.75R, 4A, 30W, N-CH, I-PACK, LOGIC LEVEL	521
IRLU111	USE IRLU110	521
IRLU120	FET, 100V, 0.4R, 7.9A, 42W, N-CH, I-PACK, LOGIC LEVEL	526
IRLU121	USE IRLU120	526
IRLU210	FET, 100V, 2.4R, 2A, 25W, N-CH, I-PACK, LOGIC LEVEL	531
IRLU211	USE IRLU210	531
IRLU220	FET, 200V, 1.2R, 4A, 42W, N-CH, I-PACK, LOGIC LEVEL	536
IRLU221	USE IRLU220	536
IRLZ14	FET, 60V, 0.30R, 8.0A, 60W, N-CH, TO-220, LOGIC LEVEL	541
IRLZ10	USE IRLZ14	541
IRLZ24	FET, 60V, 0.15R, 14A, 50W, N-CH, TO-220, LOGIC LEVEL	545
IRLZ20	USE IRLZ24	545
IRLZ34	FET, 60V, 0.07R, 25A, 90W, N-CH, TO-220, LOGIC LEVEL	549
IRLZ30	USE IRLZ34	549
IRLZ44	FET, 60V, 0.04R, 35A, 150W, N-CH, TO-220, LOGIC LEVEL	553
IRLZ40	USE IRLZ44	553
SSP3055L	FET, 60V, 0.18R, 12A, 40W, N-CH, TO-220, LOGIC LEVEL	557
SSR3055L	FET, 60V, 0.18R, 12A, 40W, N-CH, D-PACK, LOGIC LEVEL	561
SSU3055L	FET, 60V, 0.18R, 12A, 40W, N-CH, I-PACK, LOGIC LEVEL	561

TR : Transistor, LI : Linear, FET : MOSFET, MPR : Microprocessor Peripherals, T&R : Tape & Reel

* See Supplement 1

LINEAR IC

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KA2808	IC, EARTH LEAK DETECTOR, 8PDIP	565
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KA324	IC, QUAD OP AMP, 14PDIP	577
KA339D	IC, QUAD DIFFERENTIAL COMPARATOR, 14PSOP, T&R	584
KA339	IC, QUAD DIFFERENTIAL COMPARATOR, 14PDIP	584
KA34063A	IC, DE-TO-DC CONVERTER/CONTROLLER, 8PDIP	589

PRODUCT INDEX

LINEAR IC (Continued)

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KA3842/3/4/5B	IC, CURRENT MODE PWM, 8PDIP	603
KA393D	TC, DUAL DIFFERENTIAL COMPARATOR, 8PSOP, T&R	610
KA393	TC, DUAL DIFFERENTIAL COMPARATOR, 8PDIP	610
KA431/AD	IC, VOLTAGE REFERENCE ADJUST, 8PSOP, T&R	615
KA431/A	IC, VOLTAGE REFERENCE ADJUST, TO-92	615
KA555/ID	IC, SINGLE BIPOLAR TIMER, 8PSOP, T&R	621
KA555/I	IS, SINGLE BIPOLAR TIMER, 8PDIP	621
KA556/I	IC, DUAL BIPOLAR TIMER 14PDIP	625
KA558/I	IC, QUAD BIPOLAR TIMER, 16DIP	628
KA76L05	IC, 3T, ROW DROP-REG, TO-92	630
KA7805/A/I	IC, 3T, POS V-REG, 1.5A, 5V, 4%, TO-220	632
KA7808/A/I	IC, 3T, POS V-REG, 1.5A, 8V, 4%, TO-220	632
KA7812/A/I	IC, 3T, POS V-REG, 1.5A, 12V, 4%, TO-220	632
KA7815/A/I	IC, 3T, POS V-REG, 1.5A, 15V, 4%, TO-220	632
KA7824/A/I	IC, 3T, POS V-REG, 1.5A, 24V, 4%, TO-220	632
KA78L05A	IC, VOLT-REG, 100mA, +5V, 5%, TO-92	658
KA78L08A	IC, VOLT-REG, 100mA, +5V, 5%, TO-92	658
KA78L12A	IC, VOLT-REG, 100mA, +5V, 5%, TO-92	658
KA78L15A	IC, VOLT-REG, 100mA, +5V, 5%, TO-92	658
KA7905	IC, 3T, NEG, V-REG, 1/5A, 5V, 4%, TO-220	665
KA7908	IC, 3T, NEG, V-REG, 1/5A, 5V, 4%, TO-220	665
KA7912	IC, 3T, NEG, V-REG, 1/5A, 5V, 4%, TO-220	665
KA7915	IC, 3T, NEG, V-REG, 1/5A, 5V, 4%, TO-220	665
KA79LXXA	IC, VOLT-REG, 100mA, +5V, 5%, TO-92	674

TR : Transistor, LI : Linear, FET : MOSFET, MPR : Microprocessor Peripherals, T&R : Tape & Reel

* See Supplement 1

PRODUCT INDEX

Data Converter

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KDA0476PL-50	RAM DAC, 50MHZ, 32-PIN PLCC	697
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KDA0476PL-50	RAM DAC, 50MHZ, 44-PIN PLCC	697
KDA0476PL-66	RAM DAC, 66MHZ, 44-PIN PLCC	697
KDA0476PL-80	RAM DAC, 80MHZ, 44-PIN PLCC	697
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KDA0478PL-100	RAM DAC, 100MHZ, 44-PIN PLCC	697
KDA0478PL-120	RAM DAC, 120MHZ, 44-PIN PLCC	697
KSV3110N-8	IC, 20MHZ 8-BIT VIDEO A/D AND D/A, 40PDIP	715

TR : Transistor, LI : Linear, FET : MOSFET, MPR : Microprocessor Peripherals, T&R : Tape & Reel

* See Supplement 1

Telecom

PART NO.	DESCRIPTION	PAGE
KS58006	IC, TONE/PLUSE DIALER, 18DIP	726

TR : Transistor, LI : Linear, FET : MOSFET, MPR : Microprocessor Peripherals, T&R : Tape & Reel

* See Supplement 1

Audio

PART NO.	DESCRIPTION	PAGE
KA386D	IC, AUDIO AMP, 300MW, 8PSOP, T&R	734
KA386	IC, AUDIO AMP, 6600MW, 8PDIP	734

TR : Transistor, LI : Linear, FET : MOSFET, MPR : Microprocessor Peripherals, T&R : Tape & Reel

* See Supplement 1

NOTES



DATA SHEETS

2

TRANSISTORS
MOSFETs
LINEAR ICs
GRAPHICS

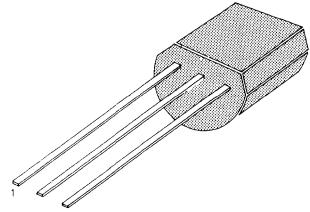
GENERAL PURPOSE TRANSISTOR

- Collector-Emitter Voltage: $V_{CEO}=40V$
- Collector Dissipation: $P_C(\text{max})=625mW$

ABSOLUTE MAXIMUM RATINGS ($T_a=25^\circ C$)

Characteristic	Symbol	Rating	Unit
Collector-Base Voltage	V_{CBO}	60	V
Collector-Emitter Voltage	V_{CEO}	40	V
Emitter-Base Voltage	V_{EBO}	6	V
Collector Current	I_C	200	mA
Collector Dissipation	P_C	625	mW
Junction Temperature	T_J	150	$^\circ C$
Storage Temperature	T_{stg}	-55 ~ 150	$^\circ C$

TO-92



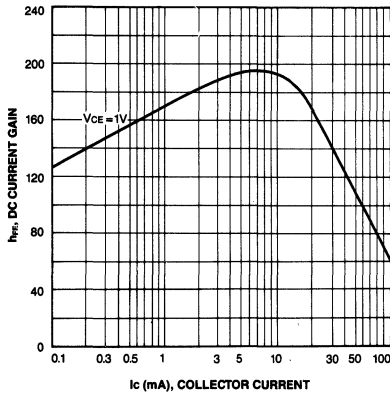
1. Emitter 2. Base 3. Collector

ELECTRICAL CHARACTERISTICS ($T_a=25^\circ C$)

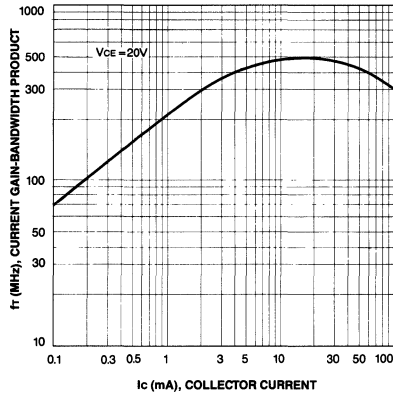
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Collector-Base Breakdown Voltage	BV_{CBO}	$I_C=10\mu A, I_E=0$	60			V
*Collector-Emitter Breakdown Voltage	BV_{CEO}	$I_C=1mA, I_B=0$	40			V
Emitter-Base Breakdown Voltage	BV_{EBO}	$I_E=10\mu A, I_C=0$	6			V
Collector Cut-off Current	I_{CEX}	$V_{CE}=30V, V_{EB}=3V$			50	nA
Base Cut-off Current	I_{BL}	$V_{CE}=30V, V_{EB}=3V$			50	nA
*DC Current Gain	h_{FE}					
	:2N3903	$V_{CE}=1V, I_C=0.1mA$	20			
	2N3904		40			
	2N3903	$V_{CE}=1V, I_C=1mA$	35			
	2N3904		70			
	2N3903	$V_{CE}=1V, I_C=10mA$	50		150	
	2N3904		100		300	
	2N3903	$V_{CE}=1V, I_C=50mA$	30			
	2N3904		60			
	2N3903	$V_{CE}=1V, I_C=100mA$	15			
	2N3904		30			
*Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C=10mA, I_B=1mA$			0.2	V
		$I_C=50mA, I_B=5mA$			0.3	V
*Base-Emitter Saturation Voltage	$V_{BE(sat)}$	$I_C=10mA, I_B=1mA$	0.65		0.85	V
		$I_C=50mA, I_B=5mA$			0.95	V
Output Capacitance	C_{OB}	$V_{CB}=5V, I_E=0$			4	pF
Current Gain Bandwidth Product	f_T	$f=1MHz$ $V_{CE}=20V, I_C=10mA$ $f=100MHz$	250			MHz
	:2N3903		300			MHz
	2N3904					ns
Turn On Time	t_{ON}	$V_{CC}=3V, V_{BE}=0.5V$ $I_C=10mA, I_{B1}=1mA$			70	ns
Turn Off Time	t_{OFF}	$V_{CC}=3V, I_C=10mA$ $I_{B1}=I_{B2}=1mA$			225	ns
	:2N3903				250	ns
	2N3904					ns

*Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

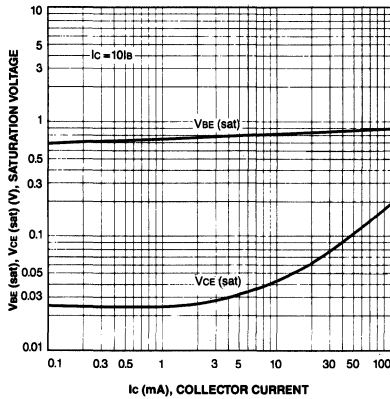
DC CURRENT GAIN



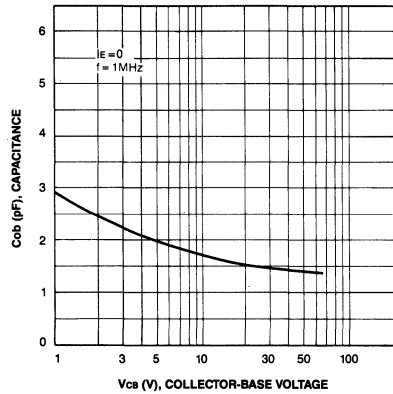
CURRENT GAIN-BANDWIDTH PRODUCT



BASE-EMITTER SATURATION VOLTAGE
COLLECTOR-EMITTER SATURATION VOLTAGE



OUTPUT CAPACITANCE



GENERAL PURPOSE TRANSISTOR

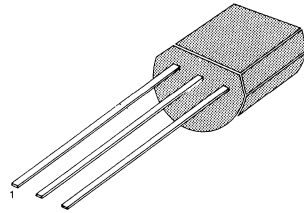
- Collector-Emitter Voltage: $V_{CEO}=40V$
- Collector Dissipation: $P_C (max)=625mW$

ABSOLUTE MAXIMUM RATINGS ($T_a=25^\circ C$)

Characteristic	Symbol	Rating	Unit
Collector-Base Voltage	V_{CBO}	-40	V
Collector-Emitter Voltage	V_{CEO}	-40	V
Emitter-Base Voltage	V_{EBO}	-5	V
Collector Current	I_C	-200	mA
Collector Dissipation	P_C	-625	mW
Junction Temperature	T_J	150	$^\circ C$
Storage Temperature	T_{stg}	-55 ~ 150	$^\circ C$

- Refer to 2N3906 for graphs

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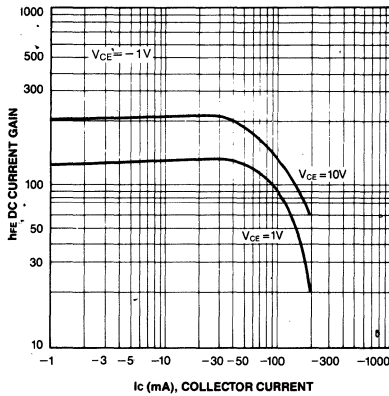
1. Emitter 2. Base 3. Collector

ELECTRICAL CHARACTERISTICS ($T_a=25^\circ C$)

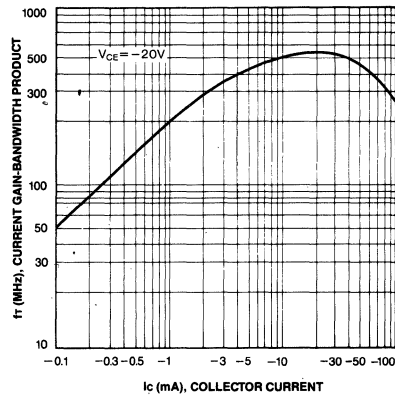
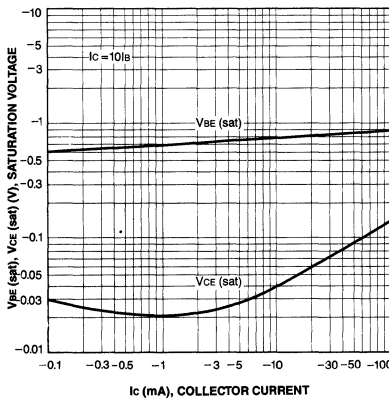
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Collector-Base Breakdown Voltage	BV_{CBO}	$I_C=-10\mu A, I_E=0$	-40			V
* Collector-Emitter Breakdown Voltage	BV_{CEO}	$I_C=-1mA, I_B=0$	-40			V
Emitter-Base Breakdown Voltage	BV_{EBO}	$I_E=-10\mu A, I_C=0$	-6			V
Collector Cut-off Current	I_{CEX}	$V_{CE}=-30V, V_{EB}=-3V$			-50	nA
Base Cut-off Current	I_{BL}	$V_{CE}=-30V, V_{EB}=-3V$			-50	nA
* DC Current Gain	h_{FE}					
	:2N3905	$V_{CE}=-1V, I_C=-0.1mA$	30			
	2N3906		60			
	:2N3905	$V_{CE}=-1V, I_C=-1mA$	40			
	2N3906		80			
	:2N3905	$V_{CE}=-1V, I_C=-10mA$	50		150	
	2N3906		100		300	
	:2N3905	$V_{CE}=-1V, I_C=-50mA$	30			
	2N3906		60			
	:2N3905	$V_{CE}=-1V, I_C=100mA$	15			
	2N3906		30			
* Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C=-10mA, I_B=-1mA$			-0.25	V
		$I_C=-50mA, I_B=-5mA$			-0.4	V
* Base-Emitter Saturation Voltage	$V_{BE(sat)}$	$I_C=-10mA, I_B=-1mA$	-0.65		-0.85	V
		$I_C=-50mA, I_B=-5mA$			-0.95	V
Output Capacitance	C_{OB}	$V_{CB}=-5V, I_E=0$			4.5	pF
		$f=100KHz$				
Current Gain Bandwidth Product	f_T	$V_{CE}=-20V, I_C=-10mA$				
	:2N3905	$f=100MHz$	200			MHz
	2N3906		250			MHz
Turn On Time	t_{ON}	$V_{CC}=-3V, V_{BE}=-0.5V$			70	ns
		$I_C=-10mA, I_{B1}=-1mA$				
Turn Off Time	t_{OFF}	$V_{CC}=-3V, I_C=-10mA$				
	:2N3905	$I_{B1}=I_{B2}=1-mA$			260	ns
	2N3906				300	ns

* Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

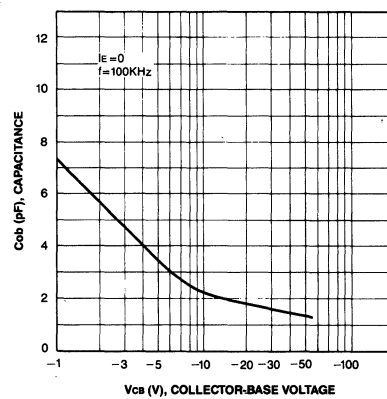
DC CURRENT GAIN



CURRENT GAIN-BANDWIDTH PRODUCT

BASE-EMITTER SATURATION VOLTAGE
COLLECTOR-EMITTER SATURATION VOLTAGE

OUTPUT CAPACITANCE



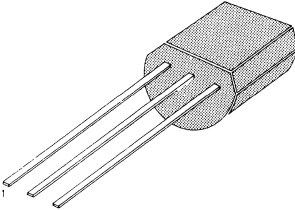
GENERAL PURPOSE TRANSISTOR

- Collector-Emitter Voltage: $V_{CEO} = 40V$
- Collector Dissipation: $P_C (max) = 625mW$

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^{\circ}C$)

Characteristic	Symbol	Rating	Unit
Collector-Base Voltage	V_{CBO}	60	V
Collector-Emitter Voltage	V_{CEO}	40	V
Emitter-Base Voltage	V_{EBO}	6	V
Collector Current	I_C	600	mA
Collector Dissipation	P_C	625	mW
Junction Temperature	T_j	150	$^{\circ}C$
Storage Temperature	T_{stg}	-55 ~ 150	$^{\circ}C$

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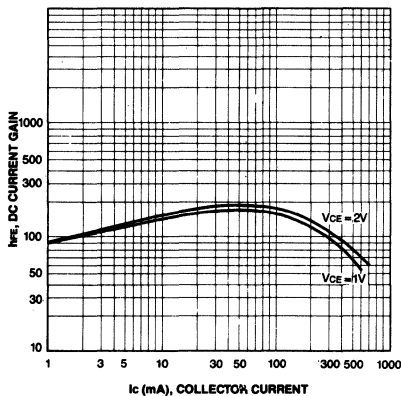
1. Emitter 2. Base 3. Collector

ELECTRICAL CHARACTERISTICS ($T_a = 25^{\circ}C$)

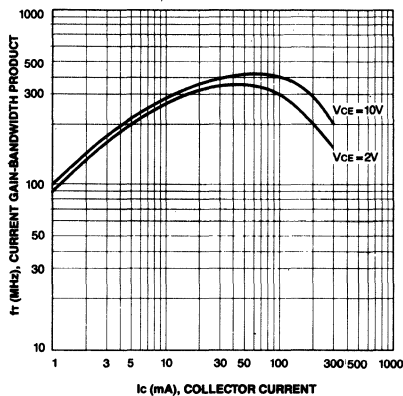
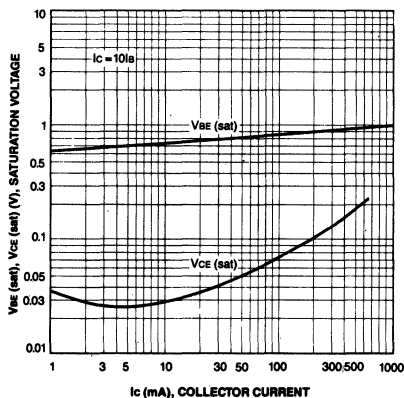
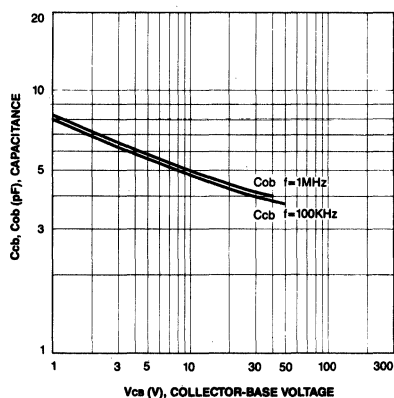
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Collector-Base Breakdown Voltage	BV_{CBO}	$I_C = 100\mu A, I_E = 0$	60			V
* Collector-Emitter Breakdown Voltage	BV_{CEO}	$I_C = 1mA, I_B = 0$	40			V
Emitter-Base Breakdown Voltage	BV_{EBO}	$I_E = 100\mu A, I_C = 0$	6			V
Collector Cut-off Current	I_{CEX}	$V_{CE} = 35V, V_{EB} = 0.4V$			100	nA
* DC Current Gain	h_{FE}					
:2N4401		$V_{CE} = 1V, I_C = 0.1mA$	20			
2N4400		$V_{CE} = 1V, I_C = 1mA$	20			
2N4401			40			
2N4400		$V_{CE} = 1V, I_C = 10mA$	40			
2N4401			80			
2N4400		$V_{CE} = 1V, I_C = 150mA$	50		150	
2N4401			100		300	
2N4400		$V_{CE} = 2V, I_C = 500mA$	20			
2N4401			40			
* Collector-Emitter Saturation Voltage	$V_{CE (sat)}$	$I_C = 150mA, I_B = 15mA$			0.4	V
		$I_C = 50mA, I_B = 50mA$			0.75	V
* Base-Emitter Saturation Voltage	$V_{BE (sat)}$	$I_C = 150mA, I_B = 15mA$	0.75		0.95	V
		$I_C = 500mA, I_B = 50mA$			1.2	V
Output Capacitance	C_{CB}	$V_{CB} = 5V, I_E = 0$			6.5	pF
		$f = 100MHz$				
Current Gain Bandwidth Product	f_T	$V_{CE} = 10V, I_C = 20mA$				
:2N4400		$f = 100MHz$	200			MHz
2N4401			250			MHz
Turn On Time	t_{ON}	$V_{CC} = 30V, V_{BE} = 2V$			35	ns
		$I_C = 150mA, I_B1 = 15mA$				
Turn Off Time	t_{OFF}	$V_{CC} = 30V, I_C = 150mA$			255	ns
		$I_B1 = I_B2 = 15mA$				

* Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

DC CURRENT GAIN



CURRENT GAIN-BANDWIDTH PRODUCT

COLLECTOR-EMITTER SATURATION VOLTAGE
BASE-EMITTER SATURATION VOLTAGECOLLECTOR-BASE CAPACITANCE
OUTPUT CAPACITANCE

GENERAL PURPOSE TRANSISTOR

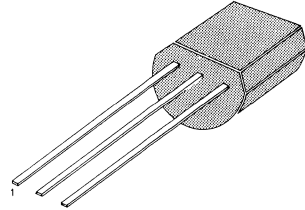
- Collector-Emitter Voltage: $V_{CE0} = 40V$
- Collector Dissipation: $P_C (\text{max}) = 625mW$

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ C$)

Characteristic	Symbol	Rating	Unit
Collector-Base Voltage	V_{CBO}	-40	V
Collector-Emitter Voltage	V_{CEO}	-40	V
Emitter-Base Voltage	V_{EBO}	-5	V
Collector Current	I_C	-600	mA
Collector Dissipation	P_C	625	mW
Junction Temperature	T_J	150	$^\circ C$
Storage Temperature	T_{stg}	-55 ~ 150	$^\circ C$

- Refer to 2N4403 for graphs

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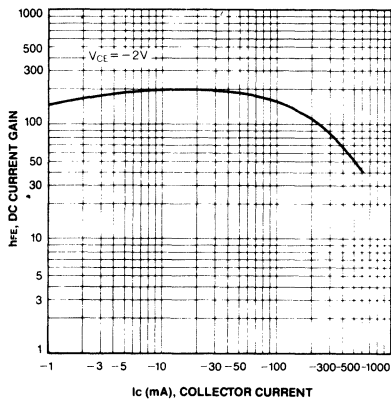
1. Emitter 2. Base 3. Collector

ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ C$)

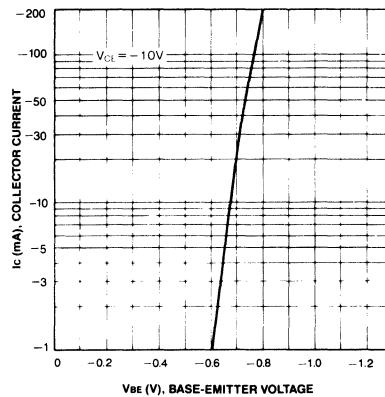
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Collector-Base Breakdown Voltage	BV_{CBO}	$I_C = -100\mu A, I_E = 0$	-40			V
*Collector-Emitter Breakdown Voltage	BV_{CEO}	$I_C = -1mA, I_B = 0$	-40			V
Emitter-Base Breakdown Voltage	BV_{EBO}	$I_E = -100\mu A, I_C = 0$	-5			V
Collector Cut-off Current	I_{CEX}	$V_{CE} = -35V, V_{EB} = -0.4V$			-100	nA
Base Cut-off Current	I_{BEV}	$V_{CE} = -35V, V_{EB} = -0.4V$			-100	nA
*DC Current Gain	h_{FE}					
2N4403		$V_{CE} = -1V, I_C = -0.1mA$	30			
2N4402		$V_{CE} = -1V, I_C = -1mA$	30			
2N4403			60			
2N4402		$V_{CE} = -1V, I_C = -10mA$	50			
2N4403			100			
2N4402		* $V_{CE} = -2V, I_C = -150mA$	50		150	
2N4403			100		300	
2N4402/2N4403		* $V_{CE} = -2V, I_C = -500mA$	20			
*Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = -150mA, I_B = -15mA$			-0.4	V
		$I_C = -500mA, I_B = -50mA$			-0.75	V
*Base-Emitter Saturation Voltage	$V_{BE(sat)}$	$I_C = -150mA, I_B = -15mA$	-0.75		-0.95	V
		$I_C = -500mA, I_B = -50mA$			-1.3	V
Collector-Base Capacitance	C_{CB}	$V_{CB} = -10V, I_E = 0, f = 140KHz$			8.5	pF
Current Gain Bandwidth Product	f_T	$V_{CE} = -10V, I_C = -20mA$				
2N4402		$f = 100MHz$	150			MHz
2N4403			200			MHz
Turn On Time	t_{ON}	$V_{CC} = -30V, V_{BE} = -2V$			35	ns
		$I_C = -150mA, I_{B1} = -15mA$				
Turn Off Time	t_{OFF}	$V_{CC} = -30V, I_C = -150mA$			255	ns
		$I_{B1} = I_{B2} = -15mA$				

*Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

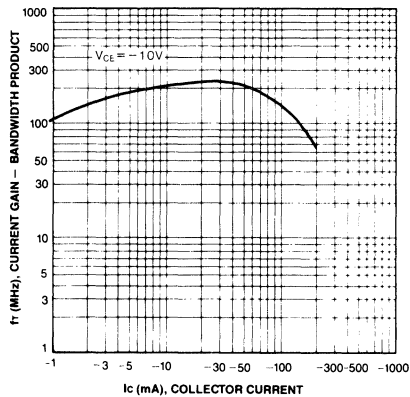
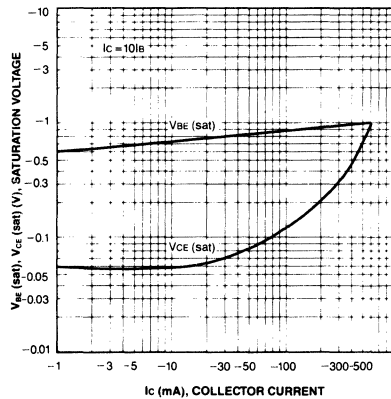
DC CURRENT GAIN



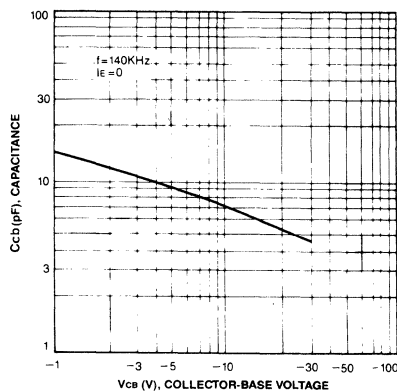
BASE-EMITTER ON VOLTAGE



CURRENT GAIN-BANDWIDTH PRODUCT

BASE-EMITTER SATURATION VOLTAGE
COLLECTOR-EMITTER SATURATION VOLTAGE

COLLECTOR-BASE CAPACITANCE



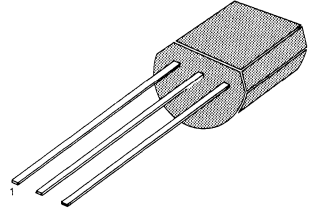
AMPLIFIER TRANSISTOR

- Collector-Emitter Voltage: $V_{CEO} = 50V$
- Collector Dissipation: $P_C (\text{max}) = 625mW$

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ C$)

Characteristic	Symbol	Rating	Unit
Collector-Base Voltage	V_{CBO}	-50	V
Collector-Emitter Voltage	V_{CEO}	-50	V
Emitter-Base Voltage	V_{EBO}	-3	V
Collector Current	I_C	-50	mA
Collector Dissipation	P_C	-625	mW
Junction Temperature	T_J	150	$^\circ C$
Storage Temperature	T_{stg}	-55 ~ 150	$^\circ C$

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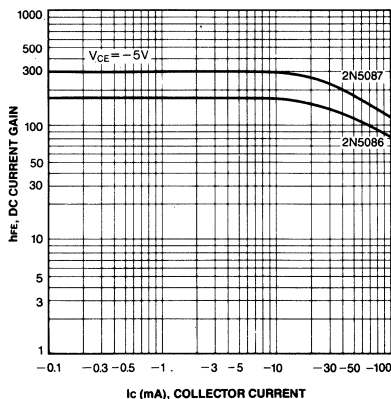
1. Emitter 2. Base 3. Collector

ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ C$)

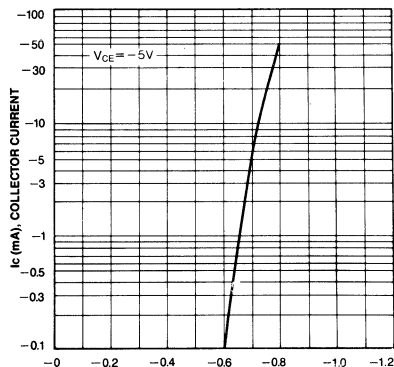
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Collector-Base Breakdown Voltage	BV_{CBO}	$I_C = -100\mu A, I_E = 0$	-50			V
*Collector-Emitter Breakdown Voltage	BV_{CEO}	$I_C = -1mA, I_B = 0$	-50			V
Collector Cut-off Current	I_{CBO}	$V_{CB} = -10V, I_E = 0$			-10	nA
		$V_{CB} = -35V, I_E = 0$			-50	nA
Base Cut-off Current	I_{EBO}	$V_{BE} = -3V, I_C = 0$			-50	nA
DC Current Gain	h_{FE}					
		$V_{CE} = -5V, I_C = -100\mu A$	150		500	
			250		800	
		$V_{CE} = -5V, I_C = -1mA$	150			
			250			
		* $V_{CE} = -5V, I_C = -10mA$	150			
Collector-Emitter Saturation Voltage	$V_{CE} (\text{sat})$	$I_C = -10mA, I_B = -1mA$			-0.3	V
Base-Emitter On Voltage	$V_{BE} (\text{on})$	$I_C = -1mA, V_{CE} = -5V$			-0.85	V
Collector-Base Capacitance	C_{CB}	$V_{CB} = -5V, I_E = 0$			4	pF
		$f = 100KHz$				
Current Gain bandwidth Product	f_T	$V_{CE} = -5V, I_C = -500\mu A$ $f = 20MHz$	40			MHz
Noise Figures	N_F	$V_{CE} = -5V, I_C = -20\mu A$ $R_S = 10K\Omega$ $f = 10Hz \text{ to } 15.7KHz$				
					3	dB
					2	dB
		$V_{CE} = -5V, I_C = -100\mu A$ $R_S = 3K\Omega, f = 1KHz$			3	dB
					2	dB

*Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

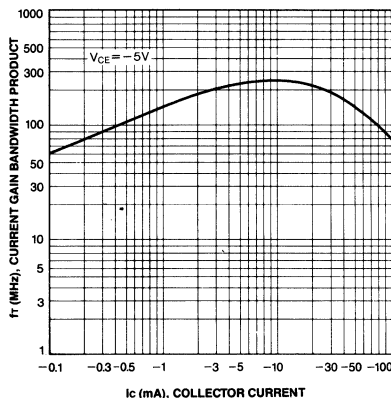
DC CURRENT GAIN



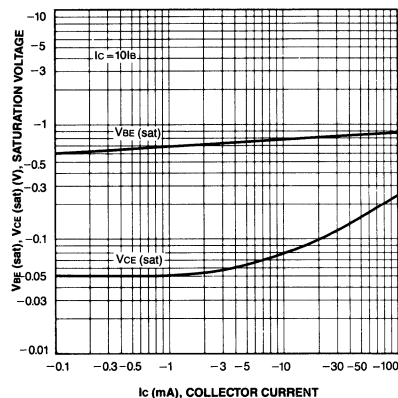
BASE-EMITTER ON VOLTAGE



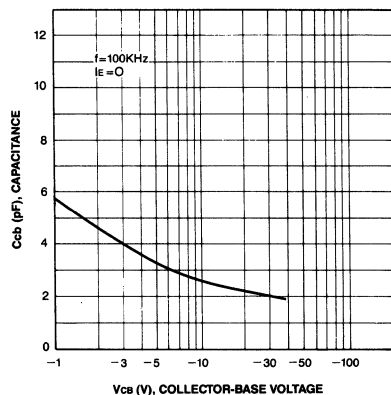
CURRENT GAIN BANDWIDTH PRODUCT



BASE-EMITTER SATURATION VOLTAGE
COLLECTOR-EMITTER SATURATION VOLTAGE



COLLECTOR-BASE CAPACITANCE



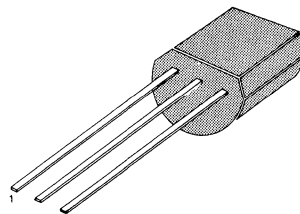
AMPLIFIER TRANSISTOR

- Collector-Emitter Voltage: $V_{CE0} = 2N5088: 30V$
 $2N5089: 25V$
- Collector Dissipation: $P_C (max) = 625mW$

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ C$)

Characteristic	Symbol	Rating	Unit
Collector-Base Voltage : 2N5088	V_{CBO}	30	V
2N5089		30	V
Collector-Emitter Voltage : 2N5088	V_{CEO}	25	V
2N5089		25	V
Emitter-Base Voltage	V_{EBO}	4.5	V
Collector Current	I_C	50	mA
Collector Dissipation	P_C	625	mW
Junction Temperature	T_J	150	$^\circ C$
Storage Temperature	T_{STG}	-55~150	$^\circ C$

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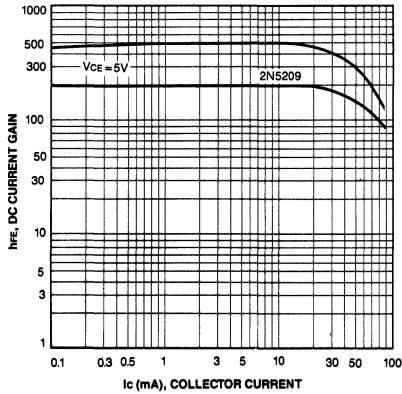
1. Emitter 2. Base 3. Collector

ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ C$)

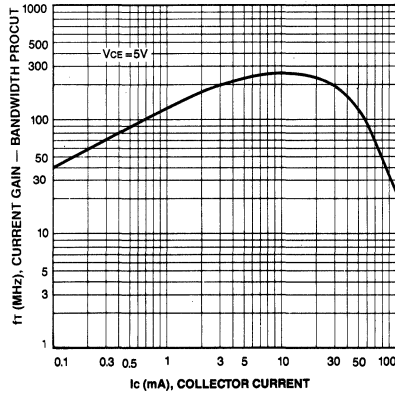
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
* Collector-Base Breakdown Voltage	BV_{CBO}	$I_C = 100\mu A, I_E = 0$				
: 2N5088			35			V
2N5089			30			V
* Collector-Emitter Breakdown Voltage	BV_{CEO}	$I_C = 1mA, I_B = 0$				
: 2N5088			30			V
2N5089			25			V
Collector Cut-off Current	I_{CBO}	$V_{CB} = 20V, I_E = 0$			50	nA
2N5088		$V_{CB} = 15V, I_E = 0$			50	nA
2N5089		$V_{BE} = 3V, I_C = 0$			50	nA
Base Cut-off Current	I_{EBO}	$V_{BE} = 4.5V, I_C = 0$			100	nA
DC Current Gain	h_{FE}	$V_{CE} = 5V, I_C = 100\mu A$	300		900	
: 2N5088		$I_C = 10mA, V_{CE} = 5V$	400		1,200	
2N5089		$f = 100KHz$	350			
2N5088		$* V_{CE} = 5V, I_C = 10mA$	450			
2N5089			300			
2N5088			400			
Collector-Emitter Saturation Voltage	$V_{CE} (sat)$	$I_C = 10mA, I_B = 1mA$			0.5	V
* Base-Emitter Saturation Voltage	$V_{BE} (on)$	$I_C = 10mA, V_{CE} = 5V$			0.8	V
Collector-Base Capacitance	C_{CB}	$V_{CB} = 5V, I_E = 0$			4	pF
Current Gain Bandwidth Product	f_T	$V_{CE} = 5V, I_C = 500\mu A$	50			MHz
Noise Figure	N_F	$f = 20MHz$				
		$V_{CE} = 5V, I_C = 100\mu A$				
		$R_S = 10K\Omega$				
		$f = 10Hz \text{ to } 15.7KHz$				
: 2N5088					3	dB
2N5089					2	dB

* Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

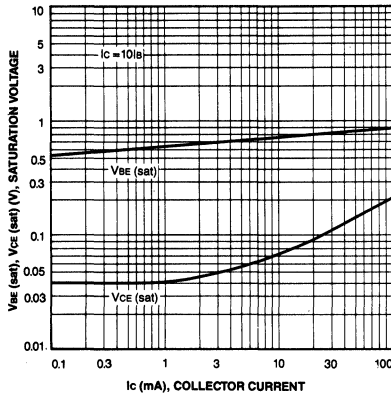
DC CURRENT GAIN



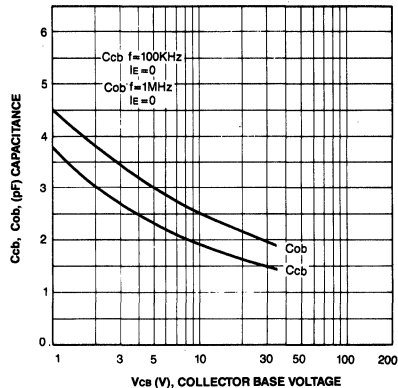
CURRENT GAIN BANDWIDTH PRODUCT



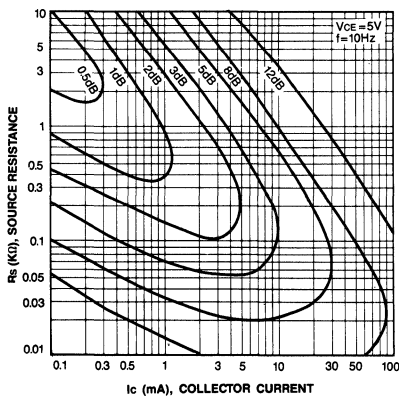
BASE-EMITTER SATURATION VOLTAGE
COLLECTOR-EMITTER SATURATION VOLTAGE



OUTPUT CAPACITANCE
COLLECTOR-BASE CAPACITANCE



NOISE FIGURE



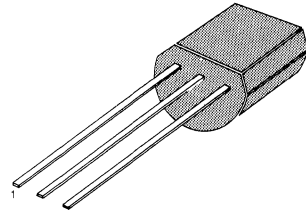
AMPLIFIER TRANSISTOR

- Collector-Emitter Voltage: $V_{CE0} = 160V$
- Collector Dissipation: $P_C(max) = 625mW$

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ C$)

Characteristic	Symbol	Rating	Unit
Collector-Base Voltage	V_{CBO}	180	V
Collector-Emitter Voltage	V_{CEO}	160	V
Emitter-Base Voltage	V_{EBO}	6	V
Collector Current	I_C	600	mA
Collector Dissipation	P_C	625	mW
Junction Temperature	T_J	150	$^\circ C$
Storage Temperature	T_{stg}	-55 ~ 150	$^\circ C$

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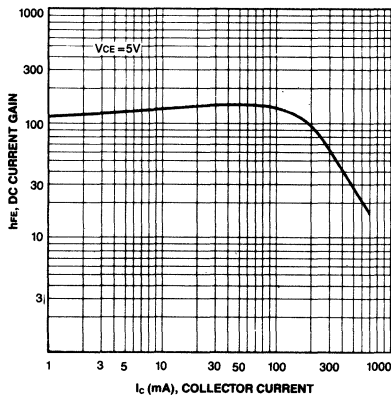
1. Emitter 2. Base 3. Collector

ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ C$)

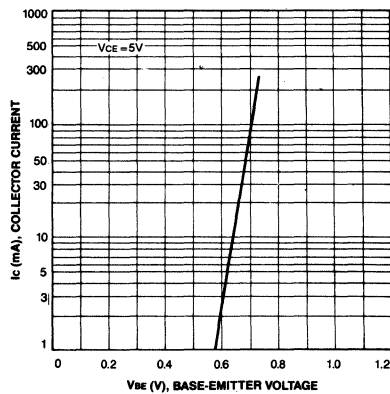
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Collector-Base Breakdown Voltage	BV_{CBO}	$I_C = 100\mu A, I_E = 0$	180			V
*Collector-Emitter Breakdown Voltage	BV_{CEO}	$I_C = 1mA, I_B = 0$	160			V
Emitter-Base Breakdown Voltage	BV_{EBO}	$I_E = 10\mu A, I_C = 0$	6			V
Collector Cut-off Current	I_{CBO}	$V_{CB} = 120V, I_E = 0$			50	nA
Emitter Cut-off Current	I_{EBO}	$V_{BE} = 4V, I_C = 0$			50	nA
*DC Current Gain	h_{FE}	$I_C = 1mA, V_{CE} = 5V$	80			
		$I_C = 10mA, V_{CE} = 5V$	80		250	
		$I_C = 50mA, V_{CE} = 5V$	30			
*Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 10mA, I_B = 1mA$			0.15	V
		$I_C = 50mA, I_B = 5mA$			0.2	V
*Base-Emitter Saturation Voltage	$V_{BE(sat)}$	$I_C = 10mA, I_B = 1mA$			1	V
		$I_C = 50mA, I_B = 5mA$			1	V
Current Gain Bandwidth Product	f_T	$I_C = 10mA, V_{CE} = 10V$ $f = 100MHz$	100		300	MHz
Output Capacitance	C_{ob}	$V_{CB} = 10V, I_E = 0$ $f = 1MHz$			6	pF
Noise Figure	NF	$I_C = 250\mu A, V_{CE} = 5V$ $R_S = 1K\Omega$ $f = 10Hz$ to $15.7KHz$			8	dB

* Pulse Test: Pulse Width = 300 μ S, Duty Cycle = 2%

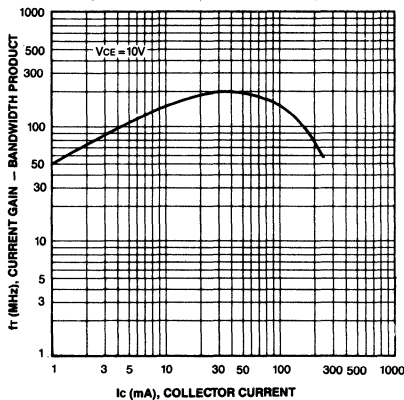
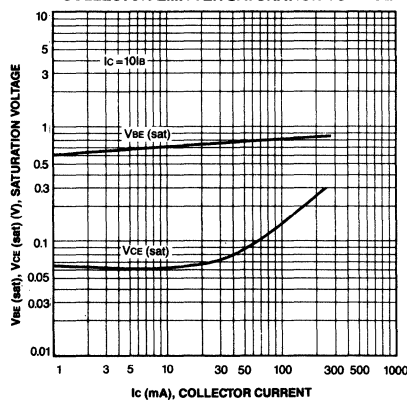
DC CURRENT GAIN



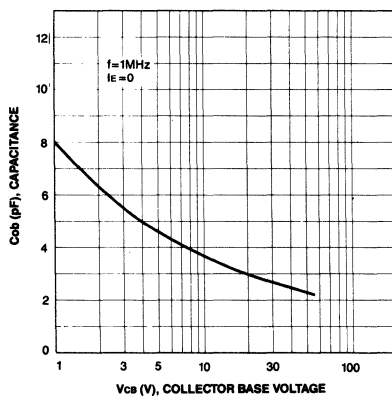
BASE-EMITTER ON VOLTAGE



CURRENT GAIN-BANDWIDTH PRODUCT

BASE-EMITTER SATURATION VOLTAGE
COLLECTOR-EMITTER SATURATION VOLTAGE

OUTPUT CAPACITANCE



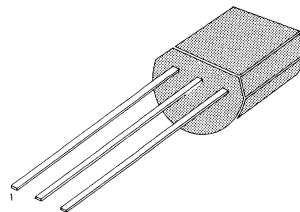
HIGH VOLTAGE TRANSISTOR

- Collector-Emitter Voltage: $V_{CEO} = 250V$
- Collector Dissipation: $P_C (\text{max}) = 625mW$

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ C$)

Characteristic	Symbol	Rating	Unit
Collector-Base Voltage	V_{CBO}	250	V
Collector-Emitter Voltage	V_{CEO}	250	V
Emitter-Base Voltage	V_{EBO}	6	V
Collector Current	I_C	500	mA
Collector Dissipation	P_C	625	mW
Junction Temperature	T_J	150	$^\circ C$
Storage Temperature	T_{stg}	$-55 \sim 150$	$^\circ C$

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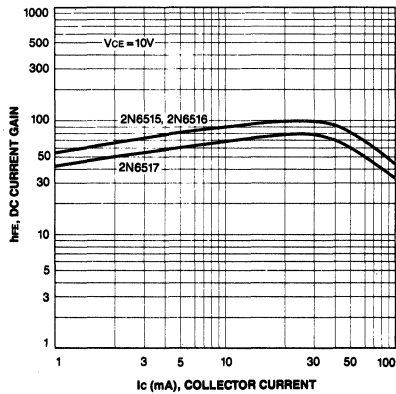
1. Emitter 2. Base 3. Collector

ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ C$)

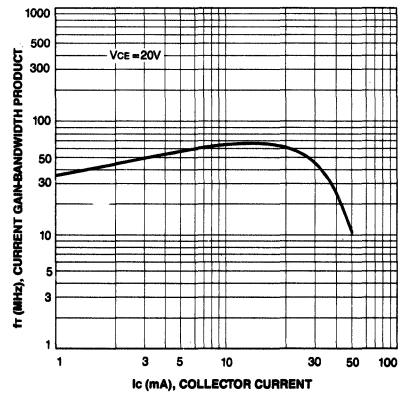
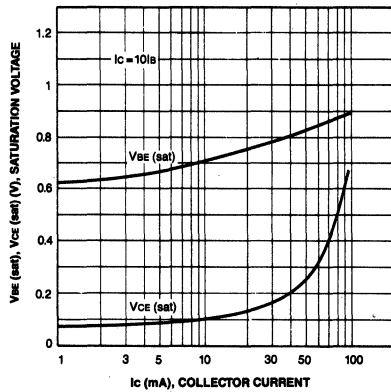
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
*Collector-Emitter Breakdown Voltage	BV_{CEO}	$I_C = 1mA, I_B = 0$	250			V
Collector-Base Breakdown Voltage	BV_{CBO}	$I_C = 100\mu A, I_E = 0$	250			V
Emitter-Base Breakdown Voltage	BV_{EBO}	$I_E = 10\mu A, I_C = 0$	6			V
Collector Cut-off Current	I_{CBO}	$V_{CB} = 150V, I_E = 0$			50	nA
Emitter Cut-off Current	I_{EBO}	$V_{BE} = 5V, I_C = 0$			50	nA
*DC Current Gain	h_{FE}	$I_C = 1mA, V_{CE} = 10V$	35			
		$I_C = 10mA, V_{CE} = 10V$	50			
		$I_C = 30mA, V_{CE} = 10V$	50		300	
		$I_C = 50mA, V_{CE} = 10V$	45		220	
		$I_C = 100mA, V_{CE} = 10V$	25			
Collector-Emitter Saturation Voltage	$V_{CE} (\text{sat})$	$I_C = 10mA, I_B = 1mA$			0.3	V
		$I_C = 20mA, I_B = 2mA$			0.35	V
		$I_C = 30mA, I_B = 3mA$			0.5	V
		$I_C = 50mA, I_B = 5mA$			1	V
Base-Emitter Saturation Voltage	$V_{BE} (\text{sat})$	$I_C = 10mA, I_B = 1mA$			0.75	V
		$I_C = 20mA, I_B = 2mA$			0.85	V
		$I_C = 30mA, I_B = 3mA$			0.9	V
Collector-Base Capacitance	C_{cb}	$V_{CB} = 20V, I_E = 0$			6	pF
		$f = 1MHz$				
*Current Gain Bandwidth Product	f_T	$I_C = 10mA, V_{CE} = 20V$	40		200	MHz
		$f = 20MHz$				
Base Emitter On Voltage	$V_{BE} (\text{on})$	$I_C = 100mA, V_{CE} = 10V$			2	V

* Pulse Test: Pulse Width=300 μ S, Duty Cycle=2%

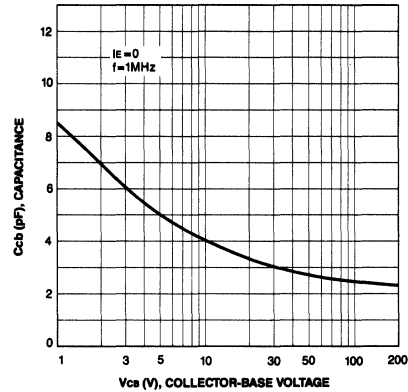
DC CURRENT GAIN



CURRENT GAIN BANDWIDTH PRODUCT

COLLECTOR-EMITTER SATURATION VOLTAGE
BASE-EMITTER SATURATION VOLTAGE

COLLECTOR-BASE CAPACITANCE



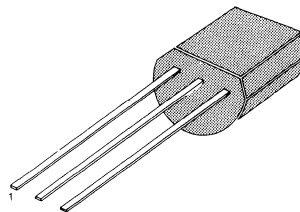
AMPLIFIER TRANSISTOR

- Collector-Emitter Voltage: $V_{CE0} =$ KSP05: 60V
KSP06: 80V
- Collector Dissipation: P_C (max)=625mW

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Characteristic	Symbol	Rating	Unit
Collector Base Voltage	V_{CBO}		
KSP05		60	V
KSP06		80	V
Collector-Emitter Voltage	V_{CEO}		
KSP05		60	V
KSP06		80	V
Emitter-Base Voltage	V_{EBO}	4	V
Collector Current	I_C	500	mA
Collector Dissipation	P_C	625	mW
Junction Temperature	T_J	150	$^\circ\text{C}$
Storage Temperature	T_{STG}	- 55 ~ 150	$^\circ\text{C}$

TO-92



1. Emitter 2. Base 3. Collector

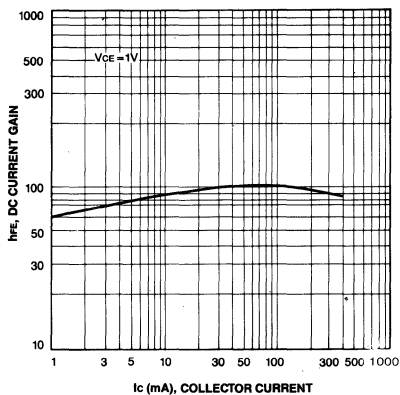
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ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

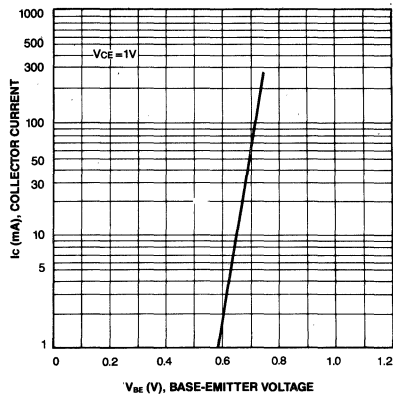
Characteristic	Symbol	Test Condition	Min	Max	Unit
* Collector-Emitter Breakdown Voltage	BV_{CEO}	$I_C = 1\text{mA}, I_B = 0$			
KSP05			60		V
KSP06			80		V
Emitter-Base Breakdown Voltage	BV_{EBO}	$I_E = 100\mu\text{A}, I_C = 0$	4		V
Collector Cut-off Current	I_{CBO}	$V_{CB} = 60\text{V}, I_E = 0$		0.1	μA
		$V_{CB} = 80\text{V}, I_E = 0$		0.1	μA
		$V_{CE} = 60\text{V}, I_B = 0\text{V}$		0.1	μA
Collector Cut-off Current	I_{CEO}	$V_{CE} = 1\text{V}, I_C = 10\text{mA}$	50		
DC Current Gain	h_{FE}	$V_{CE} = 1\text{V}, I_C = 100\text{mA}$	50		
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 100\text{mA}, I_B = 10\text{mA}$		0.25	V
Base-Emitter On Voltage	$V_{BE(on)}$	$V_{CE} = 1\text{V}, I_C = 100\text{mA}$		1.2	V
Current Gain Bandwidth Product	f_T	$V_{CE} = 2\text{V}, I_C = 10\text{mA}$ $f = 100\text{MHz}$	100		MHz

* Pulse Test: $PW = 300\mu\text{s}$, Duty Cycle = 2%

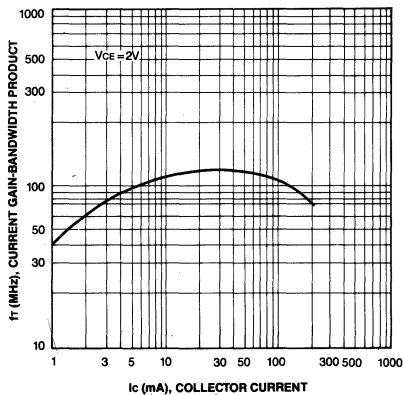
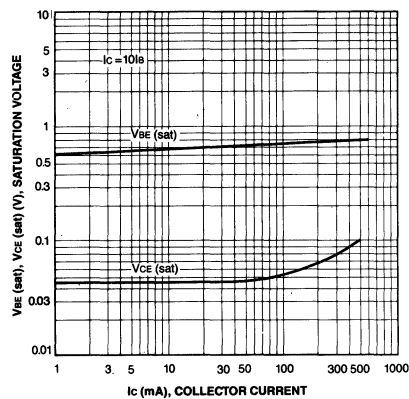
DC CURRENT GAIN



BASE-EMITTER ON VOLTAGE



CURRENT GAIN-BANDWIDTH PRODUCT

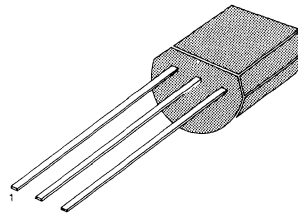
COLLECTOR-EMITTER SATURATION VOLTAGE
BASE-EMITTER SATURATION VOLTAGE

VHF/UHF TRANSISTOR

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Characteristic	Symbol	Rating	Unit
Collector-Base Voltage	V_{CBO}	30	V
Collector-Emitter Voltage	V_{CEO}	25	V
Emitter-Base Voltage	V_{EBO}	3.0	V
Collector Dissipation ($T_a = 25^\circ\text{C}$)	P_C	350	mW
Derate above 25°C		2.8	mW/ $^\circ\text{C}$
Collector Dissipation ($T_c = 25^\circ\text{C}$)	P_C	1.0	W
Derate above 25°C		8.0	mW/ $^\circ\text{C}$
Junction Temperature	T_j	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	$-55 \sim 150$	$^\circ\text{C}$
Thermal Resistance, Junction to Case	$R_{th(j-c)}$	125	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{th(j-a)}$	357	$^\circ\text{C/W}$

TO-92



1. Base 2. Emitter 3. Collector

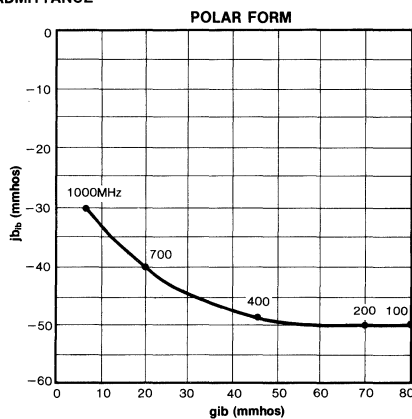
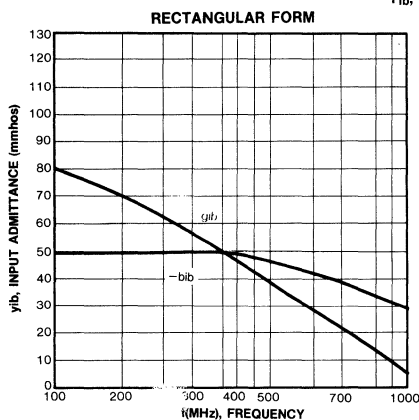
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ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

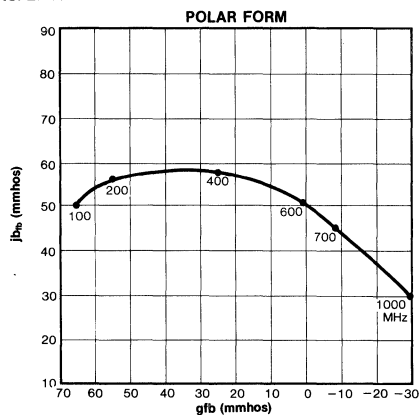
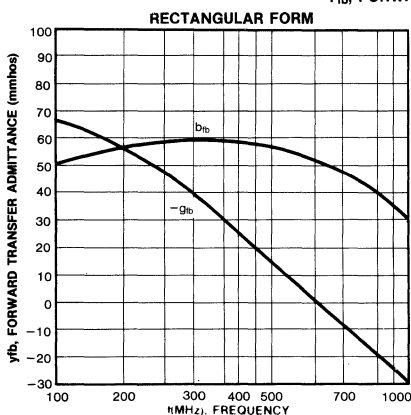
Characteristic	Symbol	Test Condition	Min	Max	Unit
Collector-Base Breakdown Voltage	BV_{CBO}	$I_C = 100\mu\text{A}$, $I_E = 0$	30		V
Collector-Emitter Breakdown Voltage	BV_{CEO}	$I_C = 1\text{mA}$, $I_B = 0$	25		V
Emitter-Base Breakdown Voltage	BV_{EBO}	$I_E = 10\mu\text{A}$, $I_C = 0$	3.0		V
Collector Cutoff Current	I_{CBO}	$V_{CB} = 25\text{V}$, $I_E = 0$		100	nA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = 2\text{V}$, $I_C = 0$		100	nA
DC Current Gain	h_{FE}	$V_{CE} = 10\text{V}$, $I_C = 4\text{mA}$	60		
Collector Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 4\text{mA}$, $I_B = 0.4\text{mA}$		0.5	V
Base-Emitter On Voltage	$V_{BE(on)}$	$V_{CE} = 10\text{V}$, $I_C = 4\text{mA}$		0.95	V
Current Gain Bandwidth Product	f_T	$V_{CE} = 10\text{V}$, $I_C = 4\text{mA}$, $f = 100\text{MHz}$	650		MHz
Collector Base Capacitance	C_{cb}	$V_{CB} = 10\text{V}$, $I_E = 0$, $f = 1\text{MHz}$		0.7	pF
Collector Base Feedback Capacitance	C_{rb}	$V_{CB} = 10\text{V}$, $I_E = 0$, $f = 1\text{MHz}$			
KSP10			0.35	0.65	pF
KSP11			0.6	0.9	pF
Collector Base Time Constant	$C_c \cdot r_{bb'}$	$V_{CB} = 10\text{V}$, $I_C = 4\text{mA}$, $f = 31.8\text{MHz}$		9.0	ps

COMMON-BASE y PARAMETERS vs FREQUENCY
 $(V_{CB} = 10V, I_C = 4mA, T_a = 25^\circ C)$

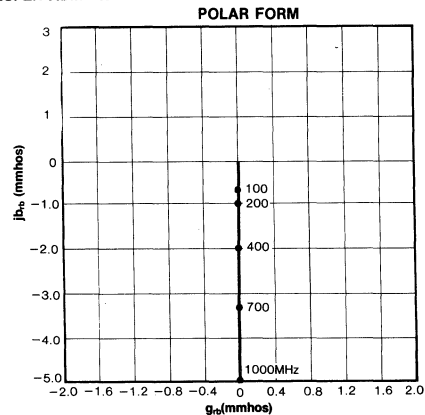
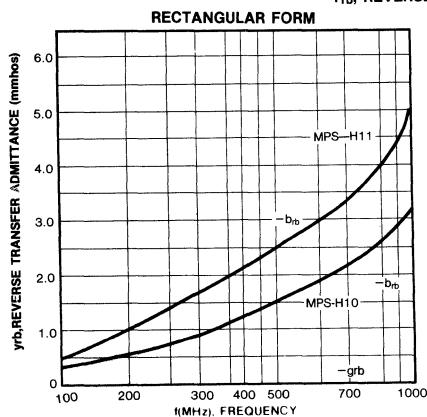
Y_{ib} , INPUT ADMITTANCE



Y_{fb} , FORWARD TRANSFER ADMITTANCE

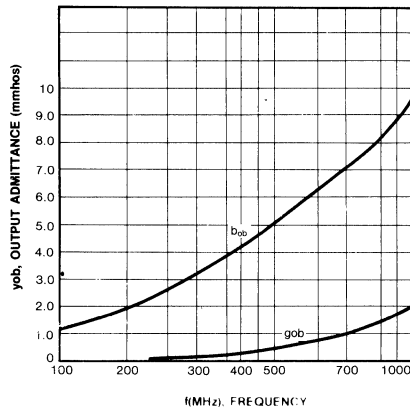


Y_{rb} , REVERSE TRANSFER ADMITTANCE

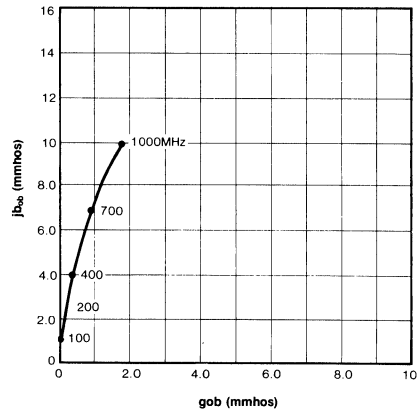


Y_{ob} , OUTPUT ADMITTANCE

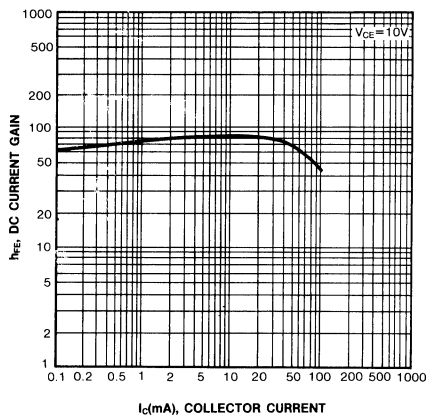
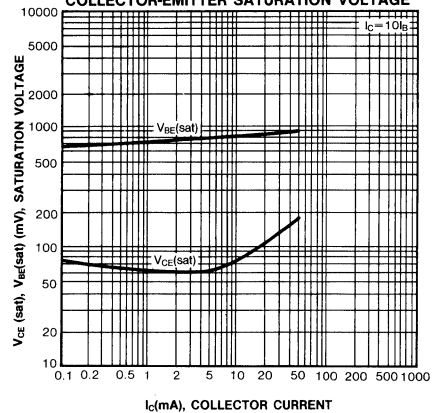
RECTANGULAR FORM



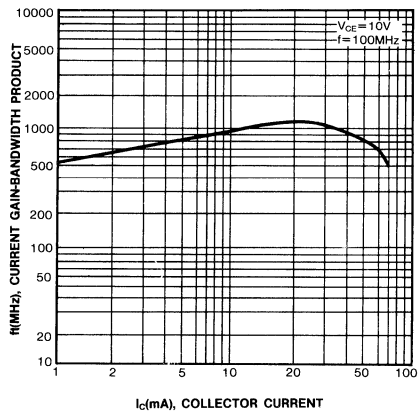
POLAR FORM



DC CURRENT GAIN

BASE-EMITTER SATURATION VOLTAGE
COLLECTOR-EMITTER SATURATION VOLTAGE

CURRENT GAIN BANDWIDTH PRODUCT



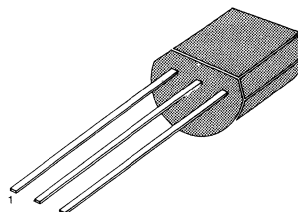
DARLINGTON TRANSISTOR

- Collector-Emitter Voltage: $V_{CES}=30V$
- Collector Dissipation: $P_c(\max)=625mW$

ABSOLUTE MAXIMUM RATINGS ($T_a=25^\circ C$)

Characteristic	Symbol	Rating	Unit
Collector-Base Voltage	V_{CBO}	30	V
Collector-Emitter Voltage	V_{CES}	30	V
Emitter-Base Voltage	V_{EBO}	10	V
Collector Current	I_C	500	mA
Collector Dissipation	P_C	625	mW
Junction Temperature	T_J	150	$^\circ C$
Storage Temperature	T_{stg}	-55 ~ 150	$^\circ C$

TO-92

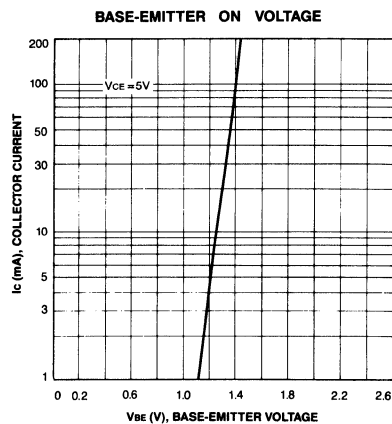
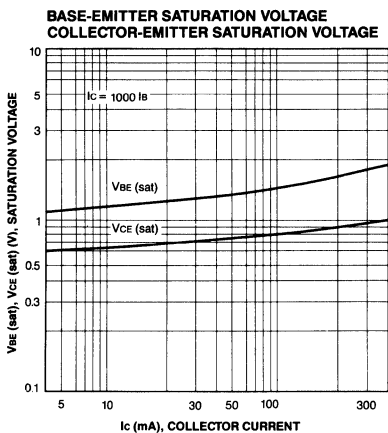
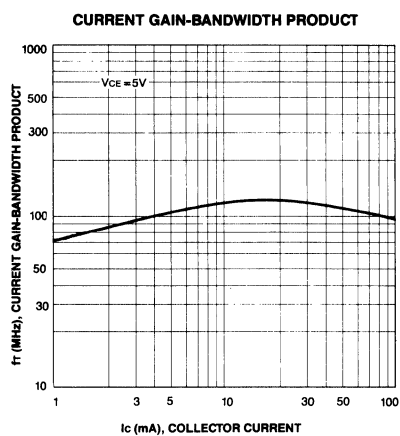
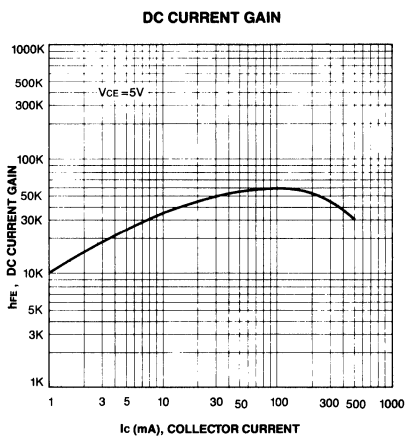


1. Emitter 2. Base 3. Collector

ELECTRICAL CHARACTERISTICS ($T_a=25^\circ C$)

Characteristic	Symbol	Test Conditions	Min	Max	Unit
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C=100\mu A, I_B=0$	30		V
Collector Cut-off Current	I_{CBO}	$V_{CB}=30V, I_E=0$		100	nA
Emitter Cut-off Current	I_{EBO}	$V_{BE}=10V, I_C=0$		100	nA
*DC Current Gain	h_{FE}				
	KSP13	$V_{CE}=5V, I_C=10mA$	5,000		
	KSP14		10,000		
	KSP13	$V_{CE}=5V, I_C=100mA$	10,000		
	KSP14		20,000		
*Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C=100mA, I_B=0.1mA$		1.5	V
*Base-Emitter On Voltage	$V_{BE(on)}$	$V_{CE}=5V, I_C=100mA$		2.0	V
Current Gain Bandwidth Product	f_T	$V_{CE}=5V, I_C=10mA$ $f=100MHz$	125		MHz

*Pulse Test: Pulse Width=300 μs , Duty Cycle=2%



2

GENERAL PURPOSE TRANSISTOR

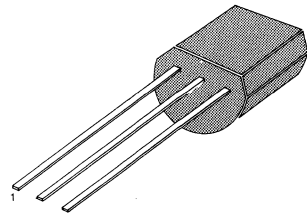
- Collector-Emitter Voltage: $V_{CE0} = 40V$
- Collector Dissipation: $P_C (\text{max}) = 625mW$

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ C$)

Characteristic	Symbol	Rating	Unit
Collector-Base Voltage	V_{CBO}	75	V
Collector-Emitter Voltage	V_{CEO}	40	V
Emitter-Base Voltage	V_{EBO}	6	V
Collector Current	I_C	600	mA
Collector Dissipation	P_C	625	mW
Junction Temperature	T_J	150	$^\circ C$
Storage Temperature	T_{stg}	-55 ~ 150	$^\circ C$

- Refer to KSP2222 for graphs

TO-92



1. Emitter 2. Base 3. Collector

ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ C$)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Collector-Base Breakdown Voltage	BV_{CBO}	$I_C = 10\mu A, I_E = 0$	75			V
Collector-Emitter Breakdown Voltage	BV_{CEO}	$I_C = 10mA, I_B = 0$	40			V
Emitter-Base Breakdown Voltage	BV_{EBO}	$I_E = 10\mu A, I_C = 0$	6			V
Collector Cut-off Current	I_{CBO}	$V_{CB} = 60V, I_E = 0$			0.01	μA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = 3V, I_C = 0$			10	nA
DC Current Gain	h_{FE}	$I_C = 0.1mA, V_{CE} = 10V$	35			
		$I_C = 1mA, V_{CE} = 10V$	50			
		$I_C = 10mA, V_{CE} = 10V$	75			
		$I_C = 150mA, V_{CE} = 10V$	100		300	
		$I_C = 500mA, V_{CE} = 10V$	40			
*Collector-Emitter Saturation Voltage	$V_{CE} (\text{sat})$	$I_C = 150mA, I_B = 15mA$			0.3	V
		$I_C = 500mA, I_B = 50mA$			1	V
*Base-Emitter Saturation Voltage	$V_{BE} (\text{sat})$	$I_C = 150mA, I_B = 15mA$		0.6	1.2	V
		$I_C = 500mA, I_B = 50mA$			2	V
Current Gain Bandwidth Product	f_T	$I_C = 20mA, V_{CE} = 20V$	300			MHz
		$f = 100MHz$				
Output Capacitance	C_{ob}	$V_{CB} = 10V, I_E = 0, f = 1MHz$			8	pF
Turn On Time	t_{on}	$V_{CC} = 30V, I_C = 150mA$			35	ns
		$I_{B1} = 15mA, V_{BE} (\text{off}) = 0.5V$				
Turn Off Time	t_{off}	$V_{CC} = 30V, I_C = 150mA$			285	ns
		$I_{B1} = I_{B2} = 15mA$				
Noise Figure	NF	$I_C = 100\mu A, V_{CE} = 10V$			4	dB
		$R_S = 1K\Omega, f = 1KHz$				

* Pulse Test: Pulse Width = $300\mu s$, Duty Cycle = 2%
Also available as a PN2222A

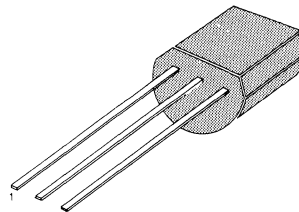
DARLINGTON TRANSISTOR

- Collector-Emitter Voltage: V_{CES} = KSP25: 40V
KSP26: 50V
KSP27: 60V
- Collector Dissipation: P_C (max)=625mW

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Characteristic	Symbol	Rating	Unit
Collector Base Voltage	V_{CES}		
KSP25		40	V
KSP26		50	V
KSP27		60	V
Emitter-Base Voltage	V_{EBO}	10	V
Collector Current	I_C	500	mA
Collector Dissipation	P_C	625	mW
Junction Temperature	T_J	150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55 ~ 150	$^\circ\text{C}$

TO-92

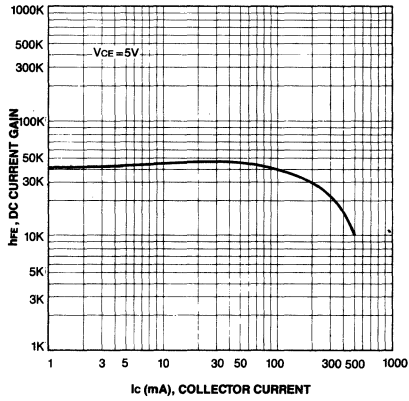
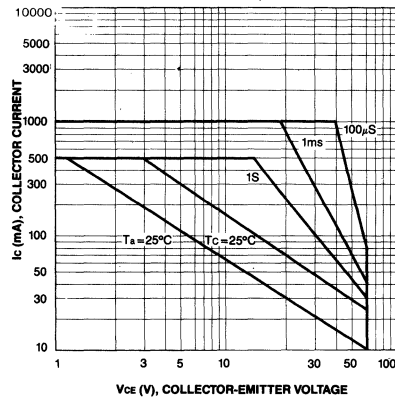
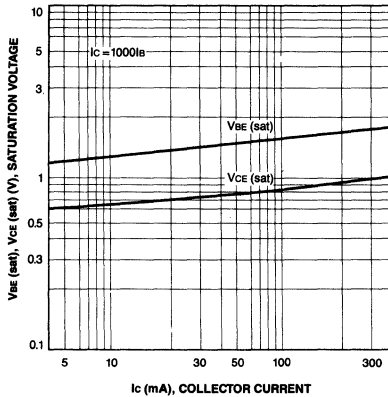
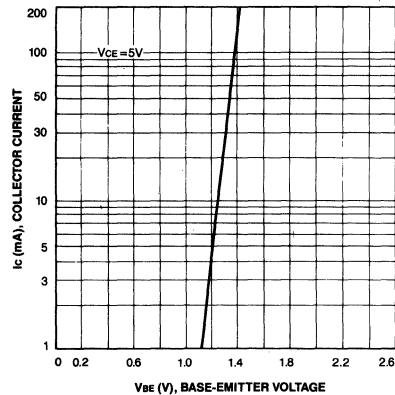


1. Emitter 2. Base 3. Collector

ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

Characteristic	Symbol	Test Condition	Min	Max	Unit
Collector-Base Breakdown Voltage	BV_{CES}	$I_C = 100\mu\text{A}, I_E = 0$			
KSP25			40		V
KSP26			50		V
KSP27			60		V
Collector-Base Breakdown Voltage	BV_{CBO}	$I_C = 100\mu\text{A}, I_E = 0$			
KSP25			40		V
KSP26			50		V
KSP27			60		V
Collector Cut-off Current	I_{CBO}				
KSP25		$V_{CE} = 30\text{V}, I_E = 0$		100	nA
KSP26		$V_{CE} = 40\text{V}, I_E = 0$		100	nA
KSP27		$V_{CE} = 50\text{V}, I_E = 0$		100	nA
Emitter Cut-off Current	I_{EBO}	$V_{CE} = 10\text{V}, I_B = 0$		100	nA
*DC Current Gain	h_{FE}	$V_{CE} = 5\text{V}, I_C = 10\text{mA}$ $V_{CE} = 5\text{V}, I_C = 100\text{mA}$	10K 10K		
*Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 100\text{mA}, I_B = 0.1\text{mA}$		1.5	V
*Base-Emitter On Voltage	$V_{BE(on)}$	$V_{CE} = 5\text{V}, I_C = 100\text{mA}$		2	V

* Pulse Test: $PW = 300\mu\text{s}$, Duty Cycle = 2%

DC CURRENT GAIN**SAFE OPERATING AREA****BASE-EMITTER SATURATION VOLTAGE
COLLECTOR-EMITTER SATURATION VOLTAGE****BASE-EMITTER ON VOLTAGE**

GENERAL PURPOSE TRANSISTOR

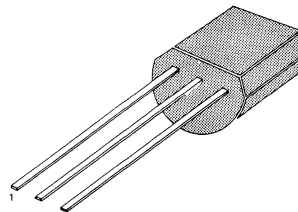
- Collector-Emitter Voltage: $V_{CE0} = 60V$
- Collector Dissipation: $P_C (\text{max}) = 625mW$

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ C$)

Characteristic	Symbol	Rating	Unit
Collector-Base Voltage	V_{CBO}	-60	V
Collector-Emitter Voltage	V_{CEO}	-60	V
Emitter-Base Voltage	V_{EBO}	-5	V
Collector Current	I_C	-600	mA
Collector Dissipation	P_C	625	mW
Junction Temperature	T_J	150	$^\circ C$
Storage Temperature	T_{stg}	-55 ~ 150	$^\circ C$

- Refer to KSP2907 for graphs

TO-92



1. Emitter 2. Base 3. Collector

ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ C$)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Collector-Base Breakdown Voltage	BV_{CBO}	$I_C = -10\mu A, I_E = 0$	-60			V
*Collector-Emitter Breakdown Voltage	BV_{CEO}	$I_C = -10mA, I_B = 0$	-60			V
Emitter-Base Breakdown Voltage	BV_{EBO}	$I_E = -10\mu A, I_C = 0$	-5			V
Collector Cut-off Current	I_{CBO}	$V_{CB} = -50V, I_E = 0$			-10	nA
DC Current Gain	h_{FE}	$I_C = -0.1mA, V_{CE} = -10V$	75			
		$I_C = -1mA, V_{CE} = -10V$	100			
		$I_C = -10mA, V_{CE} = -10V$	100			
		* $I_C = -150mA, V_{CE} = -10V$	100		300	
		* $I_C = -500mA, V_{CE} = -10V$	50			
*Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = -150mA, I_B = -15mA$			-0.4	V
		$I_C = -500mA, I_B = -50mA$			-1.6	V
*Base-Emitter Saturation Voltage	$V_{BE(sat)}$	$I_C = -150mA, I_B = -15mA$			-1.3	V
		$I_C = -500mA, I_B = -50mA$			-2.6	V
Output Capacitance	C_{ob}	$V_{CB} = -10V, I_E = 0$ $f = 1MHz$			8	pF
*Current Gain Bandwidth Product	f_T	$I_C = -50mA, V_{CE} = -20V$ $f = 100MHz$	200			MHz
Turn On Time	t_{on}	$V_{CC} = -30V, I_C = -150mA$ $I_{B1} = -15mA$			45	ns
Turn Off Time	t_{off}	$V_{CC} = -6V, I_C = -150mA$ $I_{B1} = I_{B2} = -15mA$			100	ns

*Pulse Test: Pulse Width=300 μs , Duty Cycle=2%

Also available as a PN2907A

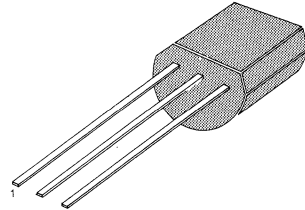
HIGH VOLTAGE TRANSISTOR

- Collector-Emitter Voltage: V_{CEO} = KSP42: 300V
KSP43: 200V
- Collector Dissipation: P_C (max)=625mW

ABSOLUTE MAXIMUM RATINGS ($T_a=25^\circ\text{C}$)

Characteristic	Symbol	Rating	Unit
Collector-Base Voltage	KSP42 KSP43	V_{CBO}	
		300 200	V V
Collector-Emitter Voltage	KSP42 KSP43	V_{CEO}	
		300 200	V V
Emitter-Base Voltage		V_{EBO}	6 V
Collector Current		I_C	500 mA
Collector Dissipation		P_C	625 mW
Junction Temperature		T_J	150 $^\circ\text{C}$
Storage Temperature		T_{STG}	-55~150 $^\circ\text{C}$

TO-92



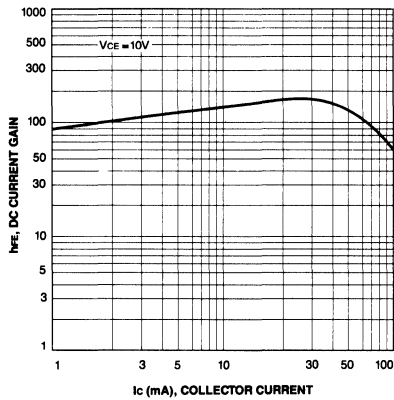
1. Emitter 2. Base 3. Collector

ELECTRICAL CHARACTERISTICS ($T_a=25^\circ\text{C}$)

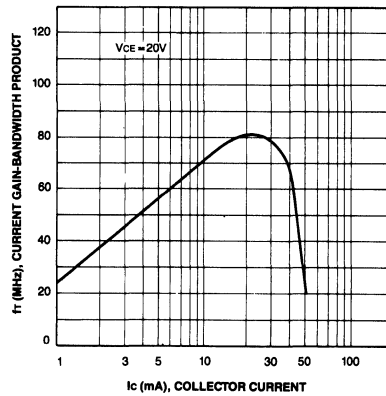
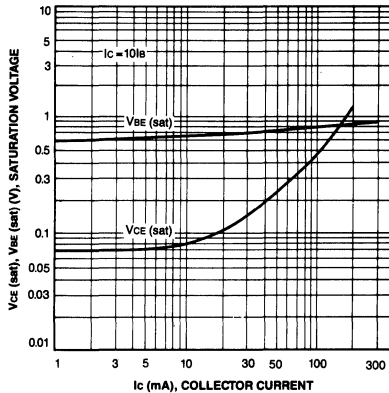
Characteristic	Symbol	Test Condition	Min	Max	Unit
Collector-Base Breakdown Voltage	KSP42 KSP43	$I_C = 100\mu\text{A}, I_B = 0$	300 200		V V
*Collector-Emitter Breakdown Voltage	KSP42 KSP43	$I_C = 1\text{mA}, I_B = 0$	300 200		V V
Emitter-Base Breakdown Voltage		$I_E = 100\mu\text{A}, I_C = 0$	6		V
Collector Cut-off Current	KSP42 KSP43	$V_{CB} = 200\text{V}, I_E = 0$ $V_{CB} = 160\text{V}, I_E = 0$		100 100	nA nA
Emitter Cut-off Current	KSP42 KSP43	$V_{BE} = 6\text{V}, I_C = 0$ $V_{BE} = 4\text{V}, I_C = 0$		100 100	nA nA
*DC Current Gain	h_{FE}	$V_{CE} = 10\text{V}, I_C = 1\text{mA}$ $V_{CE} = 10\text{V}, I_C = 10\text{mA}$ $V_{CE} = 10\text{V}, I_C = 30\text{mA}$	25 40 40		
*Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 20\text{mA}, I_B = 2\text{mA}$		0.5	V
*Base-Emitter Saturation Voltage	$V_{BE(sat)}$	$I_C = 20\text{mA}, I_B = 2\text{mA}$		0.9	V
Collector-Base Capacitance	KSP42 KSP43	$V_{CB} = 20\text{V}, I_E = 0$ $f = 1\text{MHz}$		3 4	pF pF
Current Gain Bandwidth Product	f_T	$V_{CE} = 20\text{V}, I_C = 10\text{mA}$ $f = 100\text{MHz}$	50		MHz

* Pulse Test: $PW = 300\mu\text{s}$, Duty Cycle = 2%

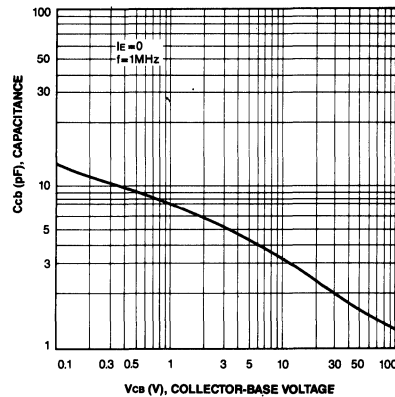
DC CURRENT GAIN



CURRENT GAIN-BANDWIDTH PRODUCT

COLLECTOR-EMITTER SATURATION VOLTAGE
BASE-EMITTER SATURATION VOLTAGE

COLLECTOR-BASE CAPACITANCE



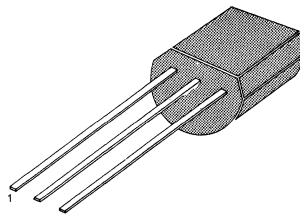
HIGH VOLTAGE TRANSISTOR

- Collector-Emitter Voltage: $V_{CEO} = \text{KSP44: } 400\text{V}$
KSP45: 350V
- Collector Dissipation: $P_c(\text{max}) = 625\text{mW}$

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Characteristic	Symbol	Rating	Unit
Collector-Base Voltage	V_{CBO}	KSP44 500	V
		KSP45 400	V
Collector-Emitter Voltage	V_{CEO}	KSP44 400	V
		KSP45 350	V
		6	V
Emitter-Base Voltage	V_{EBO}	6	V
Collector Current	I_C	300	mA
Collector Dissipation ($T_a = 25^\circ\text{C}$)	P_C	625	mW
Collector Dissipation ($T_C = 25^\circ\text{C}$)	P_C	1.5	W
Junction Temperature	T_J	150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55~150	$^\circ\text{C}$

TO-92



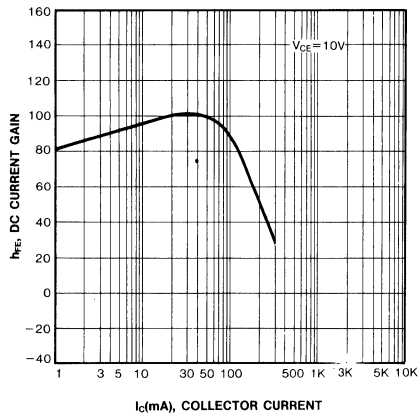
1. Emitter 2. Base 3. Collector

ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

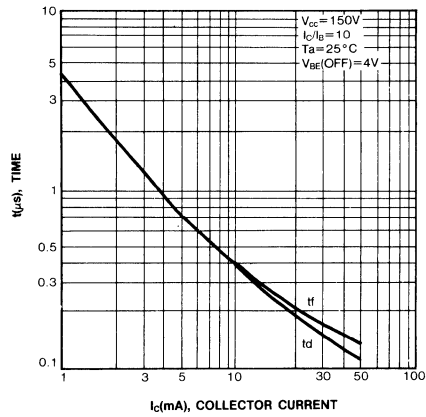
Characteristic	Symbol	Test Condition	Min	Max	Unit
Collector-Base Breakdown Voltage	BV_{CBO}	$I_C = 100\mu\text{A}, I_B = 0$	500		V
			400		V
*Collector-Emitter Breakdown Voltage	BV_{CEO}	$I_C = 1\text{mA}, I_B = 0$	400		V
			350		V
Emitter-Base Breakdown Voltage	BV_{EBO}	$I_E = 100\mu\text{A}, I_C = 0$	6		V
					V
Collector Cut-off Current	I_{CBO}	$V_{CB} = 400\text{V}, I_E = 0$ $V_{CB} = 320\text{V}, I_E = 0$		0.1	μA
				0.1	μA
Collector Cut-off Current	I_{CES}	$V_{CE} = 400\text{V}, I_B = 0$ $V_{CE} = 320\text{V}, I_B = 0$		0.5	μA
				0.5	μA
Emitter Cut-off Current	I_{EBO}	$V_{EB} = 4\text{V}, I_C = 0$		0.1	μA
					μA
*DC Current Gain	h_{FE}	$V_{CE} = 10\text{V}, I_C = 1\text{mA}$	40		
		$V_{CE} = 10\text{V}, I_C = 10\text{mA}$	50	200	
		$V_{CE} = 10\text{V}, I_C = 50\text{mA}$	45		
		$V_{CE} = 10\text{V}, I_C = 100\text{mA}$	40		
*Collector-Emitter Saturation Voltage	$V_{CE}(\text{sat})$	$I_C = 1\text{mA}, I_B = 0.1\text{mA}$		0.4	V
		$I_C = 10\text{mA}, I_B = 1\text{mA}$		0.5	V
		$I_C = 50\text{mA}, I_B = 5\text{mA}$		0.75	V
*Base-Emitter Saturation Voltage	$V_{BE}(\text{sat})$	$I_C = 10\text{mA}, I_B = 1\text{mA}$		0.75	V
					V
Output Capacitance	C_{OB}	$V_{CB} = 20\text{V}, I_E = 0$		7	pF
		$f = 1\text{MHz}$			

* Pulse Test: $PW = 300\mu\text{s}$, Duty Cycle = 2%

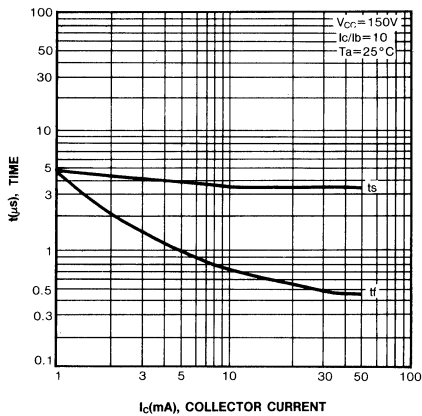
DC CURRENT GAIN



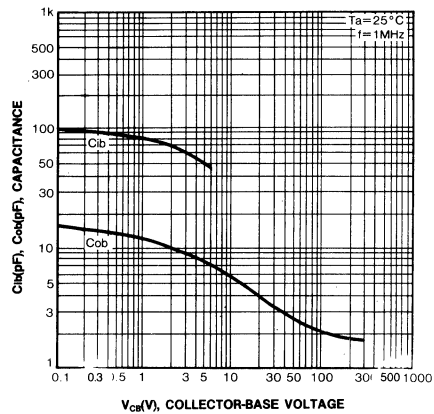
TURN-ON SWITCHING TIMES



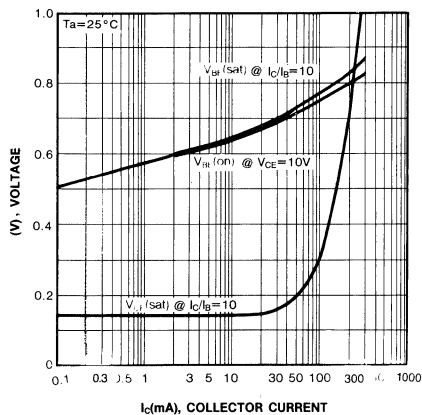
TURN-OFF SWITCHING TIMES



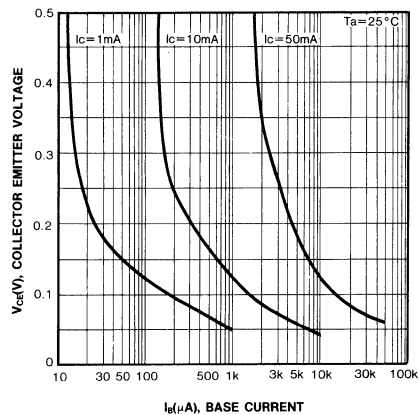
CAPACITANCE



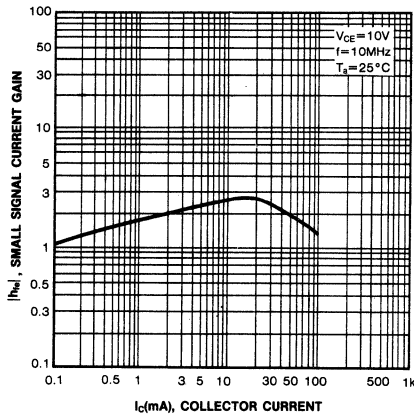
ON VOLTAGE



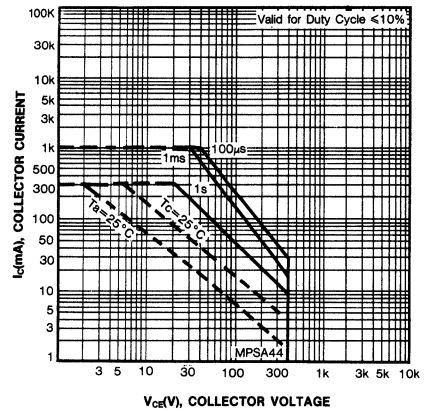
COLLECTOR SATURATION REGION



HIGH FREQUENCY CURRENT GAIN



SAFE OPERATING AREA



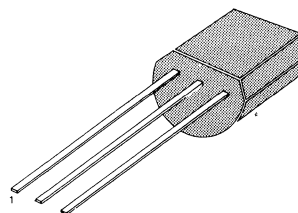
AMPLIFIER TRANSISTOR

- Collector-Emitter Voltage: $V_{CE0} =$ KSP55: 60V
KSP56: 80V
- Collector Dissipation: P_C (max)=625mW

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Characteristic	Symbol	Rating	Unit
Collector-Base Voltage	V_{CBO}	-60	V
KSP55		-80	V
Collector-Emitter Voltage	V_{CEO}	-60	V
KSP55		-80	V
Emitter-Base Voltage	V_{EBO}	-4	V
Collector Current	I_C	-500	mA
Collector Dissipation	P_C	625	mW
Junction Temperature	T_J	150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55~150	$^\circ\text{C}$

TO-92



1. Emitter 2. Base 3. Collector

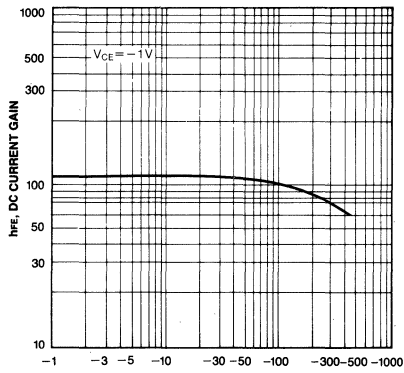
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ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

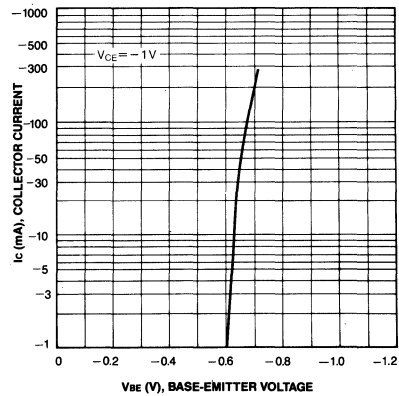
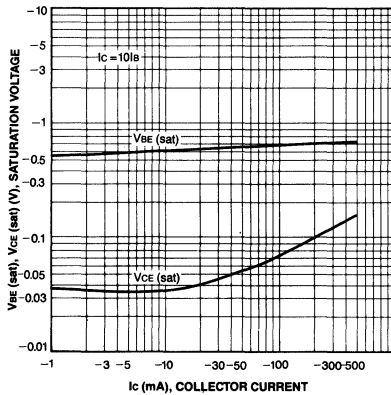
Characteristic	Symbol	Test Conditions	Min	Max	Unit
*Collector-Emitter Breakdown Voltage	BV_{CEO}	$I_C = -1\text{mA}, I_B = 0$	-60		V
KSP55			-80		V
KSP56			-4		V
Emitter-Base Breakdown Voltage	BV_{EBO}	$I_E = -100\mu\text{A}, I_C = 0$			V
Collector Cut-off Current	I_{CBO}	$V_{CB} = -60\text{V}, I_E = 0$		-0.1	μA
KSP55		$V_{CB} = -80\text{V}, I_E = 0$		-0.1	μA
KSP56		$V_{CE} = -60\text{V}, I_B = 0$		-0.1	μA
Collector Cut-off Current	I_{CEO}	$V_{CE} = -1\text{V}, I_C = -10\text{mA}$	50		
DC Current Gain	h_{FE}	$V_{CE} = -1\text{V}, I_C = -100\text{mA}$	50		
Collector-Emitter Saturation Voltage	$V_{CE}(\text{sat})$	$I_C = -100\text{mA}, I_B = -10\text{mA}$		-0.25	V
Base-Emitter On Voltage	$V_{BE}(\text{on})$	$V_{CE} = -1\text{V}, I_C = -100\text{mA}$		-1.2	V
Current Gain Bandwidth Product	f_T	$V_{CE} = -2\text{V}, I_C = -10\text{mA}$ $f = 100\text{MHz}$	50		MHz

*Pulse Test: $PW = 300\mu\text{s}$, Duty Cycle = 2%

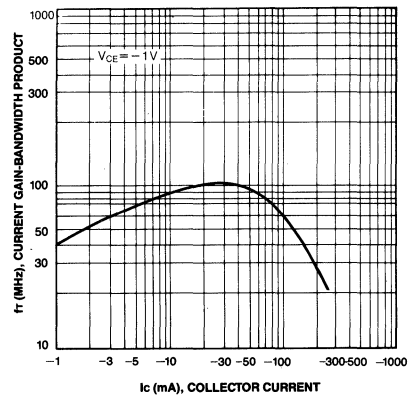
DC CURRENT GAIN



BASE-EMITTER ON VOLTAGE

COLLECTOR-EMITTER SATURATION VOLTAGE
BASE-EMITTER SATURATION VOLTAGE

CURRENT GAIN-BANDWIDTH PRODUCT

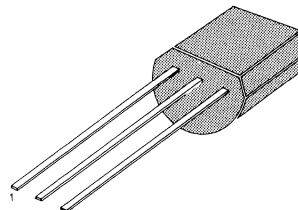


HIGH VOLTAGE TRANSISTOR

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Characteristic	Symbol	Rating	Unit
Collector-Base Voltage : KSP92	V_{CBO}	-300	V
: KSP93		-200	V
Collector-Emitter Voltage: KSP92	V_{CEO}	-300	V
: KSP93		-200	V
Emitter-Base Voltage	V_{EBO}	-5	V
Collector Current	I_C	-500	mA
Collector Dissipation ($T_a = 25^\circ\text{C}$)	P_C	625	mW
Derate above 25°C		5	mW/ $^\circ\text{C}$
Collector Dissipation ($T_c = 25^\circ\text{C}$)	P_C	1.5	W
Derate above 25°C		12	mW/ $^\circ\text{C}$
Junction Temperature	T_j	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55~150	$^\circ\text{C}$

TO-92



1. Emitter 2. Base 3. Collector

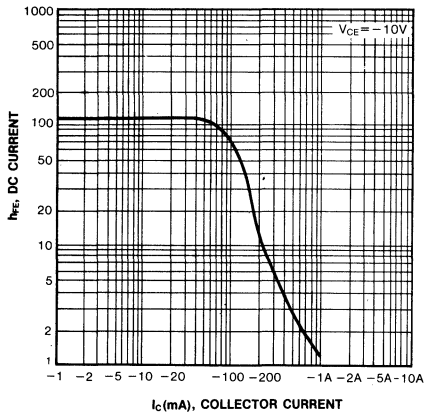
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ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

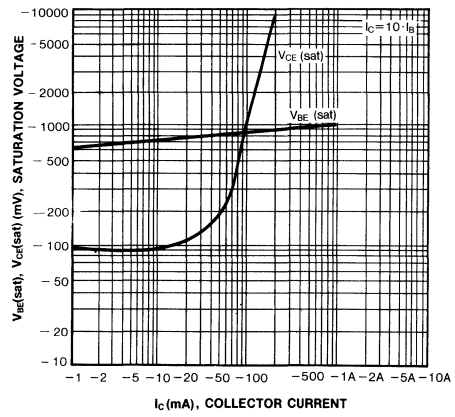
Characteristic	Symbol	Test Condition	Min	Max	Unit
Collector-Base Breakdown Voltage	BV_{CBO}	$I_C = -100\mu\text{A}, I_E = 0$			V
KSP92			-300		V
KSP93			-200		V
*Collector-Emitter Breakdown Voltage	BV_{CEO}	$I_C = -1\text{mA}, I_B = 0$			V
KSP92			-300		V
KSP93			-200		V
Emitter-Base Breakdown Voltage	BV_{EBO}	$I_E = -100\mu\text{A}, I_C = 0$		-5	V
Collector Cut-off Current	I_{CBO}	$V_{CB} = -200\text{V}, I_E = 0$		-0.25	μA
KSP92		$V_{CB} = -160\text{V}, I_E = 0$		-0.25	μA
KSP93		$V_{EB} = -3\text{V}, I_C = 0$		-0.10	μA
Emitter Cut-off Current	I_{EBO}	$V_{CE} = -10\text{V}, I_C = -1\text{mA}$	25		
*DC Current Gain	h_{FE}	$V_{CE} = -10\text{V}, I_C = -10\text{mA}$	40		
		$V_{CE} = -10\text{V}, I_C = -30\text{mA}$	25		
*Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = -20\text{mA}, I_B = -2\text{mA}$		-0.50	V
*Base-Emitter Saturation Voltage	$V_{BE(sat)}$	$I_C = -20\text{mA}, I_B = -2\text{mA}$		-0.90	V
Current Gain Bandwidth Product	f_T	$V_{CE} = -20\text{V}, I_C = -10\text{mA}$ $f = 100\text{MHz}$	50		MHz
Collector Base Capacitance	C_{CB}	$V_{CB} = -20\text{V}, I_E = 0$ $f = 1\text{MHz}$		6	pF
KSP92				8	pF
KSP93					

* Pulse Test: $PW = 300\mu\text{s}$, Duty Cycle = 2%

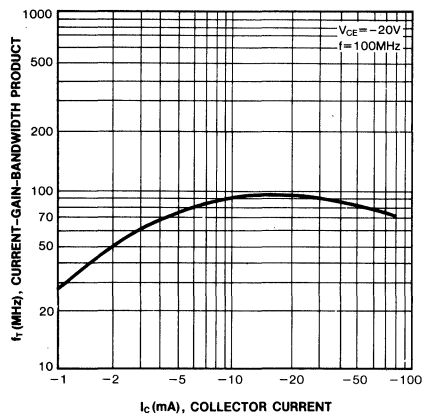
DC CURRENT GAIN



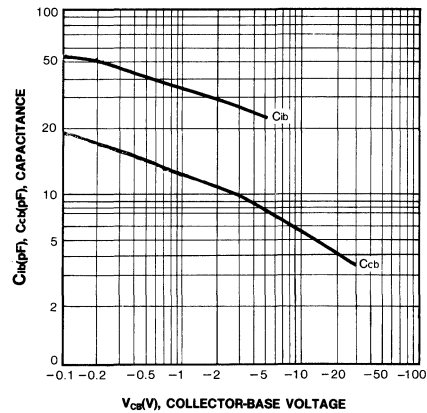
SATURATION VOLTAGES



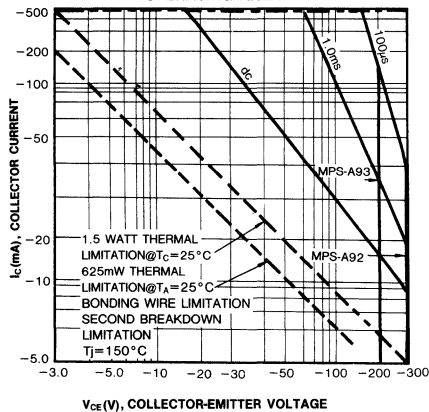
CURRENT-GAIN-BANDWIDTH PRODUCT



CAPACITANCE



ACTIVE-REGION SAFE OPERATING AREA



VHF/UHF TRANSISTOR

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

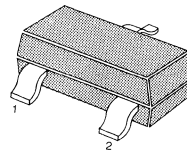
Characteristic	Symbol	Rating	Unit
Collector-Base Voltage	V_{CBO}	30	V
Collector-Emitter Voltage	V_{CEO}	25	V
Emitter-Base Voltage	V_{EBO}	3	V
Collector Dissipation	P_C	350	mW
Storage Temperature	T_{stg}	150	$^\circ\text{C}$
Thermal Resistance Junction to Ambient	$R_{th(j-a)}$	357	$^\circ\text{C/W}$

- Refer to KSP10/11 for graphs

ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

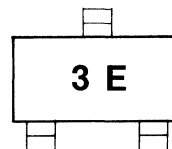
Characteristic	Symbol	Test Condition	Min	Max	Unit
Collector-Base Breakdown Voltage	BV_{CBO}	$I_C = 100\mu\text{A}$, $I_E = 0$	30		V
Collector-Emitter Breakdown Voltage	BV_{CEO}	$I_C = 1\text{mA}$, $I_B = 0$	25		V
Emitter-Base Breakdown Voltage	BV_{EBO}	$I_E = 10\mu\text{A}$, $I_C = 0$	3		V
Collector Cutoff Current	I_{CBO}	$V_{CB} = 25\text{V}$, $I_E = 0$		100	nA
Emitter Cutoff Current	I_{EBO}	$V_{BE} = 2\text{V}$, $I_C = 0$		100	nA
DC Current Gain	h_{FE}	$V_{CE} = 10\text{V}$, $I_C = 4\text{mA}$	60		
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 4\text{mA}$, $I_B = 0.4\text{mA}$		0.5	V
Base-Emitter On Voltage	V_{BE}	$V_{CE} = 10\text{V}$, $I_C = 4\text{mA}$		0.95	V
Current Gain-Bandwidth Product	f_T	$V_{CE} = 10\text{V}$, $I_C = 4\text{mA}$, $f = 100\text{MHz}$	650		MHz
Collector-Base Capacitance	C_{cb}	$V_{CB} = 10\text{V}$, $I_E = 0$, $f = 1\text{MHz}$		0.7	pF
Common-Base Feedback Capacitance	C_{rb}	$V_{CB} = 10\text{V}$, $I_E = 0$, $f = 1\text{MHz}$		0.65	pF
Collector Base Time Constant	$C_c \cdot r_{bb'}$	$V_{CB} = 10\text{V}$, $I_C = 4\text{mA}$, $f = 31.8\text{MHz}$		9	ps

SOT-23



1. Base 2. Emitter 3. Collector

Marking



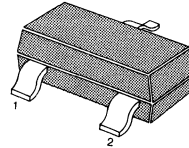
GENERAL PURPOSE TRANSISTOR

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Characteristic	Symbol	Rating	Unit
Collector-Base Voltage	V_{CBO}	75	V
Collector-Emitter Voltage	V_{CEO}	40	V
Emitter-Base Voltage	V_{EBO}	6	V
Collector Current	I_C	600	mA
Collector Dissipation	P_C	350	mW
Storage Temperature	T_{stg}	150	$^\circ\text{C}$

• Refer to KST2907 for graphs

SOT-23

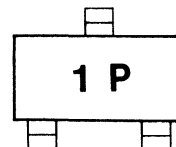


1. Base 2. Emitter 3. Collector

ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

Characteristic	Symbol	Test Condition	Min	Max	Unit
Collector-Base Breakdown Voltage	BV_{CBO}	$I_C = 10\mu\text{A}, I_E = 0$	75		V
Collector-Emitter Breakdown Voltage	BV_{CEO}	$I_C = 10\text{mA}, I_B = 0$	40		V
Emitter-Base Breakdown Voltage	BV_{EBO}	$I_E = 10\mu\text{A}, I_C = 0$	6		V
Collector Cutoff Current	I_{CBO}	$V_{CB} = 60\text{V}, I_E = 0$		0.01	μA
*DC Current Gain	h_{FE}	$V_{CE} = 10\text{V}, I_C = 0.1\text{mA}$	35		
		$V_{CE} = 10\text{V}, I_C = 1\text{mA}$	50		
		$V_{CE} = 10\text{V}, I_C = 10\text{mA}$	75		
		$V_{CE} = 10\text{V}, I_C = 150\text{mA}$	100	300	
		$V_{CE} = 10\text{V}, I_C = 500\text{mA}$	40		
*Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 150\text{mA}, I_B = 15\text{mA}$		0.3	V
		$I_C = 500\text{mA}, I_B = 50\text{mA}$		1.0	V
*Base-Emitter Saturation Voltage	$V_{BE(sat)}$	$I_C = 150\text{mA}, I_B = 15\text{mA}$	0.6	1.2	V
		$I_C = 500\text{mA}, I_B = 50\text{mA}$		2.0	V
Current Gain-Bandwidth Product	f_T	$I_C = 20\text{mA}, V_{CE} = 20\text{V}$ $f = 100\text{MHz}$	300		MHz
Collector-Base Capacitance	C_{ob}	$V_{CB} = 10\text{V}, I_E = 0$ $f = 1\text{MHz}$		8	pF
Noise Figure	NF	$I_C = 100\mu\text{A}, V_{CE} = 10\text{V}$ $R_S = 1\text{K}\Omega, f = 1\text{KHz}$	4	4	dB
Turn On Time	t_{on}	$V_{CC} = 30\text{V}, I_C = 150\text{mA}$ $V_{BE} = 0.5\text{V}, I_{B1} = 15\text{mA}$		35	ns
Turn Off Time	t_{off}	$V_{CC} = 30\text{V}, I_C = 150\text{mA}$ $I_{B1} = I_{B2} = 15\text{mA}$		285	ns

*Pulse test: Pulse Width=300 μs , Duty Cycle=2%



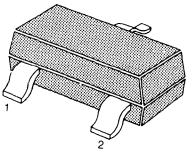
LOW NOISE TRANSISTOR

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Characteristic	Symbol	Rating	Unit
Collector-Base Voltage	V _{CBO}	60	V
Collector-Emitter Voltage	V _{CEO}	60	V
Emitter-Base Voltage	V _{EBO}	6	V
Collector Current	I _C	50	mA
Collector Dissipation	P _C	350	mW
Storage Temperature	T _{stg}	150	°C

• Refer to KST5088 for graphs

SOT-23

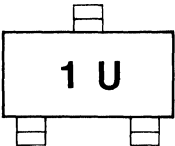


1. Base 2. Emitter 3. Collector

ELECTRICAL CHARACTERISTICS (T_a = 25°C)

Characteristic	Symbol	Test Condition	Min	Max	Unit
Collector-Base Breakdown Voltage	BV _{CBO}	I _C = 10μA, I _E = 0	60		V
Collector-Emitter Breakdown Voltage	BV _{CEO}	I _C = 10mA, I _B = 0	60		V
Emitter-Base Breakdown Voltage	BV _{EBO}	I _E = 10μA, I _C = 0	5		V
Collector Cutoff Current	I _{CBO}	V _{CB} = 45V, I _E = 0		10	nA
Emitter Cutoff Current	I _{EBO}	V _{EB} = 5V, I _C = 0		10	nA
DC Current Gain	h _{FE}	V _{CE} = 5V, I _C = 1mA	250		
		V _{CE} = 5V, I _C = 10μA		800	
Collector-Emitter Saturation Voltage	V _{CE} (sat)	I _C = 1mA, I _B = 0.1mA		0.35	V
Base-Emitter On Voltage	V _{BE} (on)	I _C = 1mA, V _{CE} = 5V		0.95	V
Output Capacitance	C _{ob}	V _{CB} = 5.0V, I _E = 0		6	pF
		f = 1MHz,			
Noise Figure	NF	I _C = 10μA, V _{CE} = 5V		3	dB
		R _S = 10KΩ, f = 1KHz			

Marking



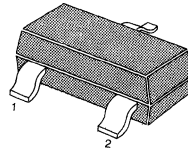
GENERAL PURPOSE TRANSISTOR

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Characteristic	Symbol	Rating	Unit
Collector-Base Voltage	V_{CBO}	-60	V
Collector-Emitter Voltage	V_{CEO}	-60	V
Emitter-Base Voltage	V_{EBO}	-5	V
Collector Current	I_C	-600	mA
Collector Dissipation	P_C	350	mW
Storage Temperature	T_{stg}	150	$^\circ\text{C}$

• Refer to KST2907 for graphs

SOT-23



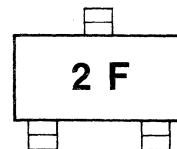
1. Base 2. Emitter 3. Collector

ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

Characteristic	Symbol	Test Condition	Min	Max	Unit
Collector-Base Breakdown Voltage	BV_{CBO}	$I_C = -10\mu\text{A}, I_E = 0$	-60		V
*Collector-Emitter Breakdown Voltage	BV_{CEO}	$I_C = -10\text{mA}, I_B = 0$	-60		V
Emitter-Base Breakdown Voltage	BV_{EBO}	$I_E = -10\mu\text{A}, I_C = 0$	-5		V
Collector Cutoff Current	I_{CBO}	$V_{CB} = -50\text{V}, I_E = 0$		-0.01	μA
DC Current Gain	h_{FE}	$V_{CE} = -10\text{V}, I_E = -0.1\text{mA}$	75		
		$V_{CE} = -10\text{V}, I_C = -1.0\text{mA}$	100		
		$V_{CE} = -10\text{V}, I_C = -10\text{mA}$	100		
		* $V_{CE} = -10\text{V}, I_C = -150\text{mA}$	100	300	
		* $V_{CE} = -10\text{V}, I_C = -500\text{mA}$	50		
*Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = -150\text{mA}, I_B = -15\text{mA}$		-0.4	V
		$I_C = -500\text{mA}, I_B = -50\text{mA}$		-1.6	V
*Base-Emitter Saturation Voltage	$V_{BE(sat)}$	$I_C = -150\text{mA}, I_B = -15\text{mA}$		-1.3	V
		$I_C = -500\text{mA}, I_B = -50\text{mA}$		-2.6	V
Current Gain-Bandwidth Product	f_T	$I_C = -50\text{mA}, V_{CE} = -20\text{V}$ $f = 100\text{MHz}$	200		MHz
Output Capacitance	C_{ob}	$V_{CB} = -10\text{V}, I_E = 0$ $f = 1.0\text{MHz}$		8	pF
Turn On Time	t_{on}	$V_{CC} = -30\text{V}, I_C = -150\text{mA}$ $I_{B1} = -15\text{mA}$		50	ns
Turn Off Time	t_{off}	$V_{CC} = -6\text{V}, I_C = -150\text{mA}$ $I_{B1} = I_{B2} = -15\text{mA}$		110	ns

*Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$

Marking

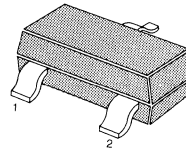


GENERAL PURPOSE TRANSISTOR

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Characteristic	Symbol	Rating	Unit
Collector-Base Voltage	V_{CBO}	-60	V
Collector-Emitter Voltage	V_{CEO}	-40	V
Emitter-Base Voltage	V_{EBO}	-6	V
Collector Current	I_C	-200	mA
Collector Dissipation	P_C	350	mW
Storage Temperature	T_{stg}	150	$^\circ\text{C}$

SOT-23



1. Base 2. Emitter 3. Collector

2

ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

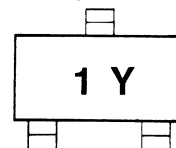
Characteristic	Symbol	Test Condition	Min	Max	Unit
Collector-Base Breakdown Voltage	BV_{CBO}	$I_C = 10\mu\text{A}, I_E = 0$	60		V
*Collector-Emitter Breakdown Voltage	BV_{CEO}	$I_C = 1\text{mA}, I_B = 0$	40		V
Emitter-Base Breakdown Voltage	BV_{EBO}	$I_E = 10\mu\text{A}, I_C = 0$	6		V
Collector Cut-off Current	I_{CEX}	$V_{CE} = 30\text{V}, V_{EB} = 3\text{V}$		50	nA
*DC Current Gain	h_{FE}	$V_{CE} = 1\text{V}, I_C = 0.1\text{mA}$	20		
	KST3903		40		
	KST3904	$V_{CE} = 1\text{V}, I_C = 1\text{mA}$	35		
	KST3903		70		
	KST3904	$V_{CE} = 1\text{V}, I_C = 10\text{mA}$	50	150	
	KST3903		100	300	
	KST3904	$V_{CE} = 1\text{V}, I_C = 50\text{mA}$	30		
	KST3903		60		
	KST3904	$V_{CE} = 1\text{V}, I_C = 100\text{mA}$	15		
	KST3903		30		
*Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 10\text{mA}, I_B = 1\text{mA}$		0.2	V
		$I_C = 50\text{mA}, I_B = 5\text{mA}$		0.3	V
*Base-Emitter Saturation Voltage	$V_{BE(sat)}$	$I_C = 10\text{mA}, I_B = 1\text{mA}$	0.65	0.85	V
		$I_C = 50\text{mA}, I_B = 5\text{mA}$		0.95	V
Output Capacitance	C_{OB}	$V_{CB} = 5\text{V}, I_E = 0, f = 1\text{MHz}$		4	pF
Current Gain Bandwidth Product	f_T	$V_{CE} = 20\text{V}, I_C = 10\text{mA}$			
	KST3903	$f = 100\text{MHz}$	250		MHz
	KST3904		300		MHz
Noise Figures	N_F	$I_C = 100\mu\text{A}, V_{CE} = 5\text{V}, R_S = 1\text{K}\Omega$			
	KST3903	$f = 10\text{Hz to } 15.7\text{KHz}$		6	dB
	KST3904			5	dB
Turn On Time	t_{ON}	$V_{CC} = 3\text{V}, V_{BE} = 0.5\text{V}$		70	ns
		$I_C = 10\text{mA}, I_{B1} = 1\text{mA}$			
Turn Off Time	t_{OFF}	$V_{CC} = 3\text{V}, I_C = 10\text{mA}$			
	KST3903	$I_{B1} = I_{B2} = 1\text{mA}$		225	ns
	KST3904			250	ns

* Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$

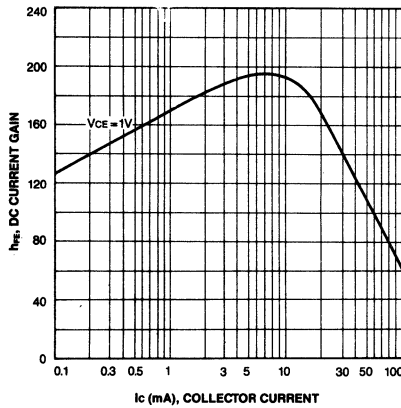
MARKING CODE

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MARK	1Y	1A

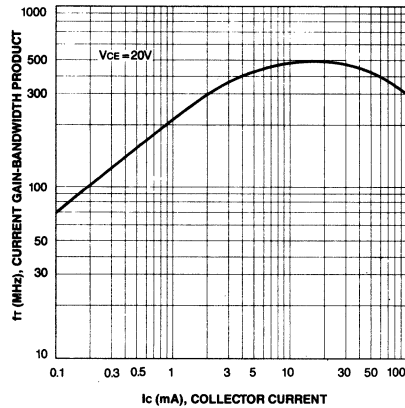
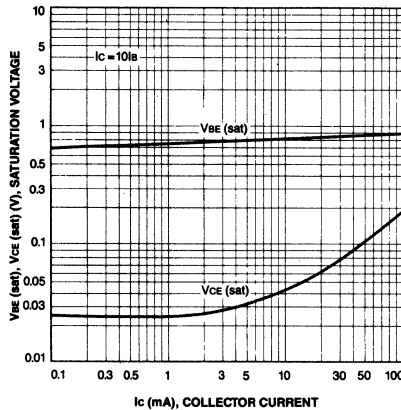
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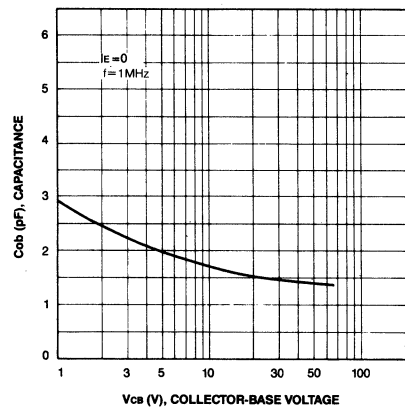
DC CURRENT GAIN



CURRENT GAIN-BANDWIDTH PRODUCT

BASE-EMITTER SATURATION VOLTAGE
COLLECTOR-EMITTER SATURATION VOLTAGE

OUTPUT CAPACITANCE

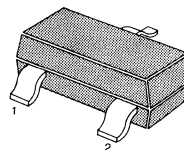


GENERAL PURPOSE TRANSISTOR

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Characteristic	Symbol	Rating	Unit
Collector-Base Voltage	V_{CBO}	-40	V
Collector-Emitter Voltage	V_{CEO}	-40	V
Emitter-Base Voltage	V_{EBO}	-5	V
Collector Current	I_C	-200	mA
Collector Dissipation	P_C	350	mW
Storage Temperature	T_{stg}	150	$^\circ\text{C}$

SOT-23



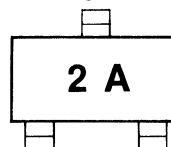
1. Base 2. Emitter 3. Collector

ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

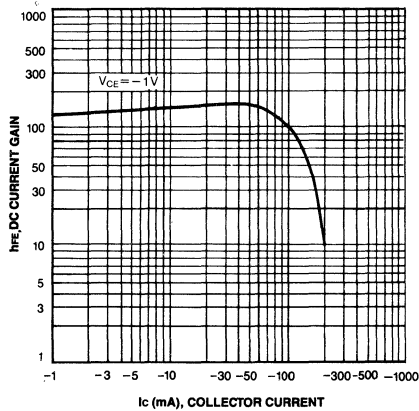
Characteristic	Symbol	Test Condition	Min	Max	Unit
Collector-Base Breakdown Voltage	BV_{CBO}	$I_C = -10\mu\text{A}$, $I_E = 0$	-40		V
*Collector-Emitter Breakdown Voltage	BV_{CEO}	$I_C = -1.0\text{mA}$, $I_B = 0$	-40		V
Emitter-Base Breakdown Voltage	BV_{EBO}	$I_E = -10\mu\text{A}$, $I_C = 0$	-5		V
Collector Cutoff Current	I_{CEX}	$V_{CE} = -30\text{V}$, $V_{EB} = -3\text{V}$		-50	nA
*DC Current Gain	h_{FE}	$V_{CE} = -1\text{V}$, $I_C = -0.1\text{mA}$	60		
		$V_{CE} = -1\text{V}$, $I_C = -1\text{mA}$	80		
		$V_{CE} = -1\text{V}$, $I_C = -10\text{mA}$	100	300	
		$V_{CE} = -1\text{V}$, $I_C = -50\text{mA}$	60		
		$V_{CE} = -1\text{V}$, $I_C = -100\text{mA}$	30		
*Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = -10\text{mA}$, $I_B = -1\text{mA}$		-0.25	V
		$I_C = -50\text{mA}$, $I_B = -5.0\text{mA}$		-0.4	V
*Base-Emitter Saturation Voltage	$V_{BE(sat)}$	$I_C = -10\text{mA}$, $I_B = -1.0\text{mA}$	-0.65	-0.85	V
		$I_C = -50\text{mA}$, $I_B = -5.0\text{mA}$		-0.95	V
Current Gain-Bandwidth Product	f_T	$I_C = -10\text{mA}$, $V_{CE} = -20\text{V}$ $f = 100\text{MHz}$	250		MHz
Output Capacitance	C_{ob}	$V_{CB} = -5\text{V}$, $I_E = 0$ $f = 1.0\text{MHz}$		4.5	pF
Noise Figure	NF	$I_C = -100\mu\text{A}$, $V_{CE} = -5\text{V}$ $R_S = 1\text{K}\Omega$ $f = 10\text{Hz to } 15.7\text{KHz}$		4	dB
Turn On Time	t_{on}	$V_{CC} = -3\text{V}$, $V_{BE} = -0.5\text{V}$ $I_C = -10\text{mA}$, $I_{B1} = -1\text{mA}$		70	ns
Turn Off Time	t_{off}	$V_{CC} = -3\text{V}$, $I_C = -10\text{mA}$ $I_{B1} = I_{B2} = -1\text{mA}$		300	ns

*Pulse Test: Pulse Width=300 μs , Duty Cycle=2%

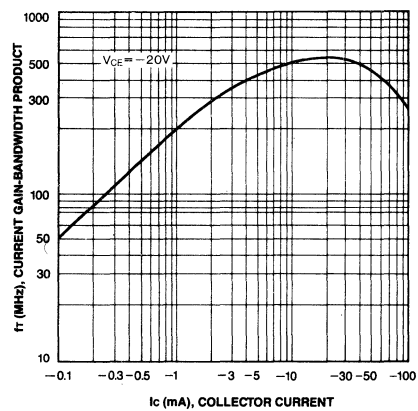
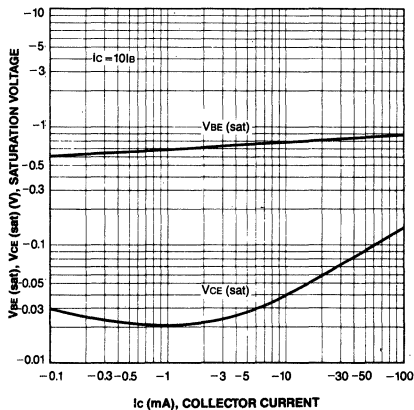
Marking



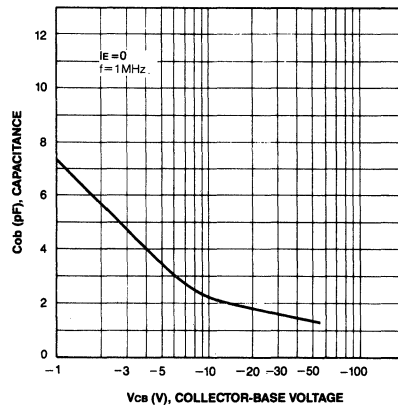
DC CURRENT GAIN



CURRENT GAIN-BANDWIDTH PRODUCT

BASE-EMITTER SATURATION VOLTAGE
COLLECTOR-EMITTER SATURATION VOLTAGE

OUTPUT CAPACITANCE

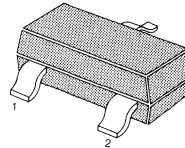


HIGH VOLTAGE TRANSISTOR

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Characteristic	Symbol	Rating	Unit
Collector Base Voltage	V_{CBO}	300	V
KST42		200	V
KST43			
Collector-Emitter Voltage	V_{CEO}	300	V
KST42		200	V
KST43			
Emitter-Base Voltage	V_{EBO}	6	V
Collector Current	I_C	500	mA
Collector Dissipation	P_C	350	mW
Storage Temperature	T_{STG}	150	$^\circ\text{C}$
Thermal Resistance Junction to Ambient	$R_{TH(j-a)}$	357	$^\circ\text{C/W}$

SOT-23



1. Base 2. Emitter 3. Collector

2

ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

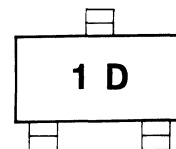
Characteristic	Symbol	Test Condition	Min	Max	Unit
Collector-Base Breakdown Voltage	BV_{CBO}	$I_C = 100\mu\text{A}, I_E = 0$	300		V
KST42			200		V
KST43					
*Collector-Emitter Breakdown Voltage	BV_{CEO}	$I_C = 1\text{mA}, I_B = 0$	300		V
KST42			200		V
KST43					
Emitter-Base Breakdown Voltage	BV_{EBO}	$I_E = 100\mu\text{A}, I_C = 0$	6		V
Collector Cut-off Current	I_{CBO}	$V_{CE} = 200\text{V}, I_E = 0$		0.1	μA
Emitter Cut-off Current	I_{EBO}	$V_{CE} = 5\text{V}, I_C = 0$		0.1	μA
*DC Current Gain	h_{FE}	$V_{CE} = 10\text{V}, I_C = 1\text{mA}$	25		
		$V_{CE} = 10\text{V}, I_C = 10\text{mA}$	40		
		$V_{CE} = 10\text{V}, I_C = 30\text{mA}$	40		
*Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 20\text{mA}, I_B = 2\text{mA}$		0.5	V
*Base-Emitter Saturation Voltage	$V_{BE(sat)}$	$I_C = 20\text{mA}, I_B = 2\text{mA}$		0.9	V
Collector-Base Capacitance	C_{CB}	$V_{CB} = 20\text{V}, I_E = 0$		3	pF
KST42		$f = 1\text{MHz}$		4	pF
KST43					
Current Gain Bandwidth Product	f_T	$V_{CE} = 20\text{V}, I_C = 10\text{mA}$	50		MHz
		$f = 100\text{MHz}$			

* Pulse Test: $PW = 300\mu\text{s}$, Duty Cycle = 2%

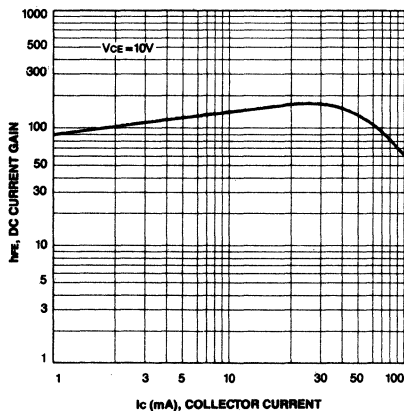
Marking

MARKING CODE

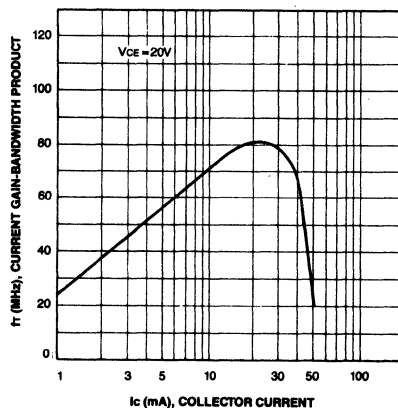
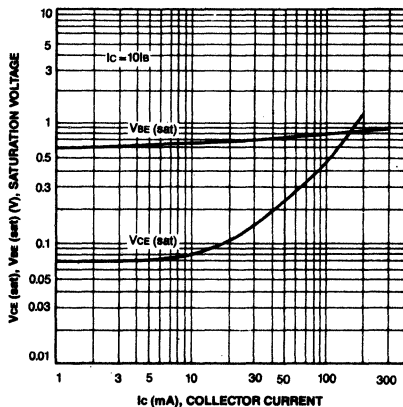
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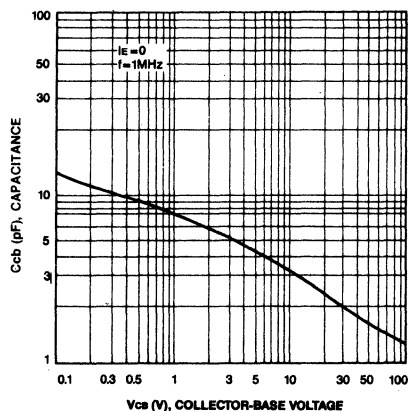
DC CURRENT GAIN



CURRENT GAIN-BANDWIDTH PRODUCT

COLLECTOR-EMITTER SATURATION VOLTAGE
BASE-EMITTER SATURATION VOLTAGE

COLLECTOR-BASE CAPACITANCE

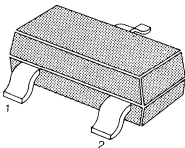


SWITCHING TRANSISTOR

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Rating	Unit
Collector-Base Voltage	V _{CBO}	60	V
Collector-Emitter Voltage	V _{CEO}	40	V
Emitter-Base Voltage	V _{EBO}	6	V
Collector Current	I _C	600	mA
Collector Dissipation	P _C	350	mW
Storage Temperature	T _{stg}	150	°C

SOT-23



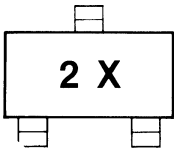
1. Base 2. Emitter 3. Collector

ELECTRICAL CHARACTERISTICS (T_a=25°C)

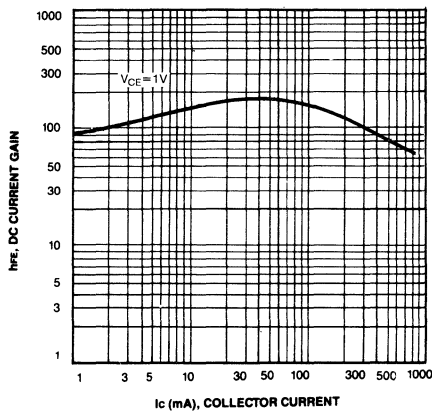
Characteristic	Symbol	Test Condition	Min	Max	Unit
Collector-Base Breakdown Voltage	BV _{CBO}	I _C =100μA, I _E =0	60		V
* Collector-Emitter Breakdown Voltage	BV _{CEO}	I _C =1.0mA, I _B =0	40		V
Emitter-Base Breakdown Voltage	BV _{EBO}	I _E =100μA, I _C =0	6		V
Base Cutoff Current	I _{BEV}	V _{CE} =35V, V _{EB} =0.4V		100	nA
Collector Cutoff Current	I _{CEX}	V _{CE} =35V, V _{BE} =0.4V		100	nA
* DC Current Gain	h _{FE}	V _{CE} =1V, I _C =0.1mA	20		
		V _{CE} =1V, I _C =1mA	40		
		V _{CE} =1V, I _C =10mA	80		
		V _{CE} =1V, I _C =150mA	100	300	
		V _{CE} =2V, I _C =500mA	40		
* Collector-Emitter Saturation Voltage	V _{CE} (sat)	I _C =150mA, I _B =15mA		0.4	V
		I _C =500mA, I _B =50mA		0.75	V
* Base-Emitter Saturation Voltage	V _{BE} (sat)	I _C =150mA, I _B =15mA	0.75	0.95	V
		I _C =500mA, I _B =50mA		1.2	V
Current Gain-Bandwidth Product	f _T	I _C =20mA, V _{CE} =10V f=100MHz	250		MHz
Collector Base Capacitance	C _{cb}	V _{CB} =5V, I _E =0 f=100K Hz		6.5	pF
Turn On Time	t _{on}	V _{CC} =30V, V _{BE} =2V I _C =150mA, I _{B1} =15mA		35	ns
Turn Off Time	t _{off}	V _{CC} =30V, I _C =150mA I _{B1} =I _{B2} =15mA		255	ns

*Pulse Test: Pulse Width=300μs, Duty Cycle=2%

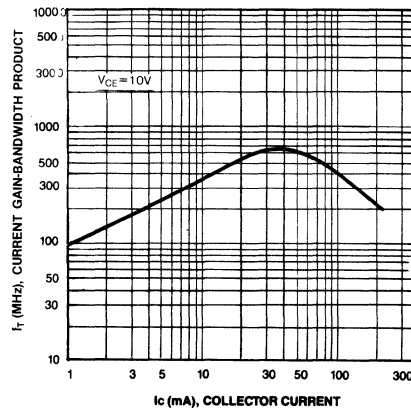
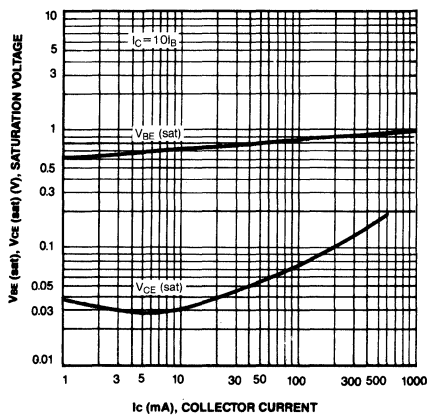
Marking



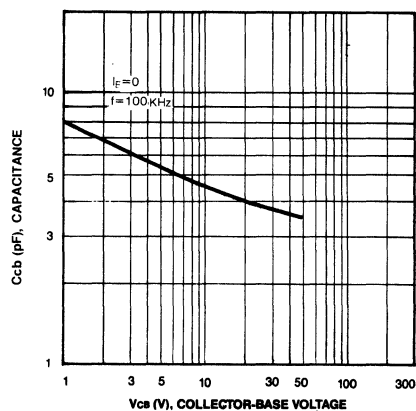
DC CURRENT GAIN



CURRENT GAIN-BANDWIDTH PRODUCT

COLLECTOR-EMITTER SATURATION VOLTAGE
BASE-EMITTER SATURATION VOLTAGE

COLLECTOR-BASE CAPACITANCE

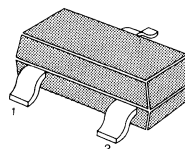


SWITCHING TRANSISTOR

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Characteristic	Symbol	Rating	Unit
Collector-Base Voltage	V_{CBO}	-40	V
Collector-Emitter Voltage	V_{CEO}	-40	V
Emitter-Base Voltage	V_{EBO}	-5	V
Collector Current	I_C	-600	mA
Collector Dissipation	P_C	350	mW
Storage Temperature	T_{stg}	150	$^\circ\text{C}$

SOT-23



1: Base 2: Emitter 3: Collector

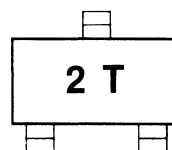
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ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

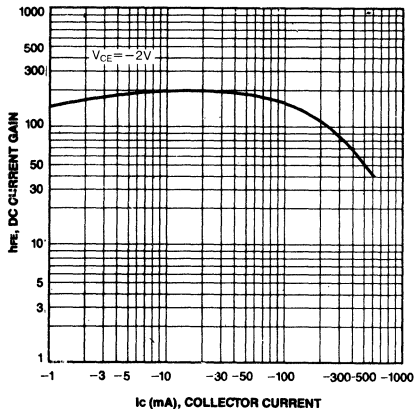
Characteristic	Symbol	Test Condition	Min	Max	Unit
Collector-Base Breakdown Voltage	BV_{CBO}	$I_C = -0.1\text{mA}, I_E = 0$	-40		V
*Collector-Emitter Breakdown Voltage	BV_{CEO}	$I_C = -1.0\text{mA}, I_B = 0$	-40		V
Emitter-Base Breakdown Voltage	BV_{EBO}	$I_E = -0.1\text{mA}, I_C = 0$	-5		V
Base Cutoff Current	I_{BEV}	$V_{CE} = -35\text{V}, V_{BE} = -0.4\text{V}$		-0.1	μA
Collector Cutoff Current	I_{CEX}	$V_{CE} = -35\text{V}, V_{BE} = -0.4\text{V}$		-0.1	μA
DC Current Gain	h_{FE}	$V_{CE} = -1\text{V}, I_C = -0.1\text{mA}$	30		
		$V_{CE} = -1\text{V}, I_C = -1.0\text{mA}$	60		
		$V_{CE} = -1\text{V}, I_C = -10\text{mA}$	100		
		* $V_{CE} = -2\text{V}, I_C = -150\text{mA}$	100	300	
		* $V_{CE} = -2\text{V}, I_C = -500\text{mA}$	20		
*Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = -150\text{mA}, I_B = -15\text{mA}$		-0.4	V
		$I_C = -500\text{mA}, I_B = -50\text{mA}$		-0.75	V
*Base-Emitter Saturation Voltage	$V_{BE(sat)}$	$I_C = -150\text{mA}, I_B = -15\text{mA}$	-0.75	-0.95	V
		$I_C = -500\text{mA}, I_B = -50\text{mA}$		-1.3	V
Current Gain-Bandwidth Product	f_T	$I_C = -20\text{mA}, V_{CE} = -10\text{V}$ $f = 100\text{MHz}$	200		MHz
Collector-Base Capacitance	C_{cb}	$V_{CB} = -10\text{V}, I_E = 0$ $f = 140\text{kHz}$		8.5	pF
Turn On Time	t_{on}	$V_{CC} = -30\text{V}, V_{BE} = -2\text{V}$ $I_C = -150\text{mA}, I_{B1} = -15\text{mA}$		35	ns
Turn Off Time	t_{off}	$V_{CC} = -30\text{V}, I_C = -150\text{mA}$ $I_{B1} = I_{B2} = -15\text{mA}$		255	ns

*Pulse Test: Pulse Width=300 μs , Duty Cycle=2%

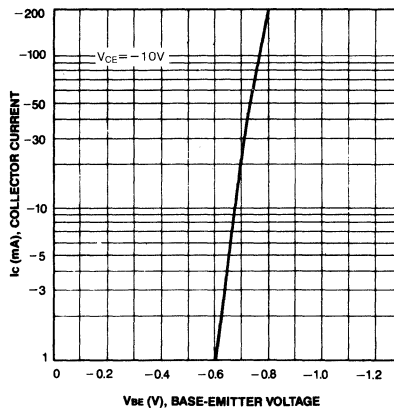
Marking



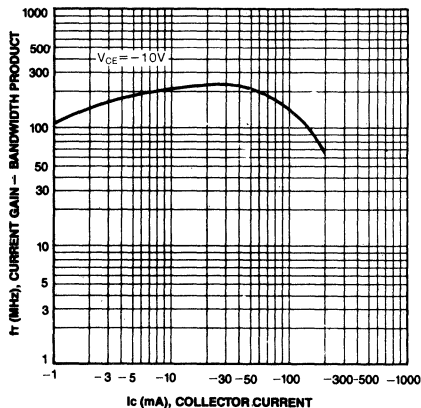
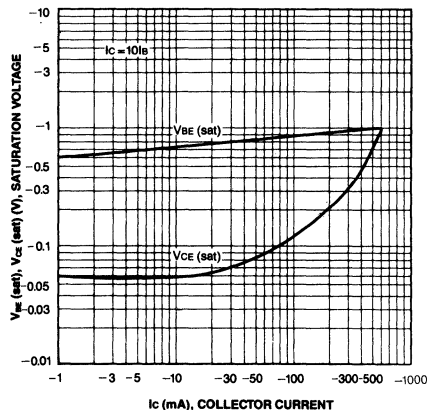
DC CURRENT GAIN



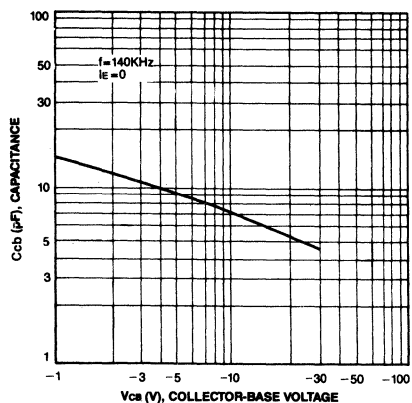
BASE-EMITTER ON VOLTAGE



CURRENT GAIN-BANDWIDTH PRODUCT

BASE-EMITTER SATURATION VOLTAGE
COLLECTOR-EMITTER SATURATION VOLTAGE

COLLECTOR-BASE CAPACITANCE

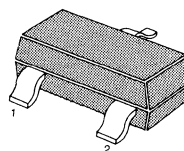


HIGH VOLTAGE TRANSISTOR

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Characteristic	Symbol	Rating	Unit
Collector-Base Voltage	V_{CBO}	-160	V
Collector-Emitter Voltage	V_{CEO}	-150	V
Emitter-Base Voltage	V_{EBO}	-5	V
Collector Current	I_C	-500	mA
Collector Dissipation	P_C	350	mW
Storage Temperature	T_{stg}	150	$^\circ\text{C}$

SOT-23

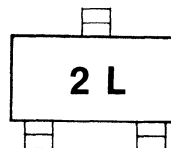


1. Base 2. Emitter 3. Collector

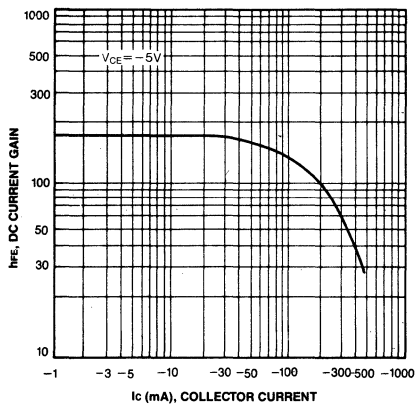
ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

Characteristic	Symbol	Test Condition	Min	Max	Unit
Collector-Base Breakdown Voltage	BV_{CBO}	$I_C = -100\mu\text{A}$, $I_E = 0$	-160		V
Collector-Emitter Breakdown Voltage	BV_{CEO}	$I_C = -1.0\text{mA}$, $I_B = 0$	-150		V
Emitter-Base Breakdown Voltage	BV_{EBO}	$I_E = -10\mu\text{A}$, $I_C = 0$	-5		V
Collector Cutoff Current	I_{CBO}	$V_{CB} = -100\text{V}$, $I_E = 0$		-50	nA
DC Current Gain	h_{FE}	$V_{CE} = -5\text{V}$, $I_C = -1.0\text{mA}$	50		
		$V_{CE} = -5\text{V}$, $I_C = -10\text{mA}$	60	240	
		$V_{CE} = -5\text{V}$, $I_C = -50\text{mA}$	50		
		$I_C = -10\text{mA}$, $I_B = -1.0\text{mA}$		-0.2	V
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = -50\text{mA}$, $I_B = -5\text{mA}$		-0.5	V
		$I_C = -10\text{mA}$, $I_B = -1.0\text{mA}$		-1.0	V
		$I_C = -50\text{mA}$, $I_B = -5\text{mA}$		-1.0	V
Base-Emitter Saturation Voltage	$V_{BE(sat)}$	$I_C = -10\text{mA}$, $V_{CE} = -10\text{V}$	100	300	MHz
		$f = 100\text{MHz}$			
Current Gain-Bandwidth Product	f_T	$I_C = -10\text{mA}$, $V_{CE} = -10\text{V}$			
Output Capacitance	C_{ob}	$V_{CB} = -10\text{V}$, $I_E = 0$		6.0	pF
		$f = 1.0\text{MHz}$			
Noise Figure	NF	$V_{CE} = -5\text{V}$, $I_C = -200\mu\text{A}$		8.0	dB
		$R_S = 10\text{K}\Omega$			
		$f = 10\text{Hz to } 15.7\text{KHz}$			

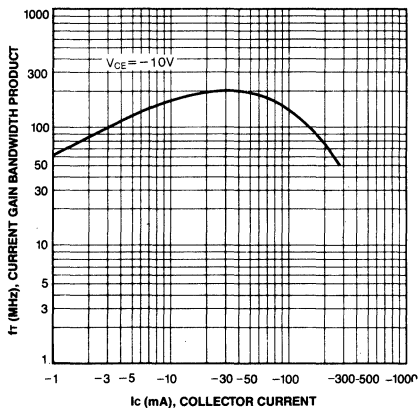
Marking



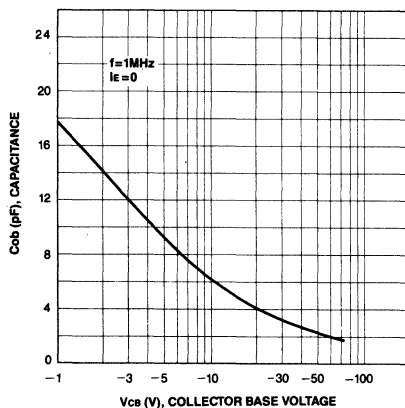
DC CURRENT GAIN



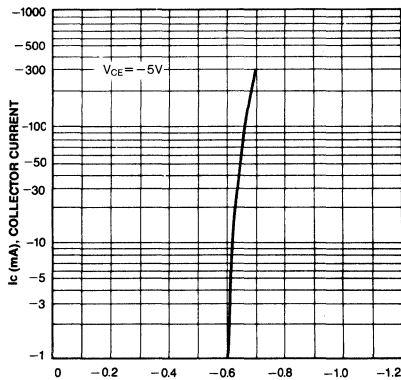
CURRENT GAIN-BANDWIDTH PRODUCT



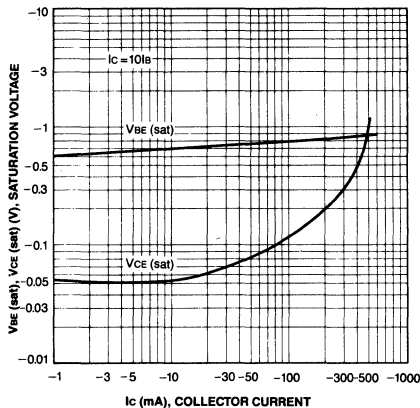
OUTPUT CAPACITANCE



BASE-EMITTER ON VOLTAGE



VBE (V), BASE-EMITTER VOLTAGE

BASE-EMITTER SATURATION VOLTAGE
COLLECTOR-EMITTER SATURATION VOLTAGE

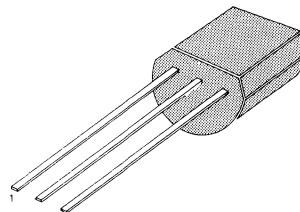
AMPLIFIER TRANSISTOR

- Collector-Emitter Voltage: $V_{CE0} = 160V$
- Collector Dissipation: $P_C(\max) = 625mW$

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ C$)

Characteristic	Symbol	Rating	Unit
Collector-Base Voltage	V_{CBO}	180	V
Collector-Emitter Voltage	V_{CEO}	160	V
Emitter-Base Voltage	V_{EBO}	6	V
Collector Current	I_C	600	mA
Collector Dissipation	P_C	625	mW
Junction Temperature	T_J	150	$^\circ C$
Storage Temperature	T_{stg}	-55 ~ 150	$^\circ C$

TO-92



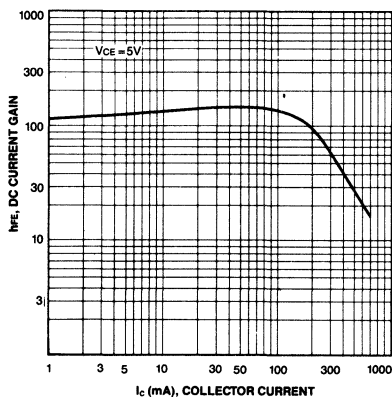
1. Emitter 2. Base 3. Collector

ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ C$)

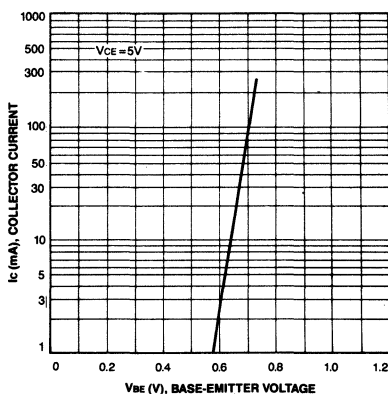
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Collector-Base Breakdown Voltage	BV_{CBO}	$I_C = 100\mu A, I_E = 0$	180			V
*Collector-Emitter Breakdown Voltage	BV_{CEO}	$I_C = 1mA, I_B = 0$	160			V
Emitter-Base Breakdown Voltage	BV_{EBO}	$I_E = 10\mu A, I_C = 0$	6			V
Collector Cut-off Current	I_{CBO}	$V_{CB} = 120V, I_E = 0$			50	nA
Emitter Cut-off Current	I_{EBO}	$V_{BE} = 4V, I_C = 0$			50	nA
*DC Current Gain	h_{FE}	$I_C = 1mA, V_{CE} = 5V$	80			
		$I_C = 10mA, V_{CE} = 5V$	80		250	
		$I_C = 50mA, V_{CE} = 5V$	30			
*Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 10mA, I_B = 1mA$			0.15	V
		$I_C = 50mA, I_B = 5mA$			0.2	V
*Base-Emitter Saturation Voltage	$V_{BE(sat)}$	$I_C = 10mA, I_B = 1mA$			1	V
		$I_C = 50mA, I_B = 5mA$			1	V
Current Gain Bandwidth Product	f_T	$I_C = 10mA, V_{CE} = 10V$ $f = 100MHz$	100		300	MHz
Output Capacitance	C_{ob}	$V_{CB} = 10V, I_E = 0$ $f = 1MHz$			6	pF
Noise Figure	NF	$I_C = 250\mu A, V_{CE} = 5V$ $R_S = 1K\Omega$ $f = 10Hz$ to $15.7KHz$			8	dB

* Pulse Test: Pulse Width = $300\mu S$, Duty Cycle = 2%

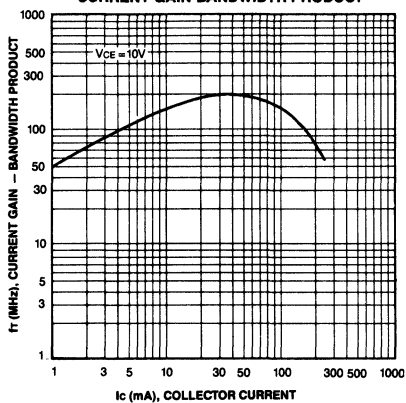
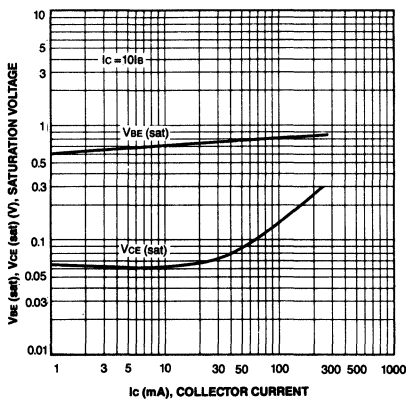
DC CURRENT GAIN



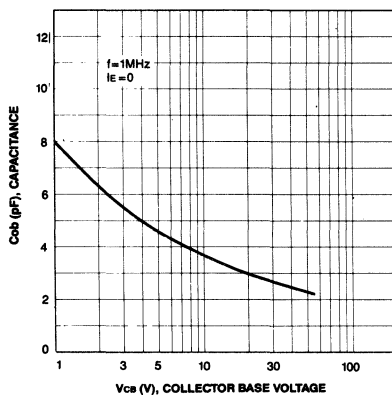
BASE-EMITTER ON VOLTAGE



CURRENT GAIN-BANDWIDTH PRODUCT

BASE-EMITTER SATURATION VOLTAGE
COLLECTOR-EMITTER SATURATION VOLTAGE

OUTPUT CAPACITANCE

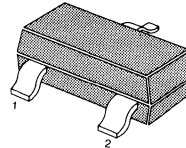


HIGH VOLTAGE TRANSISTOR

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Characteristic	Symbol	Rating	Unit
Collector Base Voltage	V_{CBO}		
KST92		- 300	V
KST93		- 200	V
Collector-Emitter Voltage	V_{CEO}		
KST92		- 300	V
KST93		- 200	V
Emitter-Base Voltage	V_{EBO}	- 5	V
Collector Current	I_C	- 500	mA
Collector Dissipation	P_C	350	mW
Storage Temperature	T_{STG}	150	$^\circ\text{C}$
Thermal Resistance Junction to Ambient	$R_{TH(j-a)}$	357	$^\circ\text{C/W}$

SOT-23



1. Base 2. Emitter 3. Collector

2

• Refer to KSP92/93 for graphs

ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

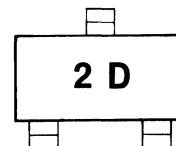
Characteristic	Symbol	Test Condition	Min	Max	Unit
Collector-Base Breakdown Voltage	BV_{CBO}	$I_C = -100\mu\text{A}, I_E = 0$			
KST92			- 300		V
KST93			- 200		V
*Collector-Emitter Breakdown Voltage	BV_{CEO}	$I_C = -1\text{mA}, I_B = 0$			
KST92			- 300		V
KST93			- 200		V
Emitter-Base Breakdown Voltage	BV_{EBO}	$I_E = -100\mu\text{A}, I_C = 0$		- 5	V
Collector Cut-off Current	I_{CBO}				
KST92		$V_{CB} = -200\text{V}, I_E = 0$		- 0.25	μA
KST93		$V_{CB} = -160\text{V}, I_E = 0$		- 0.25	μA
Emitter Cut-off Current	I_{EBO}	$V_{CE} = -3\text{V}, I_C = 0$		- 0.1	μA
*DC Current Gain	h_{FE}	$V_{CE} = -10\text{V}, I_C = -1\text{mA}$	25		
		$V_{CE} = -10\text{V}, I_C = -10\text{mA}$	40		
		$V_{CE} = -10\text{V}, I_C = -30\text{mA}$	25		
*Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = -20\text{mA}, I_B = -2\text{mA}$		- 0.5	V
*Base-Emitter Saturation Voltage	$V_{BE(sat)}$	$I_C = -20\text{mA}, I_B = -2\text{mA}$		- 0.9	V
Collector-Base Capacitance	C_{CB}	$V_{CB} = -20\text{V}, I_E = 0$			
KST92		$f = 1\text{MHz}$		6	pF
KST93				8	pF
Current Gain Bandwidth Product	f_T	$V_{CE} = -20\text{V}, I_C = -10\text{mA}$	50		MHz
		$f = 100\text{MHz}$			

* Pulse Test: $PW = 300\mu\text{s}$, Duty Cycle = 2%

MARKING CODE

TYPE	KST92	KST93
MARK	2D	2E

Marking



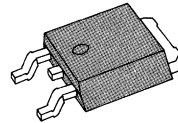
D-PACK FOR SURFACE MOUNT APPLICATIONS

- High DC Current Gain
- Built-in a Damper Diode at E-C
- Lead Formed for Surface Mount Applications (No Suffix)
- Straight Lead (I.PACK, "I" Suffix)
- Electrically Similar to Popular TIP112

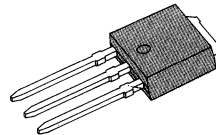
ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Characteristic	Symbol	Rating	Unit
Collector Base Voltage	V_{CBO}	100	V
Collector Emitter Voltage	V_{CEO}	100	V
Emitter Base Voltage	V_{EBO}	5	V
Collector Current (DC)	I_C	2	A
Collector Current (Pulse)	I_C	4	A
Base Current	I_B	50	A
Collector Dissipation ($T_c = 25^\circ\text{C}$)	P_c	20	W
Collector Dissipation ($T_a = 25^\circ\text{C}$)	P_c	1.75	W
Junction Temperature	T_j	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-65 ~ 150	$^\circ\text{C}$

D-PAK



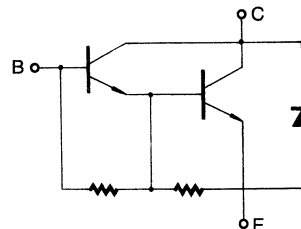
I-PAK

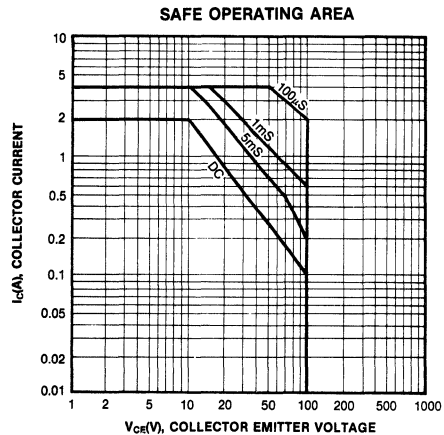
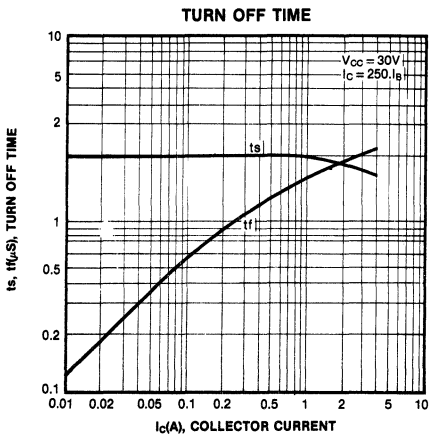
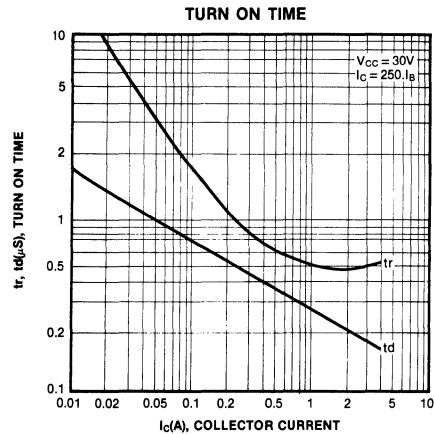
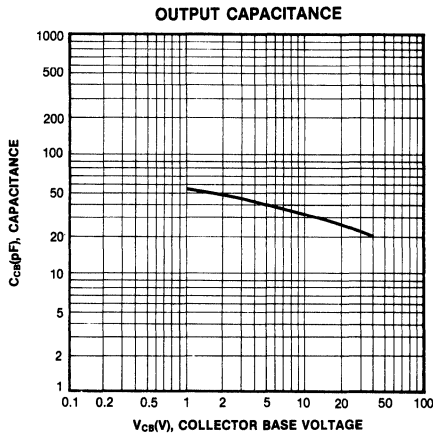
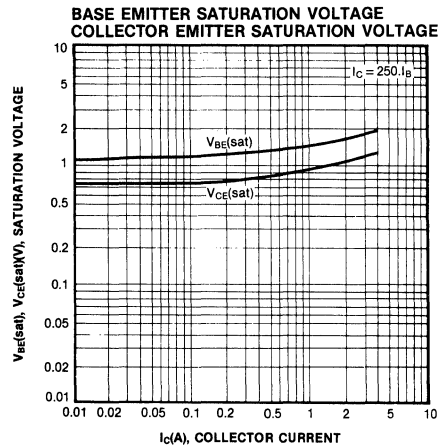
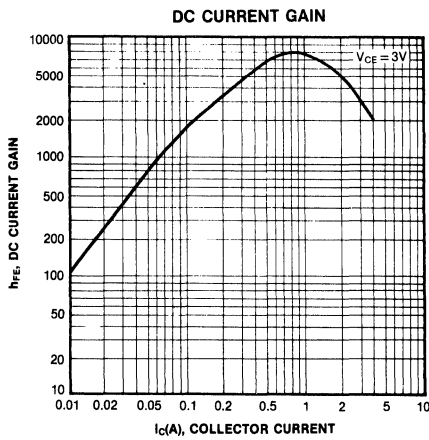


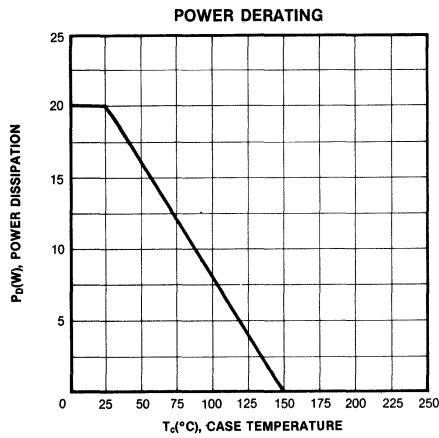
ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

Characteristic	Symbol	Test Condition	Min	Max	Unit
*Collector Emitter Sustaining Voltage	$V_{CEO(sus)}$	$I_C = 30\text{mA}, I_B = 0$	100		V
Collector Cutoff Current	I_{CEO}	$V_{CE} = 50\text{V}, I_B = 0$		20	μA
Collector Cutoff Current	I_{CBO}	$V_{CB} = 100\text{V}, I_E = 0$		20	μA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = 5\text{V}, I_C = 0$		2	mA
*DC Current Gain	h_{FE}	$V_{CE} = 3\text{V}, I_C = 0.5\text{A}$	500		
		$V_{CE} = 3\text{V}, I_C = 2\text{A}$	1000	12K	
		$V_{CE} = 3\text{V}, I_C = 4\text{A}$	200		
*Collector Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 2\text{A}, I_B = 8\text{mA}$		2	V
		$I_C = 4\text{A}, I_B = 40\text{mA}$		3	V
*Base Emitter Saturation Voltage	$V_{BE(sat)}$	$I_C = 4\text{A}, I_B = 40\text{mA}$		4	V
*Base Emitter On Voltage	$V_{BE(on)}$	$V_{CE} = 3\text{A}, I_C = 2\text{A}$		2.8	V
Current Gain Bandwidth Product	f_T	$V_{CE} = 10\text{V}, I_C = 0.75\text{A}$	25		MHz
		$f = 1\text{MHz}$			
Output Capacitance	C_{OB}	$V_{CB} = 10\text{V}, I_E = 0$		100	pF
		$f = 0.1\text{MHz}$			

* Pulse Test: $PW \leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$







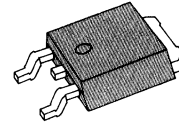
D-PACK FOR SURFACE MOUNT APPLICATIONS

- High DC Current Gain
- Built-in a Damper Diode at E-C
- Lead Formed for Surface Mount Applications (No Suffix)
- Straight Lead (I.PACK, "— I " Suffix)
- Electrically Similar to Popular TIP117

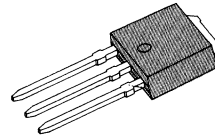
ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Characteristic	Symbol	Rating	Unit
Collector Base Voltage	V_{CB0}	- 100	V
Collector Emitter Voltage	V_{CEO}	- 100	V
Emitter Base Voltage	V_{EBO}	- 5	V
Collector Current (DC)	I_C	- 2	A
Collector Current (Pulse)	I_C	- 4	A
Base Current	I_B	- 50	A
Collector Dissipation ($T_c = 25^\circ\text{C}$)	P_c	20	W
Collector Dissipation ($T_a = 25^\circ\text{C}$)	P_c	1.75	W
Junction Temperature	T_j	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	- 65 ~ 150	$^\circ\text{C}$

D-PAK



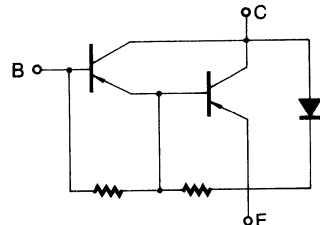
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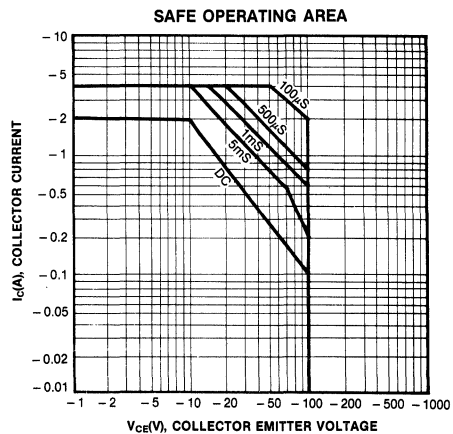
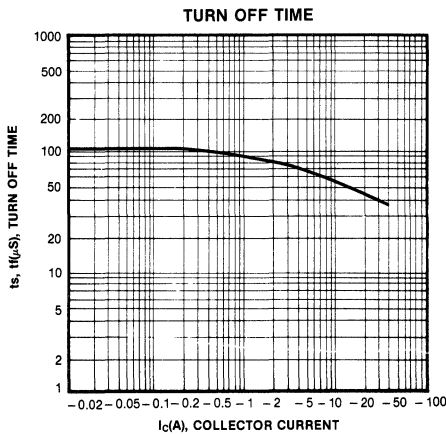
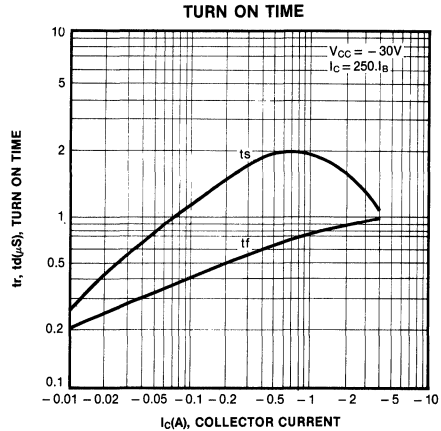
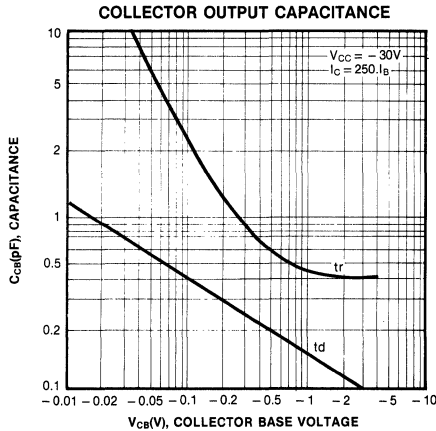
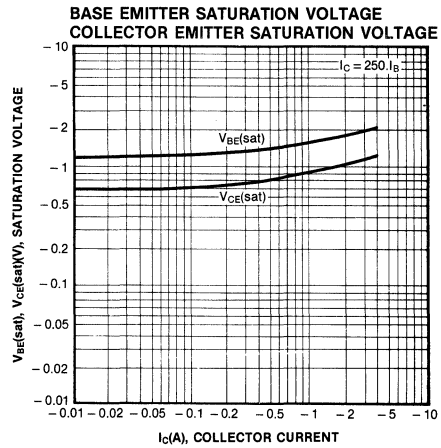
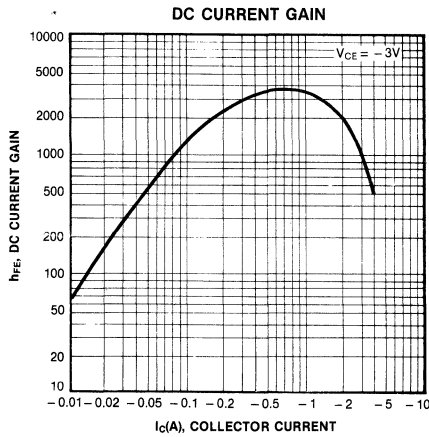


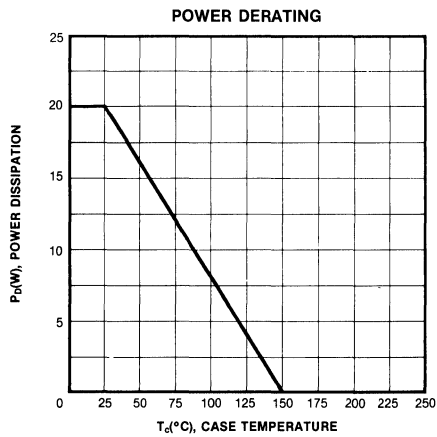
ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

Characteristic	Symbol	Test Condition	Min	Max	Unit
*Collector Emitter Sustaining Voltage	$V_{CEO(sus)}$	$I_C = -30\text{mA}, I_B = 0$	- 100		V
Collector Cutoff Current	I_{CEO}	$V_{CE} = -50\text{V}, I_B = 0$		- 20	μA
Collector Cutoff Current	I_{CBO}	$V_{CB} = -100\text{V}, I_E = 0$		- 20	μA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = -5\text{V}, I_C = 0$		- 2	mA
*DC Current Gain	h_{FE}	$V_{CE} = -3\text{V}, I_C = -0.5\text{A}$	500		
		$V_{CE} = -3\text{V}, I_C = -2\text{A}$	1000	12K	
		$V_{CE} = -3\text{V}, I_C = -4\text{A}$	200		
*Collector Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = -2\text{A}, I_B = -8\text{mA}$		- 2	V
		$I_C = -4\text{A}, I_B = -40\text{mA}$		- 3	V
*Base Emitter Saturation Voltage	$V_{BE(sat)}$	$I_C = -4\text{A}, I_B = -40\text{mA}$		- 4	V
*Base Emitter On Voltage	$V_{BE(on)}$	$V_{CE} = -3\text{A}, I_C = -2\text{A}$		- 2.8	V
Current Gain Bandwidth Product	f_T	$V_{CE} = -10\text{V}, I_C = -0.75\text{A}$ $f = 1\text{MHz}$	25		MHz
Output Capacitance	C_{OB}	$V_{CB} = -10\text{V}, I_E = 0$ $f = 0.1\text{MHz}$		200	pF

* Pulse Test: $PW \leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$







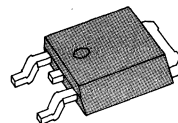
D-PACK FOR SURFACE MOUNT APPLICATIONS

- High DC Current Gain
- Built-in a Damper Diode at E-C
- Lead Formed for Surface Mount Applications (No Suffix)
- Straight Lead (I.PACK, "— I " Suffix)
- Electrically Similar to Popular TIP122

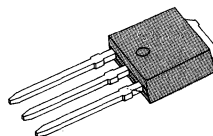
ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Characteristic	Symbol	Rating	Unit
Collector Base Voltage	V_{CBO}	100	V
Collector Emitter Voltage	V_{CEO}	100	V
Emitter Base Voltage	V_{EBO}	5	V
Collector Current (DC)	I_C	8	A
Collector Current (Pulse)	I_C	16	A
Base Current	I_B	120	A
Collector Dissipation ($T_c = 25^\circ\text{C}$)	P_c	20	W
Collector Dissipation ($T_a = 25^\circ\text{C}$)	P_c	1.75	W
Junction Temperature	T_j	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-65 ~ 150	$^\circ\text{C}$

D-PAK



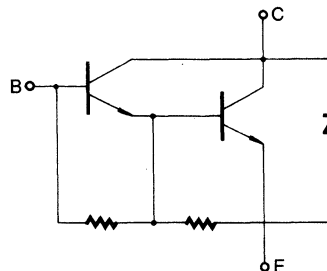
I-PAK

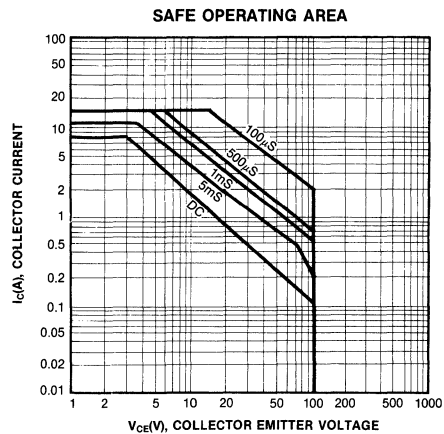
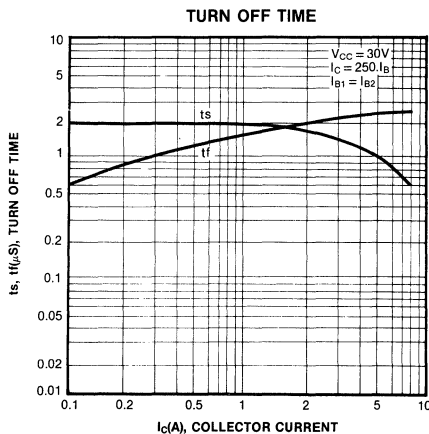
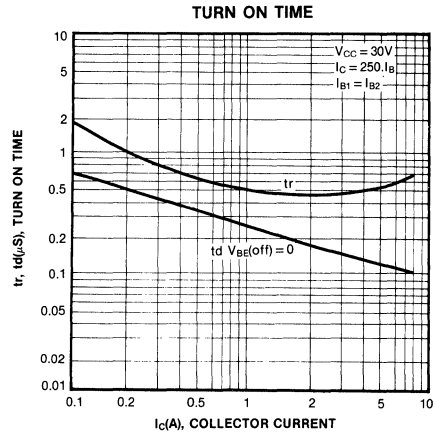
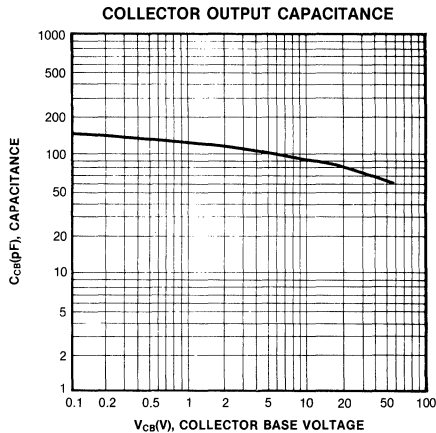
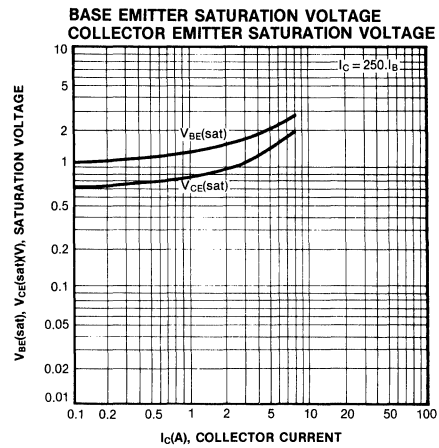
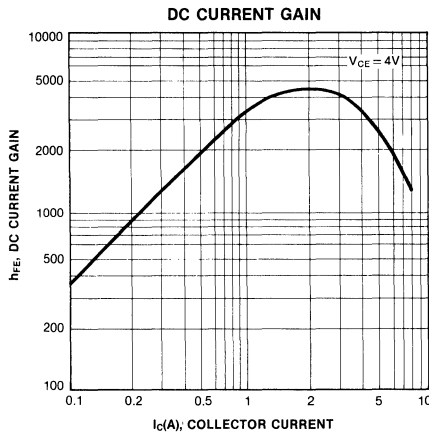


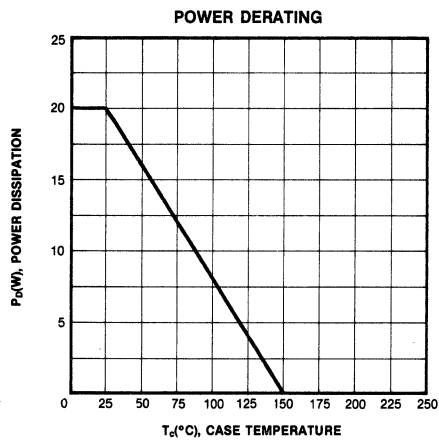
ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

Characteristic	Symbol	Test Condition	Min	Max	Unit
*Collector Emitter Sustaining Voltage	$V_{CE(sus)}$	$I_C = 30\text{mA}$, $I_B = 0$	100		V
Collector Cutoff Current	I_{CEO}	$V_{CE} = 50\text{V}$, $I_B = 0$		10	μA
Collector Cutoff Current	I_{CBO}	$V_{CB} = 100\text{V}$, $I_E = 0$		10	μA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = 5\text{V}$, $I_C = 0$		2	mA
*DC Current Gain	h_{FE}	$V_{CE} = 4\text{V}$, $I_C = 4\text{A}$	1000	12K	
		$V_{CE} = 4\text{V}$, $I_C = 8\text{A}$	100		
*Collector Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 4\text{A}$, $I_B = 16\text{mA}$		2	V
		$I_C = 8\text{A}$, $I_B = 80\text{mA}$		4	V
*Base Emitter Saturation Voltage	$V_{BE(sat)}$	$I_C = 8\text{A}$, $I_B = 80\text{mA}$		4.5	V
*Base Emitter On Voltage	$V_{BE(on)}$	$V_{CE} = 4\text{A}$, $I_C = 4\text{A}$		2.8	V
Output Capacitance	C_{OB}	$V_{CB} = 10\text{V}$, $I_E = 0$ $f = 0.1\text{MHz}$		200	pF

* Pulse Test: $PW \leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$







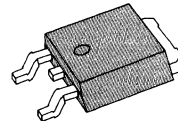
D-PACK FOR SURFACE MOUNT APPLICATIONS

- High DC Current Gain
- Built-in a Damper Diode at E-C
- Lead Formed for Surface Mount Applications (No Suffix)
- Straight Lead (I.PACK, "— I " Suffix)
- Electrically Similar to Popular TIP127

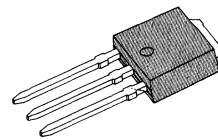
ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Characteristic	Symbol	Rating	Unit
Collector Base Voltage	V_{CBO}	- 100	V
Collector Emitter Voltage	V_{CEO}	- 100	V
Emitter Base Voltage	V_{EBO}	- 5	V
Collector Current (DC)	I_C	- 8	A
Collector Current (Pulse)	I_C	- 16	A
Base Current	I_B	- 120	A
Collector Dissipation ($T_c = 25^\circ\text{C}$)	P_c	20	W
Collector Dissipation ($T_a = 25^\circ\text{C}$)	P_c	1.75	W
Junction Temperature	T_j	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	- 65 ~ 150	$^\circ\text{C}$

D-PAK



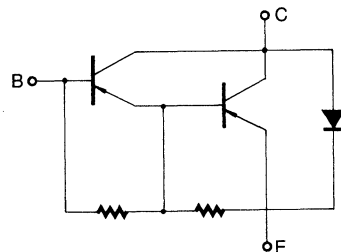
I-PAK

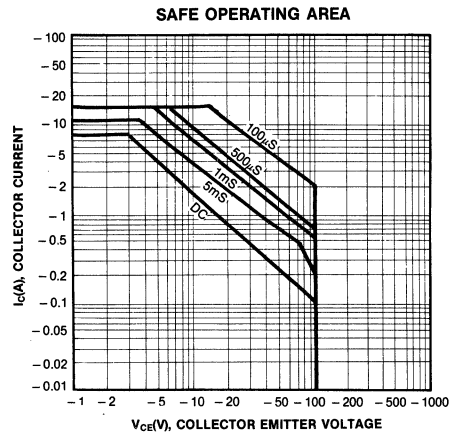
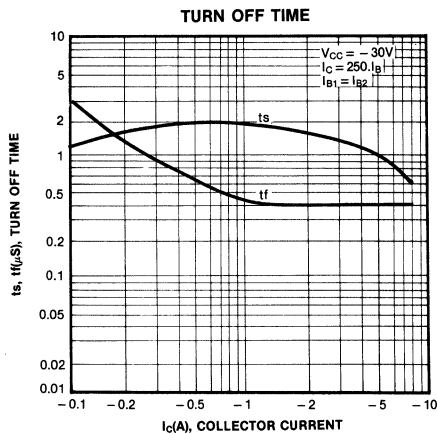
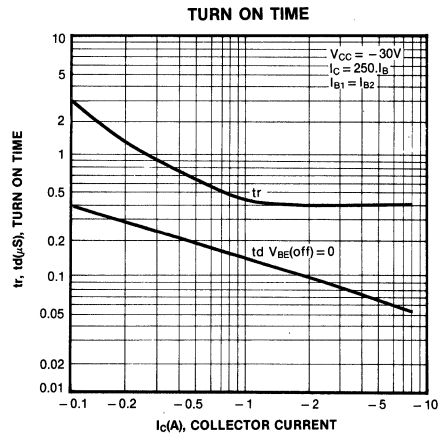
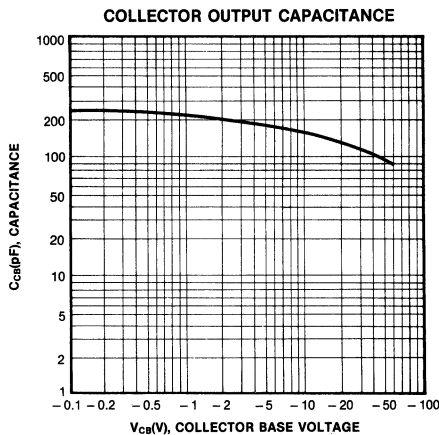
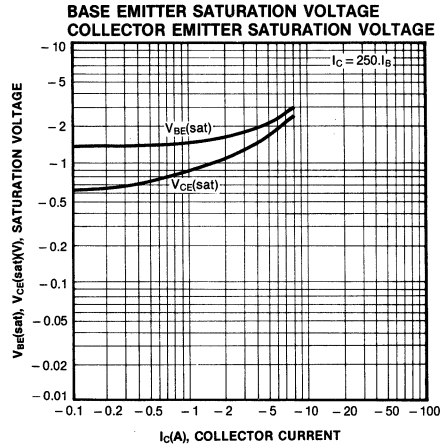
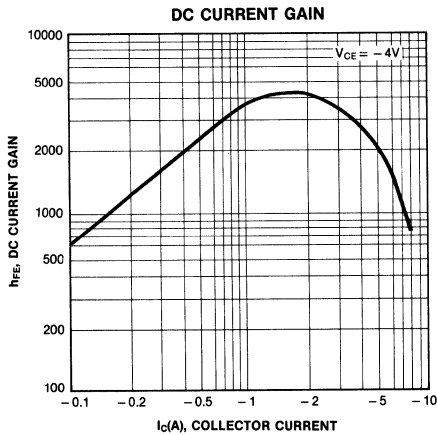


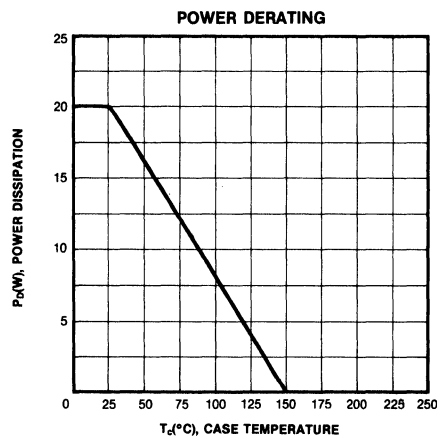
ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

Characteristic	Symbol	Test Condition	Min	Max	Unit
*Collector Emitter Sustaining Voltage	$V_{CE(sus)}$	$I_C = -30\text{mA}, I_B = 0$	- 100		V
Collector Cutoff Current	I_{CEO}	$V_{CE} = -50\text{V}, I_B = 0$		- 10	μA
Collector Cutoff Current	I_{CBO}	$V_{CB} = -100\text{V}, I_E = 0$		- 10	μA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = -5\text{V}, I_C = 0$		- 2	mA
*DC Current Gain	h_{FE}	$V_{CE} = -4\text{V}, I_C = -4\text{A}$	1000	12K	
		$V_{CE} = -4\text{V}, I_C = -8\text{A}$	100		
*Collector Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = -4\text{A}, I_B = -16\text{mA}$		- 2	V
		$I_C = -8\text{A}, I_B = -80\text{mA}$		- 4	V
*Base Emitter Saturation Voltage	$V_{BE(sat)}$	$I_C = -8\text{A}, I_B = -80\text{mA}$		- 4.5	V
*Base Emitter On Voltage	$V_{BE(on)}$	$V_{CE} = -4\text{A}, I_C = -4\text{A}$		- 2.8	V
Output Capacitance	C_{OB}	$V_{CB} = -10\text{V}, I_E = 0$ $f = 0.1\text{MHz}$		300	pF

* Pulse Test: $PW \leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$







2

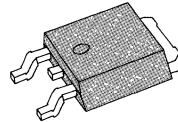
**GENERAL PURPOSE AMPLIFIER
LOW SPEED SWITCHING APPLICATIONS
D-PACK FOR SURFACE MOUNT
APPLICATIONS**

- Lead Formed for Surface Mount Applications (No Suffix)
- Straight Lead (I.PACK, "— I " Suffix)
- Electrically Similar to Popular MJE2955
- DC Current Gain Specified to 10A
- High Current Gain-Bandwidth Product:
 $f_T = 2\text{MHz (MIN)}$, $I_C = -500\text{mA}$

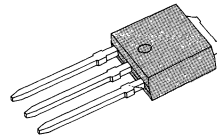
ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Characteristic	Symbol	Rating	Unit
Collector Base Voltage	V_{CBO}	- 70	V
Collector Emitter Voltage	V_{CEO}	- 60	V
Emitter Base Voltage	V_{EBO}	- 5	V
Collector Current	I_C	- 10	A
Base Current	I_B	- 6	A
Collector Dissipation ($T_c = 25^\circ\text{C}$)	P_c	20	W
Collector Dissipation ($T_a = 25^\circ\text{C}$)	P_c	1.75	W
Junction Temperature	T_j	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	- 55 ~ 150	$^\circ\text{C}$

D-PAK



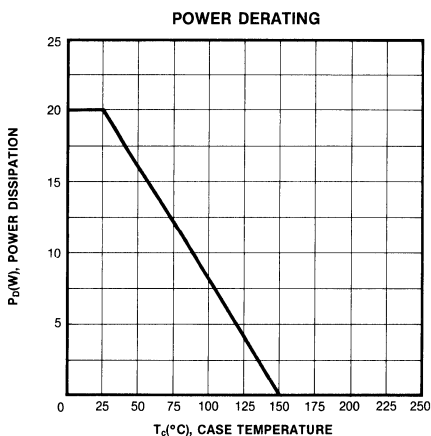
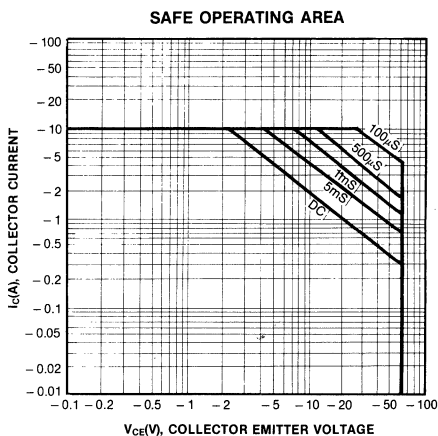
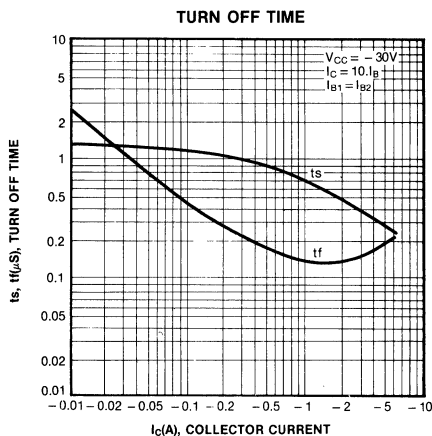
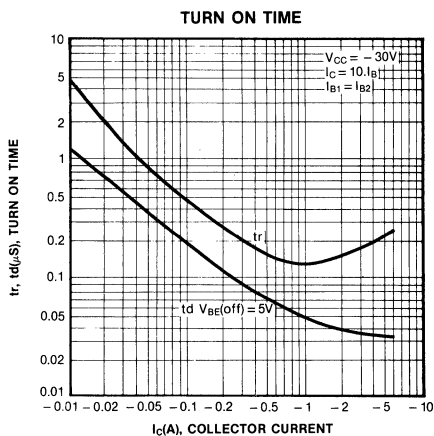
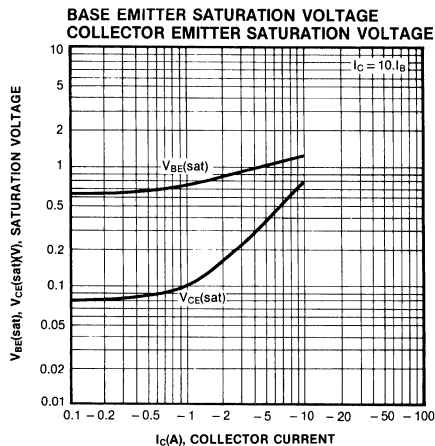
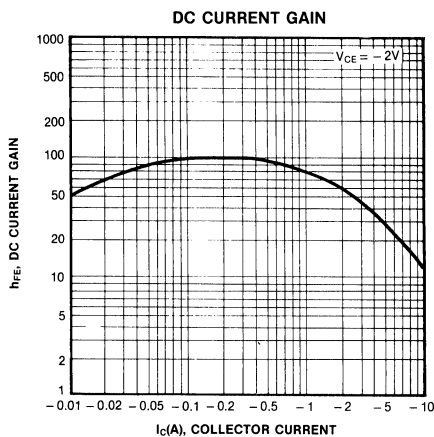
I-PAK



ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

Characteristic	Symbol	Test Condition	Min	Max	Unit
*Collector Emitter Sustaining Voltage	$V_{CE(sus)}$	$I_C = -30\text{mA}$, $I_B = 0$	- 60		V
Collector Cutoff Current	I_{CEO}	$V_{CE} = -30\text{V}$, $I_B = 0$		- 50	μA
Collector Cutoff Current	I_{CBO}	$V_{CB} = -70\text{V}$, $I_E = 0$		- 2	mA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = -5\text{V}$, $I_C = 0$		- 0.5	mA
*DC Current Gain	h_{FE}	$V_{CE} = -4\text{V}$, $I_C = -4\text{A}$	20	100	
		$V_{CE} = -4\text{V}$, $I_C = -10\text{A}$	5		
*Collector Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = -4\text{A}$, $I_B = -0.4\text{A}$		- 1.1	V
		$I_C = -10\text{A}$, $I_B = -3.3\text{A}$		- 8	V
*Base Emitter On Voltage	$V_{BE(on)}$	$V_{CE} = -4\text{A}$, $I_C = -4\text{A}$		- 1.8	V
Current Gain Bandwidth Product	f_T	$V_{CE} = -10\text{V}$, $I_C = -500\text{mA}$ $f = 500\text{KHz}$	2		MHz

* Pulse Test: $PW \leq 300\mu\text{S}$, Duty Cycle $\leq 2\%$



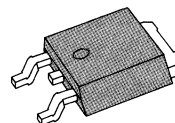
**GENERAL PURPOSE AMPLIFIER
LOW SPEED SWITCHING APPLICATIONS
D-PACK FOR SURFACE MOUNT
APPLICATIONS**

- Load Formed for Surface Mount Application(No Suffix)
- Straight Lead (I.PACK, "— I " Suffix)
- Electrically Similar to Popular TIP29 and TIP29C

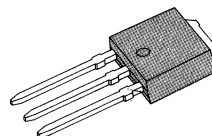
ABSOLUTE MAXIMUM RATING($T_a=25^\circ\text{C}$)

Characteristic	Symbol	Rating	Unit
Collector Base Voltage : KSH29	V_{CBO}	40	V
: KSH29C		100	V
Collector Emitter Voltage: KSH29	V_{CEO}	40	V
: KSH29C		100	V
Emitter Base Voltage	V_{EBO}	5	V
Collector Current(DC)	I_C	1	A
Collector Current(Pulse)	I_C	3	A
Base Current	I_B	0.4	A
Collector Dissipation($T_c=25^\circ\text{C}$)	P_C	15	W
Collector Dissipation($T_a=25^\circ\text{C}$)	P_C	1.56	W
Junction Temperature	T_j	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-65~150	$^\circ\text{C}$

D-PAK

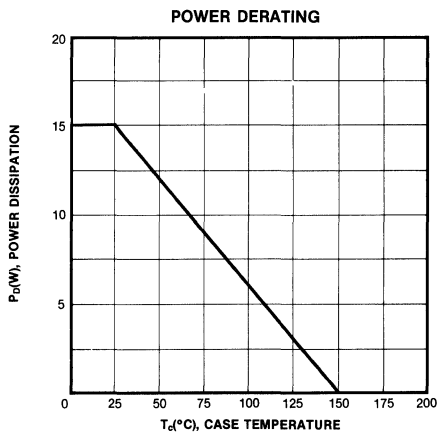
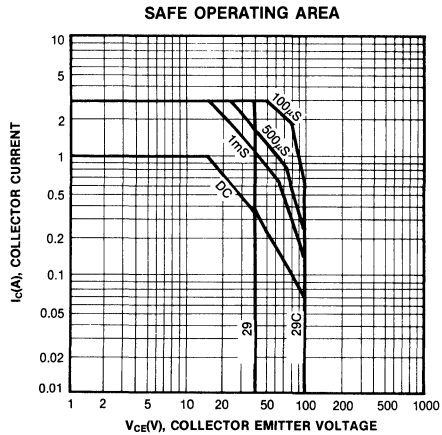
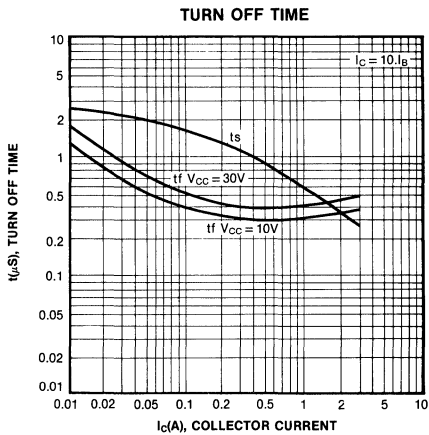
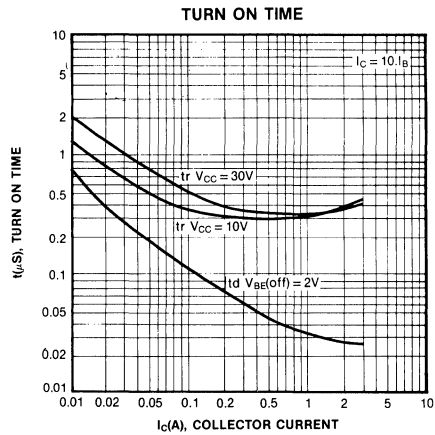
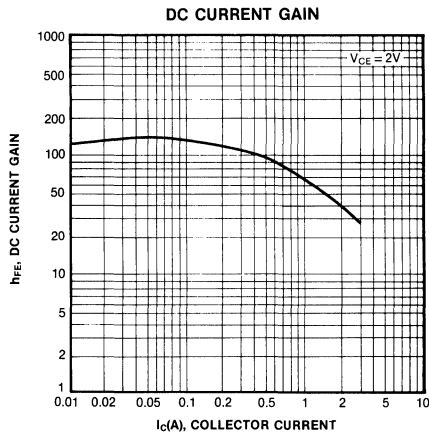


I-PAK



ELECTRICAL CHARACTERISTICS($T_a=25^\circ\text{C}$)

Characteristic	Symbol	Test Condition	Min	Max	Unit
Collector Emitter Sustaining Voltage : KSH29	$V_{CEO(sus)}$	$I_C=-30\text{mA}$, $I_B=0$	40		V
: KSH29C			100		V
Collector Cutoff Current : KSH29	I_{CEO}	$V_{CE}=40\text{V}$, $I_B=0$		50	μA
: KSH29C		$V_{CE}=60\text{V}$, $I_B=0$		50	μA
Collector Cutoff Current : KSH29	I_{CES}	$V_{CE}=40\text{V}$, $V_{EB}=0$		20	μA
: KSH29C		$V_{CE}=100\text{V}$, $V_{EB}=0$		20	μA
Emitter Cutoff Current	I_{EBO}	$V_{EB}=5\text{V}$, $I_C=0$		1	mA
*DC Current Gain	h_{FE}	$V_{CE}=4\text{V}$, $I_C=0.2\text{A}$	40		
		$V_{CE}=4\text{V}$, $I_C=1\text{A}$	15	75	
*Collector Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C=1\text{A}$, $I_B=125\text{mA}$	0.7	V	
*Base Emitter On Voltage	$V_{BE(on)}$	$V_{CE}=4\text{A}$, $I_C=1\text{A}$		1.3	V
Current Gain Bandwidth Product	f_T	$V_{CE}=10\text{V}$, $I_C=200\text{mA}$ $f=1\text{MHz}$	3		MHz



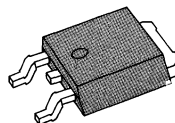
**GENERAL PURPOSE AMPLIFIER
LOW SPEED SWITCHING APPLICATIONS
D-PACK FOR SURFACE MOUNT
APPLICATIONS**

- Lead Formed for Surface Mount Applications (No Suffix)
- Straight Lead (I.PACK, "— I " Suffix)
- Electrically Similar to Popular MJE3055
- DC Current Gain Specified to 10A
- High Current Gain-Bandwidth Product:
 $f_T = 2\text{MHz (MIN)}$, $I_C = 500\text{mA}$

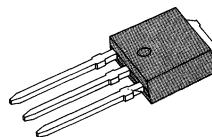
ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Characteristic	Symbol	Rating	Unit
Collector Base Voltage	V_{CBO}	70	V
Collector Emitter Voltage	V_{CEO}	60	V
Emitter Base Voltage	V_{EBO}	5	V
Collector Current	I_C	10	A
Base Current	I_B	6	A
Collector Dissipation ($T_c = 25^\circ\text{C}$)	P_c	20	W
Collector Dissipation ($T_a = 25^\circ\text{C}$)	P_c	1.75	W
Junction Temperature	T_j	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	- 55 ~ 150	$^\circ\text{C}$

D-PAK



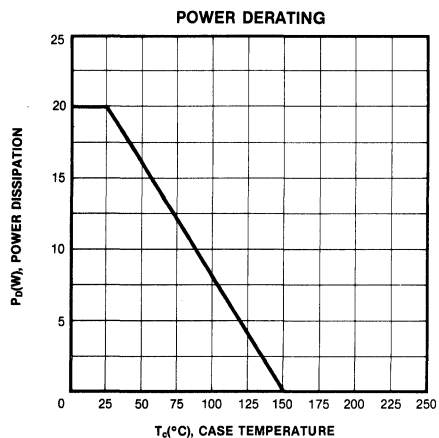
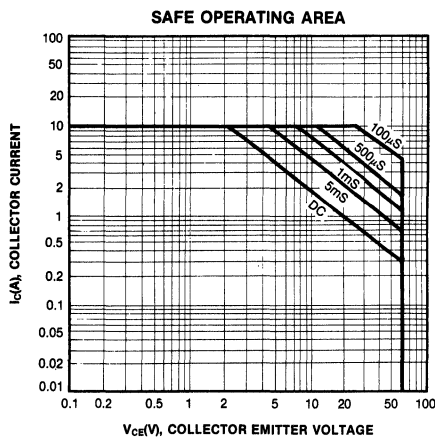
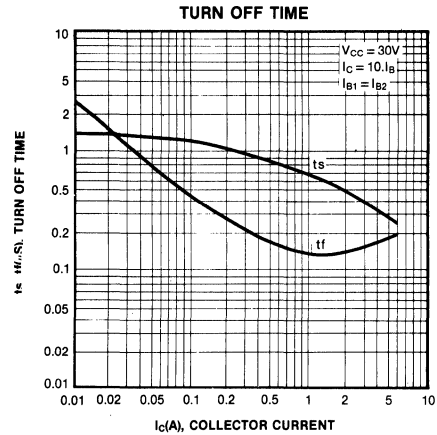
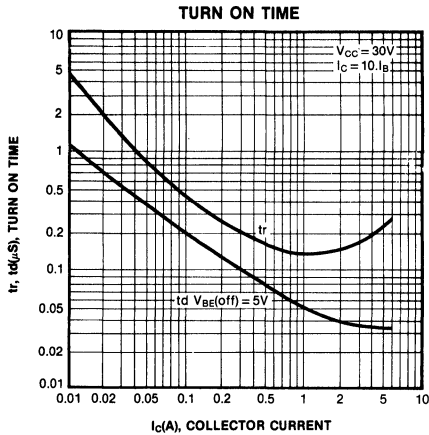
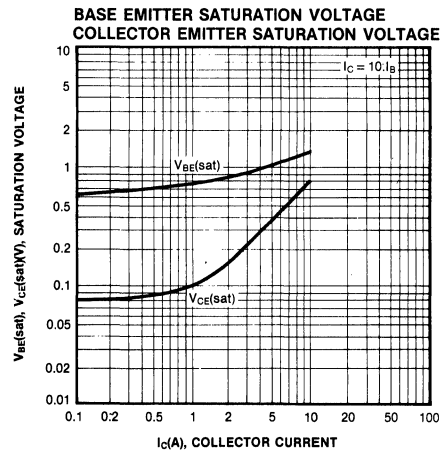
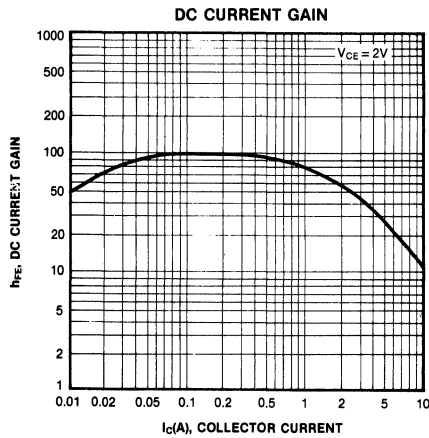
I-PAK



ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

Characteristic	Symbol	Test Condition	Min	Max	Unit
*Collector Emitter Sustaining Voltage	$V_{CEO(sus)}$	$I_C = 30\text{mA}$, $I_B = 0$	60		V
Collector Cutoff Current	I_{CEO}	$V_{CE} = 30\text{V}$, $I_B = 0$		50	μA
Collector Cutoff Current	I_{CBO}	$V_{CB} = 70\text{V}$, $I_E = 0$		2	mA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = 5\text{V}$, $I_C = 0$		0.5	mA
*DC Current Gain	h_{FE}	$V_{CE} = 4\text{V}$, $I_C = 4\text{A}$	20	100	
		$V_{CE} = 4\text{V}$, $I_C = 10\text{A}$	5		
*Collector Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 4\text{A}$, $I_B = 0.4\text{A}$		1.1	V
		$I_C = 10\text{A}$, $I_B = 3.3\text{A}$		8	V
*Base Emitter On Voltage	$V_{BE(on)}$	$V_{CE} = 4\text{A}$, $I_C = 4\text{A}$		1.8	V
Current Gain Bandwidth Product	f_T	$V_{CE} = 10\text{V}$, $I_C = 500\text{mA}$ $f = 500\text{KHz}$	2		MHz

* Pulse Test: $PW \leq 300\mu\text{S}$, Duty Cycle $\leq 2\%$



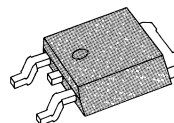
**GENERAL PURPOSE AMPLIFIER
LOW SPEED SWITCHING APPLICATIONS
D-PACK FOR SURFACE MOUNT
APPLICATIONS**

- Lead Formed for Surface Mount Applications (No Suffix)
- Straight Lead (I.PACK, "— I " Suffix)
- Electrically Similar to Popular TIP30 and TIP30C

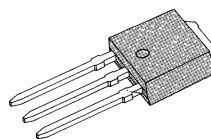
ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Characteristic	Symbol	Rating	Unit
Collector Base Voltage : KSH30	V_{CBO}	-40	V
: KSH30C		-100	V
Collector Emitter Voltage: KSH30	V_{CEO}	-40	V
: KSH30C		-100	V
Emitter Base Voltage	V_{EBO}	-5	V
Collector Current (DC)	I_C	-1	A
Collector Current (Pulse)	I_C	-3	A
Base Current	I_B	-0.4	A
Collector Dissipation ($T_c = 25^\circ\text{C}$)	P_c	-15	W
Collector Dissipation ($T_a = 25^\circ\text{C}$)	P_c	-1.56	W
Junction Temperature	T_j	-150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-65 ~ 150	$^\circ\text{C}$

D-PAK



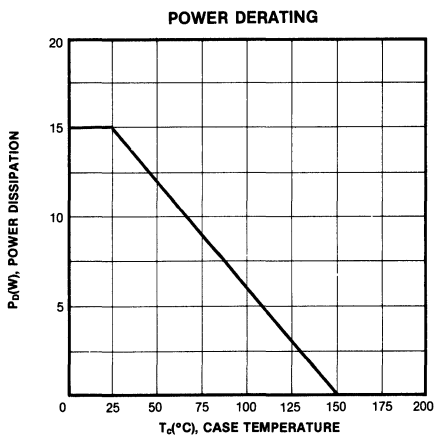
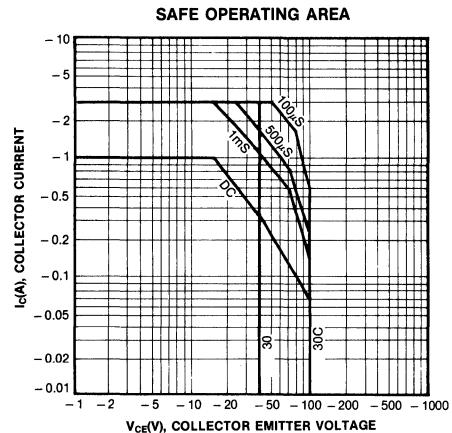
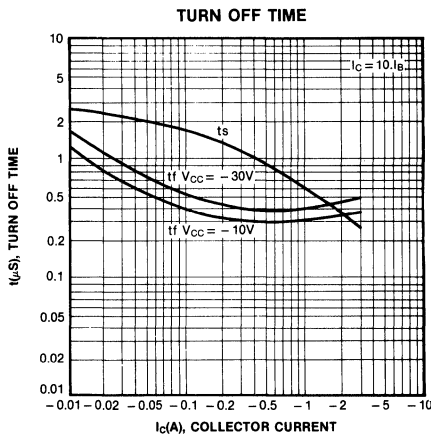
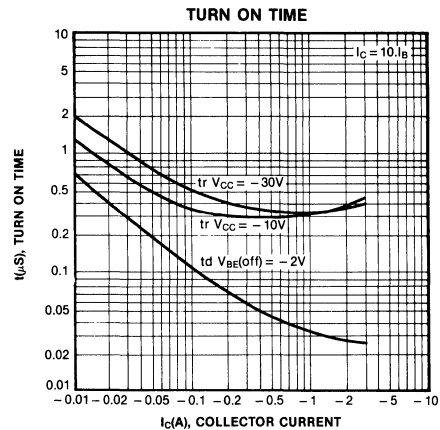
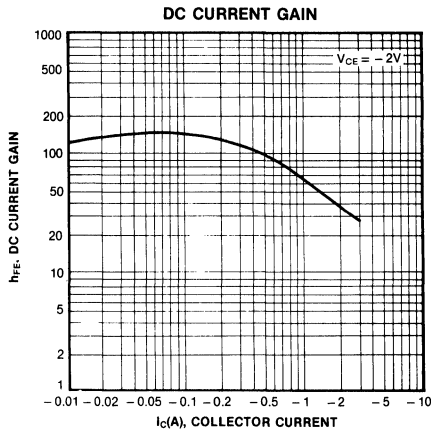
I-PAK



ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

Characteristic	Symbol	Test Condition	Min	Max	Unit
*Collector Emitter Sustaining Voltage: KSH30	$V_{CEO(sus)}$	$I_C = -30\text{mA}, I_B = 0$	-40		V
: KSH30C			-100		.V
Collector Cutoff Current : KSH30	I_{CEO}	$V_{CE} = -40\text{V}, I_B = 0$		-50	μA
: KSH30C		$V_{CE} = -60\text{V}, I_B = 0$		-50	μA
Collector Cutoff Current : KSH30	I_{CES}	$V_{CE} = -40\text{V}, V_{EB} = 0$		-20	μA
: KSH30C		$V_{CE} = -100\text{V}, V_{EB} = 0$		-20	μA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = -5\text{V}, I_C = 0$		-1	mA
*DC Current Gain	h_{FE}	$V_{CE} = -4\text{V}, I_C = -0.2\text{A}$	40		
		$V_{CE} = -4\text{V}, I_C = -1\text{A}$	15	75	
*Collector Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = -1\text{A}, I_B = -125\text{mA}$		-0.7	V
*Base Emitter On Voltage	$V_{BE(on)}$	$V_{CE} = -4\text{A}, I_C = -1\text{A}$		-1.3	V
Current Gain Bandwidth Product	f_T	$V_{CE} = -10\text{V}, I_C = -200\text{mA}$ $f = 1\text{MHz}$	3		MHz

* Pulse Test: $PW \leq 300\mu\text{S}$, Duty Cycle $\leq 2\%$



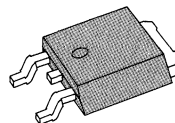
GENERAL PURPOSE POWER AND SWITCHING SUCH AS OUTPUT OR DRIVER STAGES IN APPLICATIONS D-PACK FOR SURFACE MOUNT APPLICATIONS

- Load Formed for Surface Mount Application(No Suffix)
- Straight Lead (I.PACK, "— I " Suffix)
- Electrically Similar to Popular KSE44H
- Fast Switching Speeds
- Low Collector Emitter Saturation Voltage

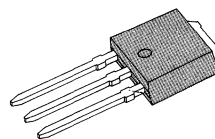
ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Characteristic	Symbol	Rating	Unit
Collector Emitter Voltage	V_{CEO}	80	V
Emitter Base Voltage	V_{EBO}	5	V
Collector Current (DC)	I_C	8	A
Collector Current (Pulse)	I_C	16	A
Collector Dissipation ($T_c = 25^\circ\text{C}$)	P_c	20	W
Collector Dissipation ($T_a = 25^\circ\text{C}$)	P_c	1.75	W
Junction Temperature	T_j	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	- 55 ~ 150	$^\circ\text{C}$

D-PAK



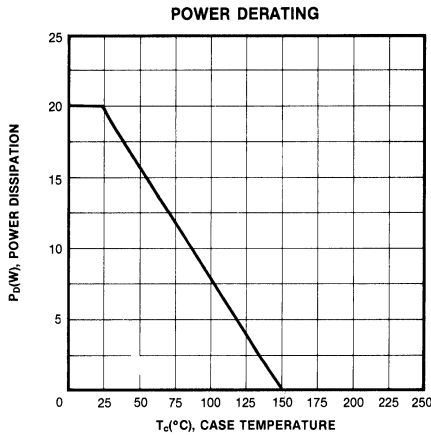
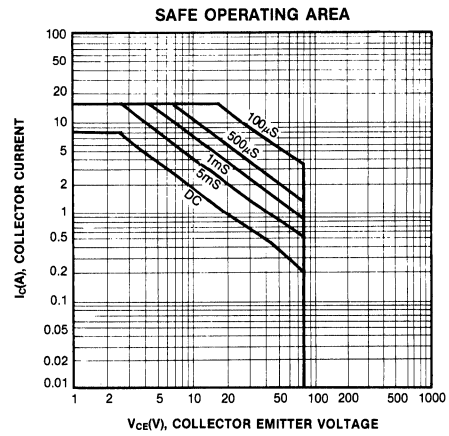
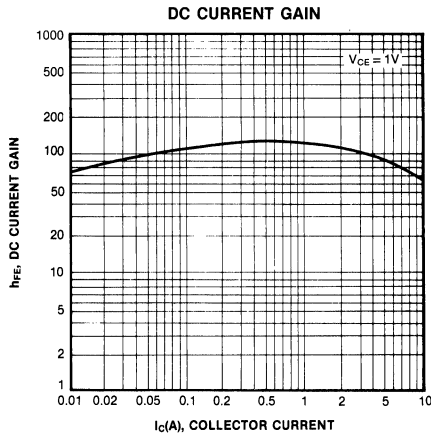
I-PAK



ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Collector Emitter Sustaining Voltage	$V_{CEO(sus)}$	$I_C = 30\text{mA}$, $I_B = 0$	80			V
Collector Cutoff Current	I_{CEO}	$V_{CE} = 80\text{V}$, $I_B = 0$			10	μA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = 5\text{V}$, $I_C = 0$			50	μA
DC Current Gain	h_{FE}	$V_{CE} = 1\text{V}$, $I_C = 2\text{A}$	60			
		$V_{CE} = 1\text{V}$, $I_C = 4\text{A}$	40			
Collector Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 8\text{A}$, $I_B = 0.4\text{A}$			1	V
Base Emitter Saturation Voltage	$V_{BE(sat)}$	$I_C = 8\text{A}$, $I_B = 0.8\text{A}$			1.5	V
Current Gain Bandwidth Product	f_T	$V_{CE} = 10\text{V}$, $I_C = 0.5\text{A}$ $f = 20\text{MHz}$		50		MHz
Collector Capacitance	C_{cb}	$V_{CB} = 10\text{V}$, $f = 1\text{MHz}$		130		pF
Turn On Time	t_{on}	$I_C = 5\text{A}$, $I_{B1} = 0.5\text{A}$		300		nS
Storage Time	t_{stg}	$I_{B1} = I_{B2} = 0.5\text{A}$		500		nS
Fall Time	t_f			140		nS

* Pulse Test: $PW \leq 300\mu\text{S}$, Duty Cycle $\leq 2\%$



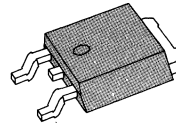
GENERAL PURPOSE POWER AND SWITCHING SUCH AS OUTPUT OR DRIVER STAGES IN APPLICATIONS D-PAK FOR SURFACE MOUNT APPLICATIONS

- Load Formed for Surface Mount Application(No Suffix)
- Straight Lead (I.PACK, "— I " Suffix)
- Electrically Similar to Popular KSE45H
- Fast Switching Speeds
- Low Collector Emitter Saturation Voltage

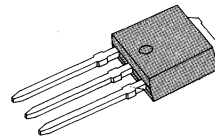
ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Characteristic	Symbol	Rating	Unit
Collector Emitter Voltage	V_{CEO}	- 80	V
Emitter Base Voltage	V_{EBO}	- 5	V
Collector Current (DC)	I_C	- 8	A
Collector Current (Pulse)	I_C	- 16	A
Collector Dissipation ($T_c = 25^\circ\text{C}$)	P_c	- 20	W
Collector Dissipation ($T_a = 25^\circ\text{C}$)	P_c	1.75	W
Junction Temperature	T_j	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	- 55 ~ 150	$^\circ\text{C}$

D-PAK



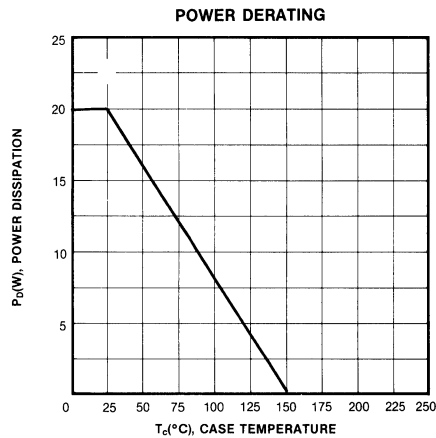
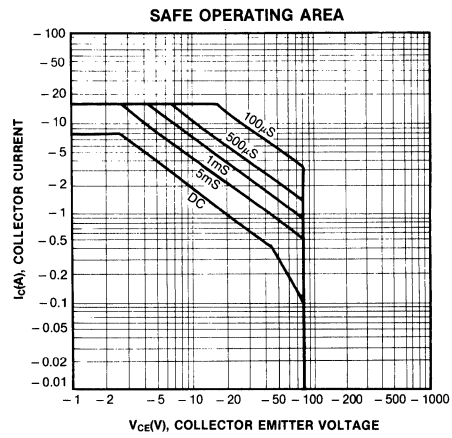
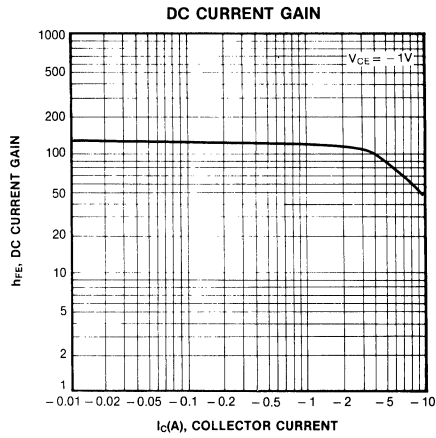
I-PAK



ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

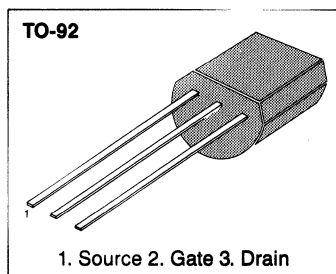
Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Collector Emitter Sustaining Voltage	$V_{CEO(sus)}$	$I_C = -30\text{mA}, I_B = 0$	- 80			V
Collector Cutoff Current	I_{CEO}	$V_{CE} = -80\text{V}, I_B = 0$			- 10	μA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = -5\text{V}, I_C = 0$			- 50	μA
DC Current Gain	h_{FE}	$V_{CE} = -1\text{V}, I_C = -2\text{A}$	60			
		$V_{CE} = -1\text{V}, I_C = -4\text{A}$	40			
Collector Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = -8\text{A}, I_B = -0.4\text{A}$			- 1	V
Base Emitter Saturation Voltage	$V_{BE(sat)}$	$I_C = -8\text{A}, I_B = -0.8\text{A}$			- 1.5	V
Current Gain Bandwidth Product	f_T	$V_{CE} = -10\text{V}, I_C = -0.5\text{A}$ $f = 20\text{MHz}$		40		MHz
Collector Capacitance	C_{cb}	$V_{CB} = -10\text{V}, f = 1\text{MHz}$		230		pF
Turn On Time	t_{on}	$I_C = -5\text{A}, I_{B1} = -0.5\text{A}$		135		nS
Storage Time	t_{stg}	$I_{B1} = I_{B2} = -0.5\text{A}$		500		nS
Fall Time	t_f			100		nS

* Pulse Test: $PW \leq 300\mu\text{S}$, Duty Cycle $\leq 2\%$



FEATURES

- Fast switching speeds
- TO-92 Package



PRODUCT SUMMARY

Part Number	V _{DS}	R _{DS(on)}	I _{D(on)}
2N7000	60V	5.0 Ω	200 mA

MAXIMUM RATINGS

Characteristic	Symbol	2N7000	Units
Drain-Source Voltage (1)	V _{DSS}	60	Vdc
Drain Gate Voltage (R _{GS} = 1.0M Ω) (1)	V _{DGR}	60	Vdc
Gate Source Voltage	V _{GS}	± 40	Vdc
Continuous Drain Current T _C = 25°C	I _D	200	mAdc
Drain Current — Pulsed (3)	I _{DM}	1000	mAdc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	P _D	400 3.2	mWatts mW/°C
Operating and Storage Junction Temperature Range	T _J , T _{STG}	- 55 to 150	°C
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T _L	300	°C

Notes: (1) T_J = 25°C to 150°C

(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse width limited by max. junction temperature

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

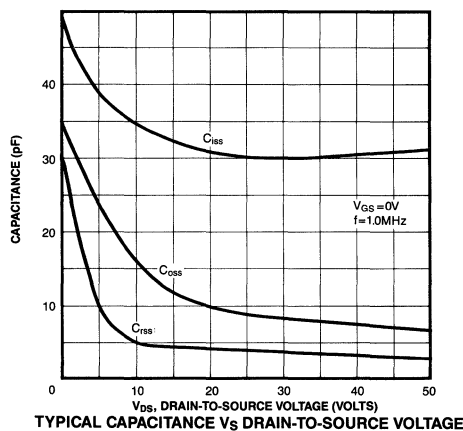
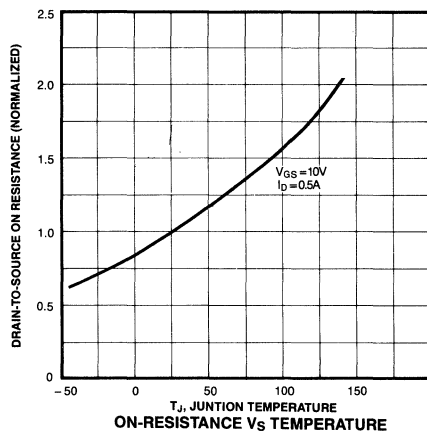
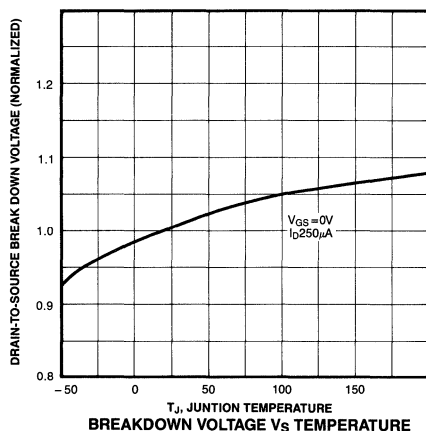
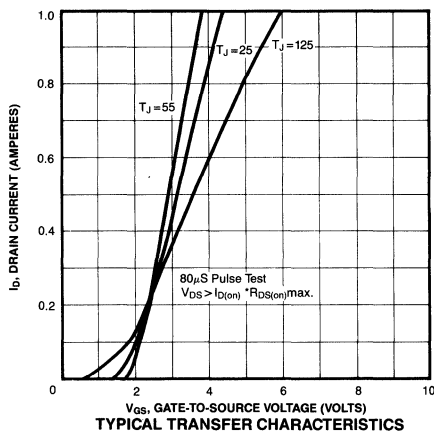
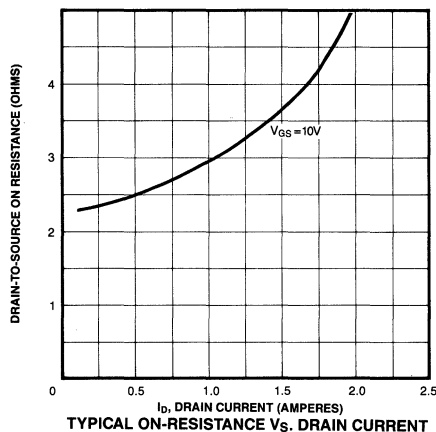
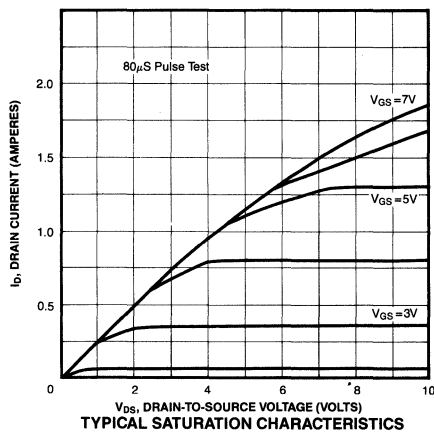
Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
BV_{DSS}	Drain Source Breakdown Voltage	60	—	—	V	$V_{GS} = 0V$ $I_D = 100\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	0.8	—	3.0	V	$V_{DS} = V_{GS}$, $I_D = 1.0mA$
I_{GSS}	Gate Source Leakage Forward	—	—	100	nA	$V_{GS} = 15V$
I_{GSS}	Gate Source Leakage Reverse	—	—	- 100	nA	$V_{GS} = -15V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	1.0	μA	$V_{DS} = 30$, $V_{GS} = 0V$
		—	—	1000	μA	$V_{DS} = 30$, $V_{GS} = 0V$, $T_C = 125^\circ\text{C}$
$I_{D(on)}$	On static Drain Source Current (2)	200	—	—	mA	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max. $V_{GS} = 10V$
$R_{DS(on)}$	Static Drain Source On State Resistance (2)	—	2.5	5.0	Ω	$V_{GS} = 10V$, $I_D = 0.5A$
g_{fs}	Forward Transconductance (2)	100	300	—	mS	$V_{DS} > 15V$, $I_D = 0.5A$
C_{iss}	Input Capacitance	—	30	—	pF	$V_{GS} = 0V$, $V_{DS} = 25V$, $f = 1.0MHz$
C_{oss}	Output Capacitance	—	12	—	pF	
C_{rss}	Reverse Transfer Capacitance	—	3.0	—	pF	
$t_{d(on)}$	Turn On Delay Time	—	—	10	ns	$V_{DD} = 0.5 BV_{DSS}$, $I_D = 0.5A$, $Z_O = 25\text{ Ohms}$, (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	—	—	10	ns	
$t_{d(off)}$	Turn Off Delay Time	—	—	10	ns	
t_f	Fall Time	—	—	10	ns	

THERMAL RESISTANCE

R_{thJA}	Junction to Ambient	—	—	312.5	K/W	Free Air Operation
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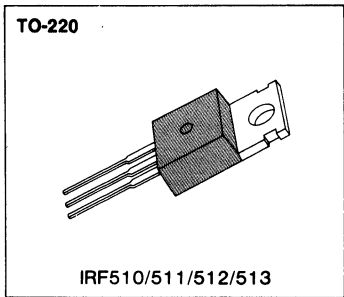
Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive: Pulse width limited by max. junction temperature



FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability



PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF510	100V	0.54Ω	5.6A
IRF511	80V	0.54Ω	5.6A
IRF512	100V	0.74Ω	4.9A
IRF513	80V	0.74Ω	4.9A

MAXIMUM RATINGS

Characteristic	Symbol	IRF510	IRF511	IRF512	IRF513	Unit
Drain-Source Voltage (1)	V_{DSS}	100	80	100	80	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	100	80	100	80	Vdc
Gate-Source Voltage	V_{GS}	± 20				Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	5.6	5.6	4.9	4.9	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	4.0	4.0	3.4	3.4	Adc
Drain Current—Pulsed (3)	I_{DM}	20	20	18	18	Adc
Gate Current—Pulsed	I_{GM}	± 1.5				Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	19				mJ
Avalanche Current	I_{AS}	5.6				A
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	43 0.34				Watts W/ $^\circ C$
Operating and Storage Junction to Case	T_J, T_{stg}	-55 to 150				$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300				$^\circ C$

- Notes: (1) $T_J=25^\circ C$ to $150^\circ C$
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature
(4) $L=0.19\text{ mH}$, $V_{dd}=25V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-Source Breakdown Voltage IRF510/512	100	—	—	V	V _{GS} =0V
	IRF511/513	80	—	—	V	I _D =250μA
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} =V _{GS} , I _D =250μA
I _{GSS}	Gate-Source Leakage Forward	—	—	100	nA	V _{GS} =20V
I _{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	V _{GS} =-20V
I _{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	V _{DS} =Max. Rating, V _{GS} =0V
		—	—	1000	μA	V _{DS} =Max. Rating×0.8, V _{GS} =0V, T _C =125°C
I _{D(on)}	On-State Drain-Source Current (2) IRF510/511	5.6	—	—	A	V _{DS} ≥4.1V, V _{GS} =10V
	IRF512/513	4.9	—	—	Ω	
R _{DS(on)}	Static Drain-Source On-State Resistance (2) IRF510/511	—	0.41	0.54	Ω	V _{GS} =10V, I _D =3.4A
	IRF512/513	—	0.54	0.74	Ω	
g _{fs}	Forward Transconductance (2)	1.3	2.0	—	Ω	V _{DS} ≥50V, I _D =3.4A
C _{iss}	Input Capacitance	—	180	—	pF	V _{GS} =0V, V _{DS} =25V, f=1.0MHz
C _{oss}	Output Capacitance	—	82	—	pF	
C _{rss}	Reverse Transfer Capacitance	—	20	—	pF	
t _{d(on)}	Turn-On Delay Time	—	7.6	11	ns	V _{DD} =0.5BV _{DSS} , I _D =3.4A, Z _O =24Ω (MOSFET switching times are essentially independent of operating temperature)
t _r	Rise Time	—	24	36	ns	
t _{d(off)}	Turn-Off Delay Time	—	14	21	ns	
t _f	Fall Time	—	14	21	ns	
Q _g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	5.2	7.7	nC	V _{GS} =10V, I _D =5.6A, V _{DS} =0.8 Max. Rating (Gate charge is essentially independent of operating temperature.)
Q _{gs}	Gate-Source Charge	—	1.5	2.3	nC	
Q _{gd}	Gate-Drain ("Miller") Charge	—	2.2	3.2	nC	

THERMAL RESISTANCE

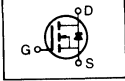
R _{thJC}	Junction-to-Case	—	—	2.9	KW	
R _{thCS}	Case-to-Sink	—	0.5	—	K/W	Mounting surface flat, smooth, and greased
R _{thJA}	Junction-to-Ambient	—	—	80	K/W	Free Air Operation

Notes: (1) T_J=25°C to 150°C

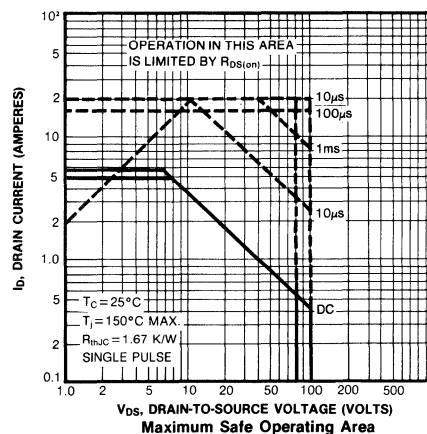
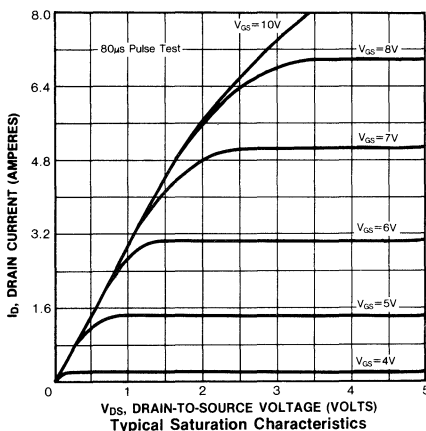
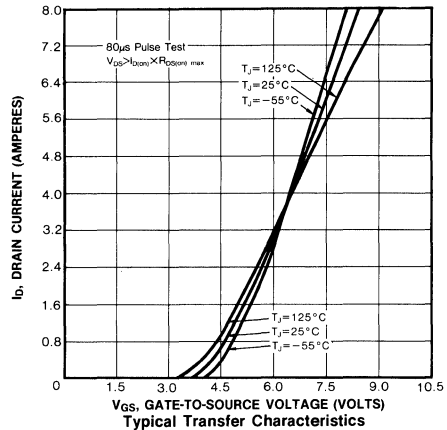
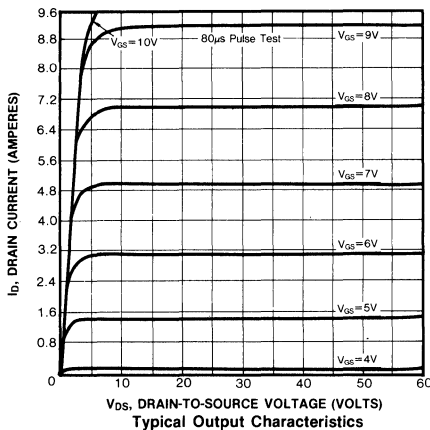
(2) Pulse test: Pulse width≤300μs, Duty Cycle≤2%

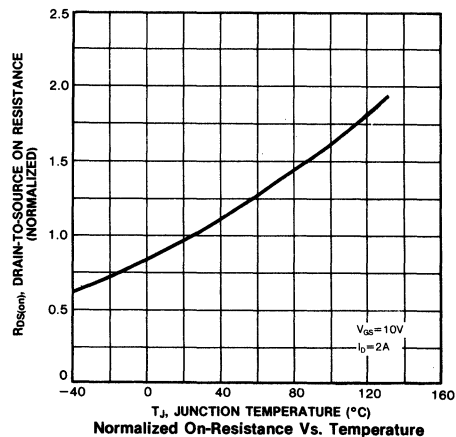
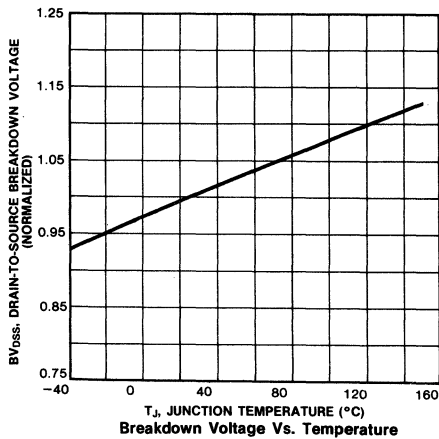
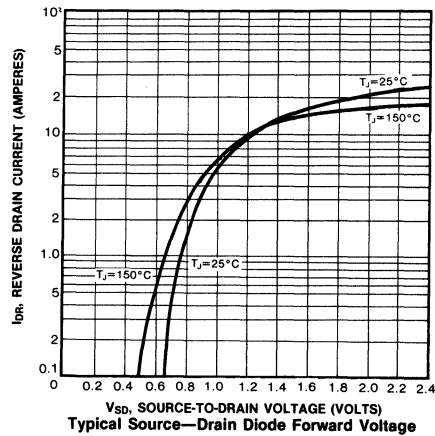
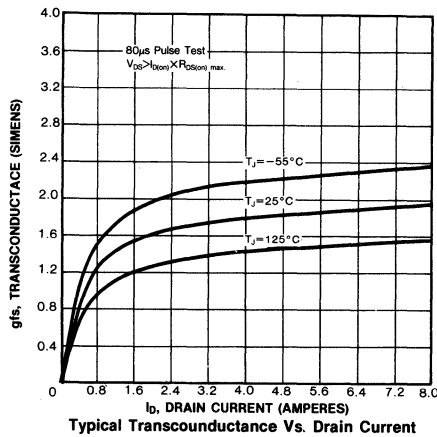
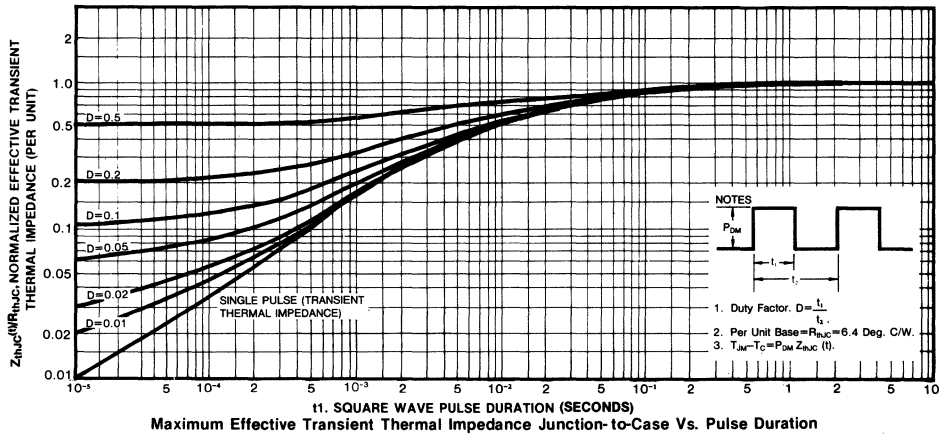
(3) Repetitive rating: Pulse width limited by max. junction temperature

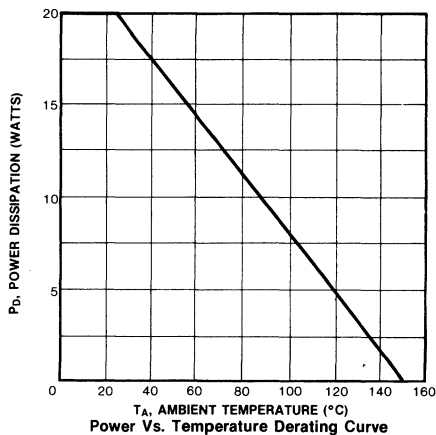
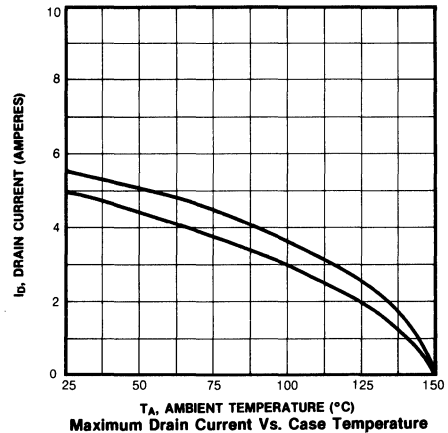
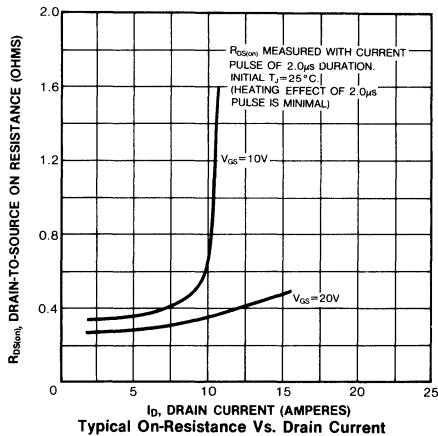
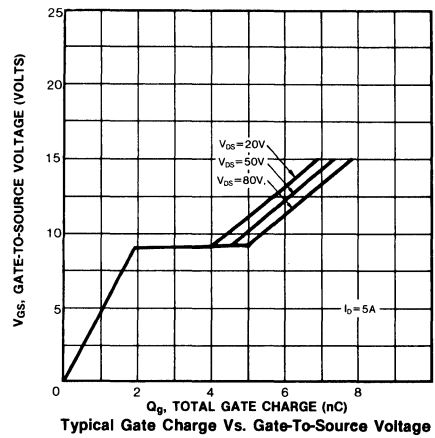
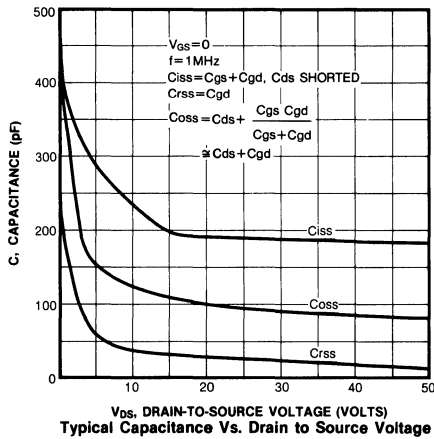
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic	Type	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	IRF510	—	—	5.6	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier 
		IRF511	—	—	5.6	A	
		IRF512	—	—	4.9	A	
		IRF513	—	—	4.9	A	
I_{SM}	Pulse Source Current (Body Diode) 1	IRF510	—	—	20	A	
		IRF511	—	—	20	A	
		IRF512	—	—	18	A	
		IRF513	—	—	18	A	
V_{SD}	Diode Forward Voltage 2	IRF510	—	—	2.5	V	$T_C = 25^\circ\text{C}$, $I_S = 5.6\text{A}$, $V_{GS} = 0\text{V}$
		IRF511	—	—	2.5	V	$T_C = 25^\circ\text{C}$, $I_S = 5.6\text{A}$, $V_{GS} = 0\text{V}$
		IRF512	—	—	2.0	V	$T_C = 25^\circ\text{C}$, $I_S = 4.9\text{A}$, $V_{GS} = 0\text{V}$
		IRF513	—	—	2.0	V	$T_C = 25^\circ\text{C}$, $I_S = 4.9\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time		—	230	—	ns	$T_J = 25^\circ\text{C}$, $I_F = 5.6\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{s}$

Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature



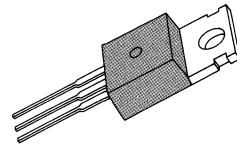




FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

TO-220



IRF520/521/522/523

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF520	100V	0.27Ω	9.2A
IRF521	80V	0.27Ω	9.2A
IRF522	100V	0.36Ω	8.0A
IRF523	80V	0.36Ω	8.0A

MAXIMUM RATINGS

Characteristics	Symbol	IRF520	IRF521	IRF522	IRF523	Unit
Drain-Source Voltage (1)	V_{DSS}	100	80	100	80	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	100	80	100	80	Vdc
Gate-Source Voltage	V_{GS}	± 20				Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	9.2	9.2	8.0	8.0	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	6.5	6.5	5.6	5.6	Adc
Drain Current—Pulsed (3)	I_{DM}	37	37	32	32	Adc
Gate Current—Pulsed	I_{GM}	± 1.5				Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	36				mJ
Avalanche Current	I_{AS}	9.2				A
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	60 0.48				Watts W/ $^\circ C$
Operating and Storage Junction to Case	T_J, T_{stg}	-55 to 150				$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300				$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=0.64$ mH, $V_{dd}=25V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS (T_C=25 °C unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-Source Breakdown Voltage	100	—	—	V	V _{GS} =0V I _D =250μA
	IRF520					
	IRF522					
	IRF521 IRF523	80	—	—	V	
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} =V _{GS} , I _D =250μA
I _{GSS}	Gate-Source Leakage Forward	—	—	100	nA	V _{GS} =20V
I _{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	V _{GS} =-20V
I _{DSS}	Zero Gate Voltage	—	—	250	μA	V _{DS} =Max. Rating, V _{GS} =0V
	Drain Current	—	—	1000	μA	V _{DS} =Max. Rating×0.8, V _{GS} =0V, T _C =125 °C
I _{D(on)}	On-State Drain-Source Current (2)	9.2	—	—	A	V _{DS} ≥3.3V, V _{GS} =10V
	IRF520					
	IRF521					
	IRF522 IRF523	8.0	—	—	A	
R _{DS(on)}	Static Drain-Source On-State Resistance (2)	—	0.25	0.27	Ω	V _{GS} =10V, I _D =5.6A
	IRF520					
	IRF521					
	IRF522 IRF523	—	0.27	0.36	Ω	
g _{fs}	Forward Transconductance (2)	2.7	4.1	—	Ω	V _{DS} ≥50V, I _D =5.6A
C _{iss}	Input Capacitance	—	400	—	pF	V _{GS} =0V, V _{DS} =25V, f=1.0MHz
C _{oss}	Output Capacitance	—	130	—	pF	
C _{rss}	Reverse Transfer Capacitance	—	40	—	pF	
t _{d(on)}	Turn-On Delay Time	—	8.8	13	ns	
t _r	Rise Time	—	30	45	ns	V _{DD} =0.5BV _{DSS} , I _D =5.6A, Z _O =18Ω (MOSFET switching times are essentially independent of operating temperature)
t _{d(off)}	Turn-Off Delay Time	—	19	27	ns	
t _f	Fall Time	—	20	30	ns	
Q _g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	9.8	15	nC	V _{GS} =10V, I _D =9.2A, V _{DS} =0.8 Max. Rating (Gate charge is essentially independent of operating temperature.)
Q _{gs}	Gate-Source Charge	—	2.2	3.3	nC	
Q _{gd}	Gate-Drain ("Miller") Charge	—	2.3	3.4	nC	

THERMAL RESISTANCE

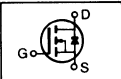
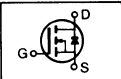
Symbol	Characteristic		IRF520-3	Unit	
R _{thJC}	Junction-to-Case	MAX	2.08	K/W	
R _{thCS}	Case-to-Sink	TYP	0.5	K/W	Mounting surface flat, smooth, and greased
R _{thJA}	Junction-to-Ambient	MAX	80	K/W	Free Air Operation

Notes: (1) T_J=25 °C to 150 °C

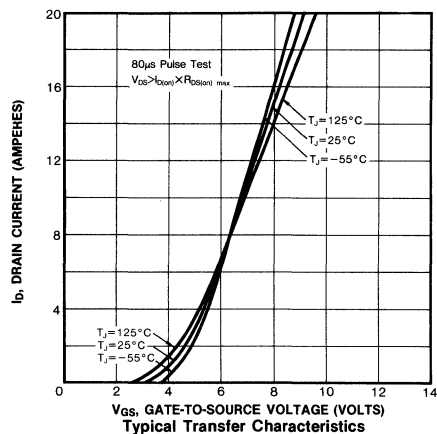
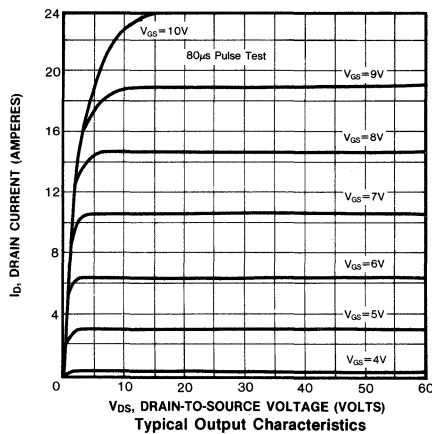
(2) Pulse test: Pulse width≤300μs, Duty Cycle≤2%

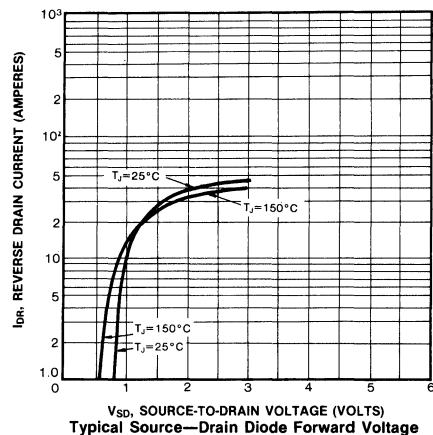
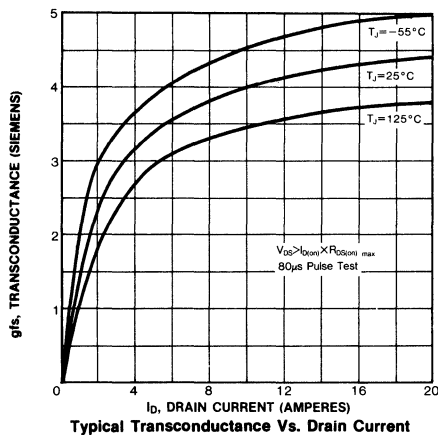
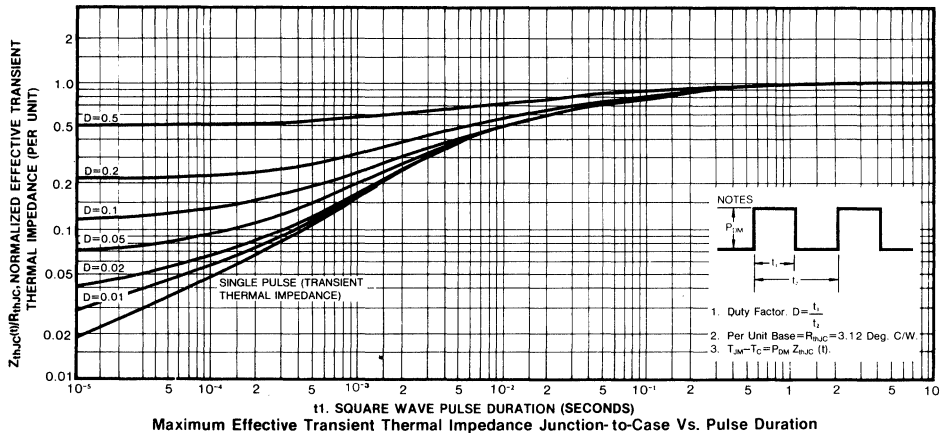
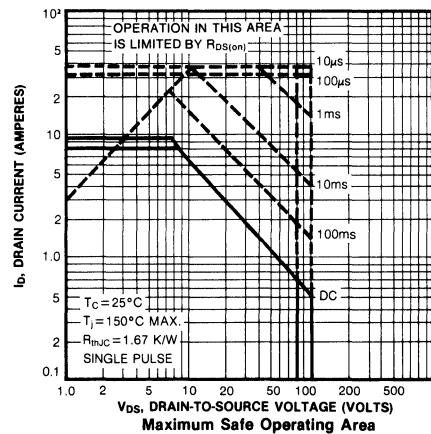
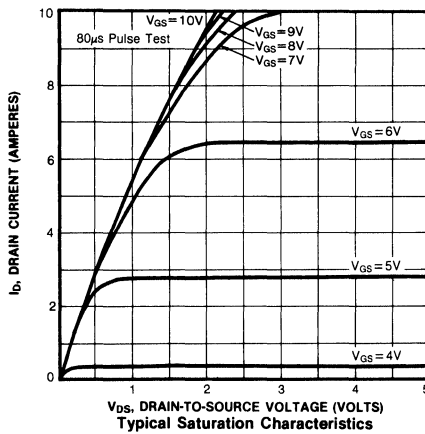
(3) Repetitive rating: Pulse width limited by max. junction temperature

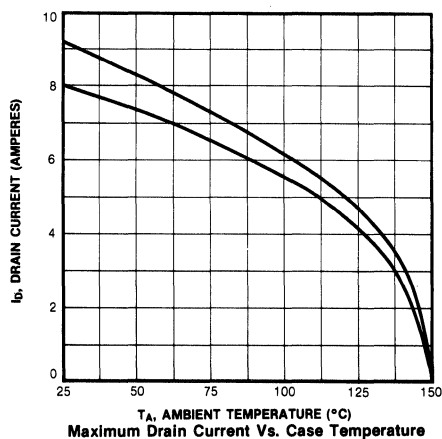
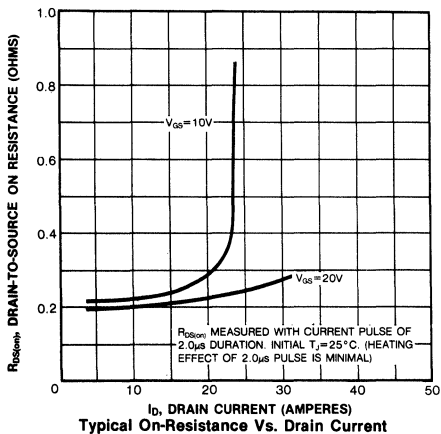
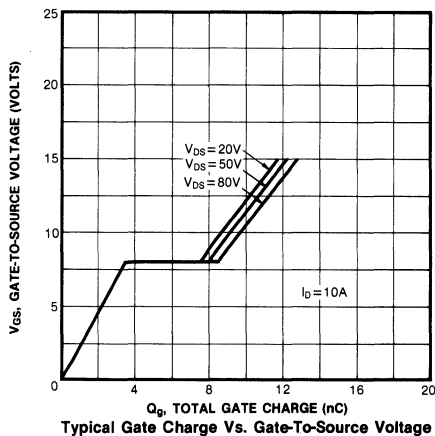
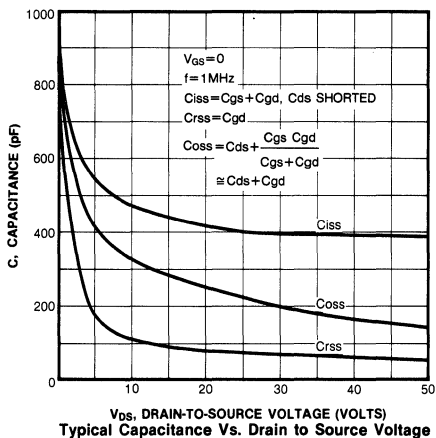
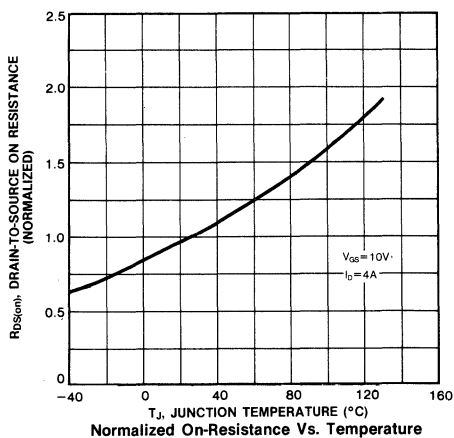
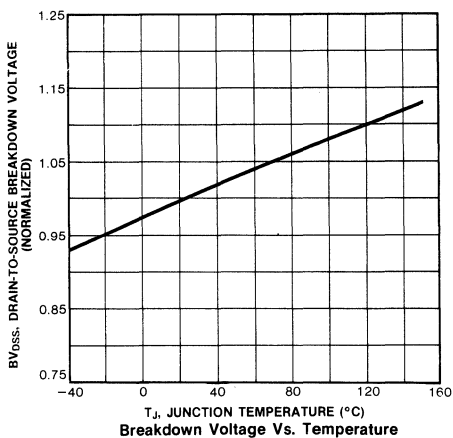
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

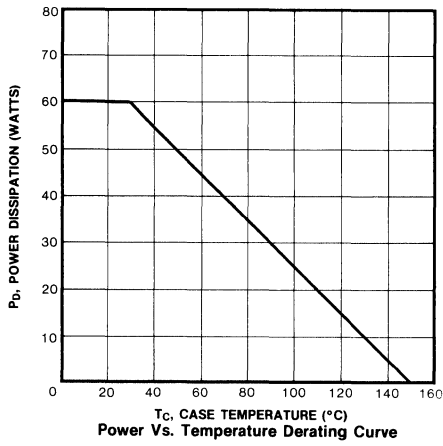
Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)					Modified MOSFET symbol showing the integral reverse P-N junction rectifier 
	IRF520	—	—	9.2	A	
	IRF521					
	IRF522					
I_{SM}	Pulse Source Current(Body Diode)(3)					Modified MOSFET symbol showing the integral reverse P-N junction rectifier 
	IRF520	—	—	37	A	
	IRF521					
	IRF522					
V_{SD}	Diode Forward Voltage (2)					$T_C=25^\circ\text{C}$, $I_S=9.2\text{A}$, $V_{GS}=0\text{V}$
	IRF520	—	—	2.5	V	
	IRF521					
	IRF522					
t_{rr}	Reverse Recovery Time	—	110	240	ns	$T_J=25^\circ\text{C}$, $I_F=9.2\text{A}$, $dI_F/dt=100\text{A}/\mu\text{S}$

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature









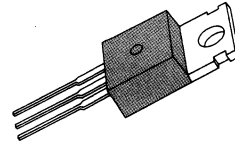
FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

PRODUCT SUMMARY

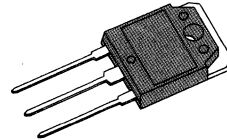
Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF530/IRFP130	100V	0.16Ω	14A
IRF531/IRFP131	80V	0.16Ω	14A
IRF532/IRFP132	100V	0.23Ω	12A
IRF533/IRFP133	80V	0.23Ω	12A

TO-220



IRF530/531/532/533

TO-3P



IRFP130/131/132/133

MAXIMUM RATINGS

Characteristics	Symbol	IRF530 IRFP130	IRF531 IRFP131	IRF532 IRFP132	IRF533 IRFP133	Unit
Drain-Source Voltage (1)	V_{DS}	100	80	100	80	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	100	80	100	80	Vdc
Gate-Source Voltage	V_{GS}	± 20				Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	14	14	12	12	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	10	10	8.3	8.3	Adc
Drain Current—Pulsed (3)	I_{DM}	56	56	48	48	Adc
Gate Current—Pulsed	I_{GM}	± 1.5				Adc
Single Pulsed Avalanche Energy(4)	E_{AS}	69				mJ
Avalanche Current	I_{AS}	14				A
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	77 0.62				Watts W/ $^\circ C$
Operating and Storage Junction to Case	T_J, T_{stg}	-55 to 150				$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300				$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=0.53 mH$, $V_{dd}=25V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage IRF530/IRFP130 IRF532/IRFP132	100	—	—	V	$V_{GS}=0V$ $I_D=250\mu A$
	IRF531/IRFP131 IRF533/IRFP133	80	—	—	V	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}$, $I_D=250\mu A$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS}=20V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	$V_{GS}=-20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS}=\text{Max. Rating}$, $V_{GS}=0V$
		—	—	1000	μA	$V_{DS}=\text{Max. Rating} \times 0.8$, $V_{GS}=0V$, $T_C=125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2) IRF530/IRFP130 IRF531/IRFP131	14	—	—	A	$V_{DS} \geq 3.2V$, $V_{GS}=10V$
	IRF532/IRFP132 IRF533/IRFP133	12	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance (2) IRF530/IRFP130 IRF531/IRFP131	—	0.10	0.16	Ω	$V_{GS}=10V$, $I_D=8.3A$
	IRF532/IRFP132 IRF533/IRFP133	—	0.16	0.23	Ω	
g_{fs}	Forward Transconductance (2)	5.1	7.6	—	Ω	$V_{DS} \geq 50V$, $I_D=8.3A$
C_{iss}	Input Capacitance	—	640	—	pF	$V_{GS}=0V$, $V_{DS}=25V$, $f=1.0\text{MHz}$
C_{oss}	Output Capacitance	—	240	—	pF	
C_{rss}	Reverse Transfer Capacitance	—	72	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	10	15	ns	$V_{DD}=0.5BV_{DSS}$, $I_D=8.3A$, $Z_0=12\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	34	51	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	23	35	ns	
t_f	Fall Time	—	24	36	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	17	26	nC	$V_{GS}=10V$, $I_D=14A$, $V_{DS}=0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	3.7	5.5	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	7	11	nC	

THERMAL RESISTANCE

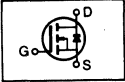
Symbol	Characteristic		IRF530-3	IRFP130-3	Unit	
R_{thJC}	Junction-to-Case	MAX	1.62	1.62	K/W	
R_{thCS}	Case-to-Sink	TYP	0.5	0.24	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	MAX	80	40	K/W	Free Air Operation

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C

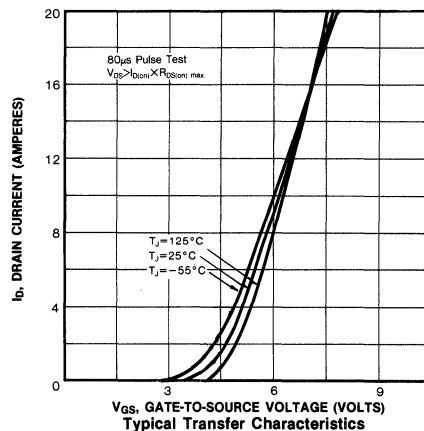
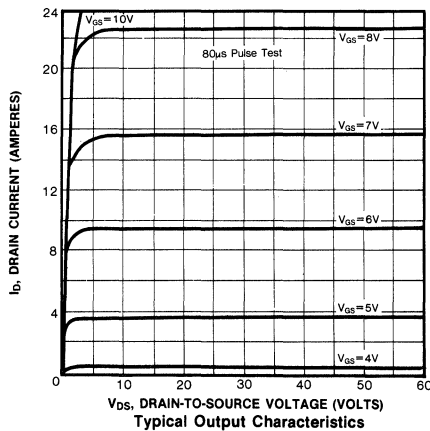
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

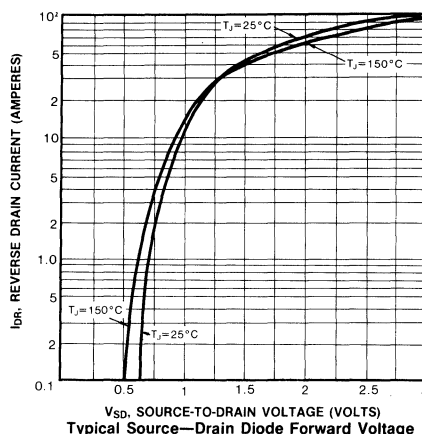
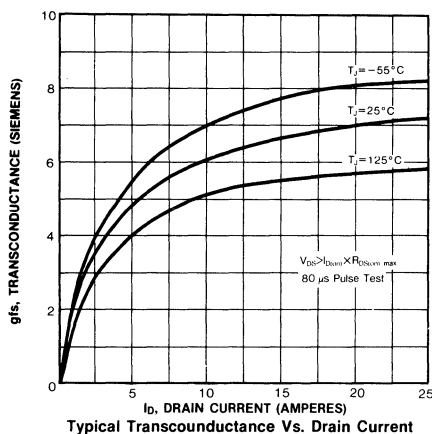
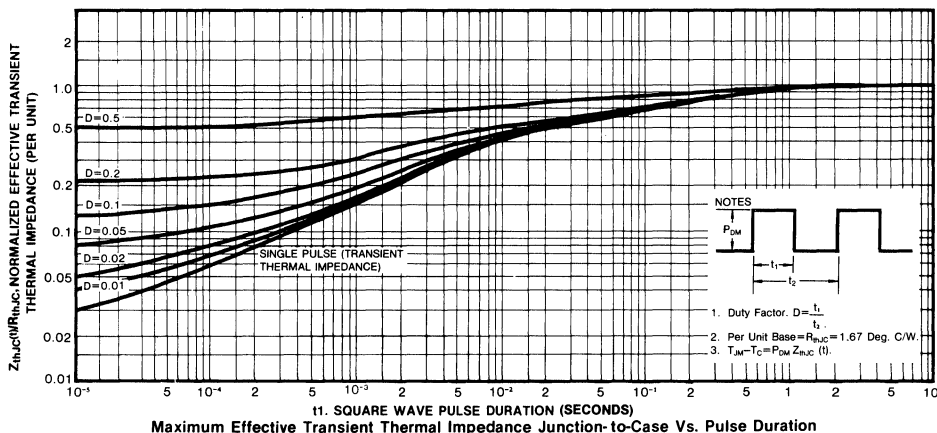
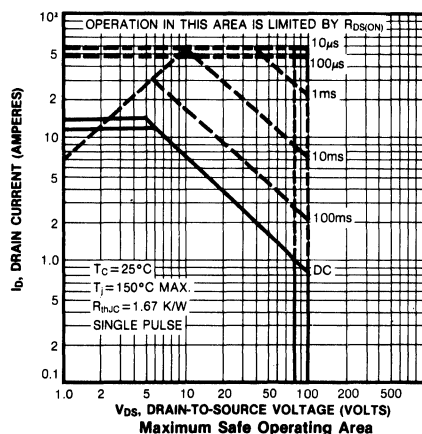
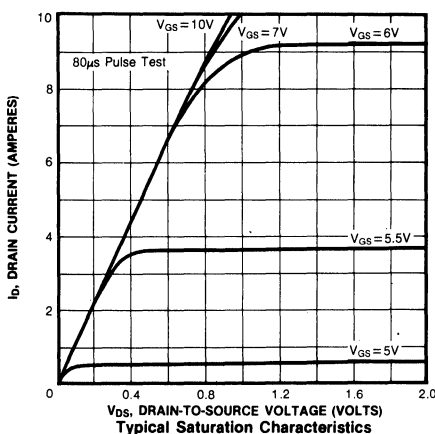
(3) Repetitive rating: Pulse width limited by max. junction temperature

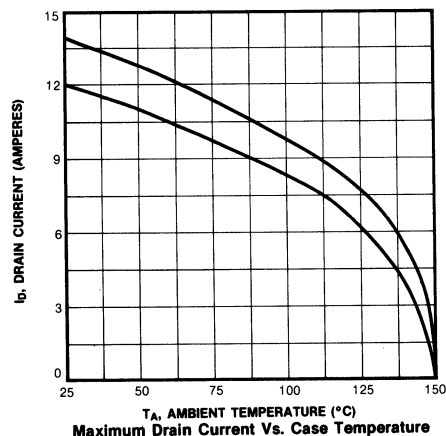
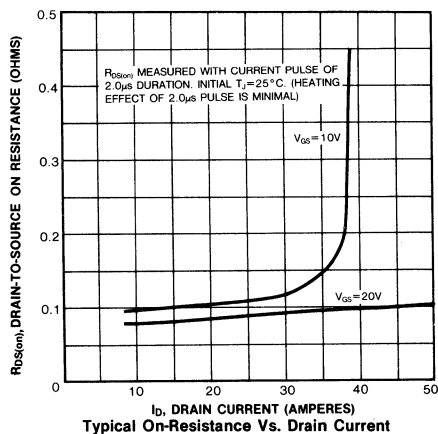
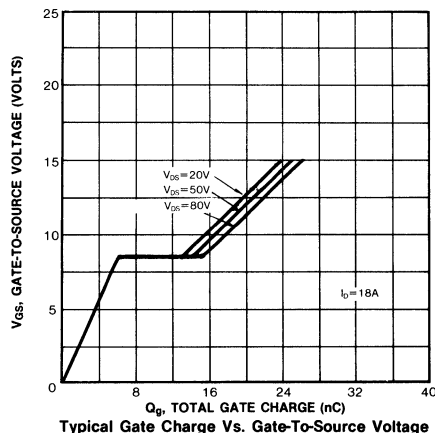
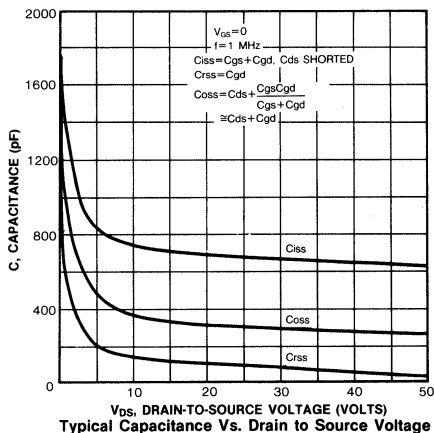
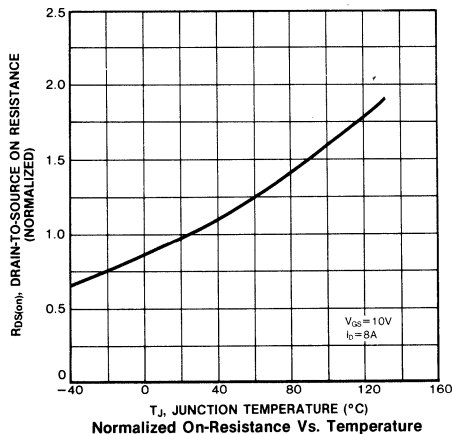
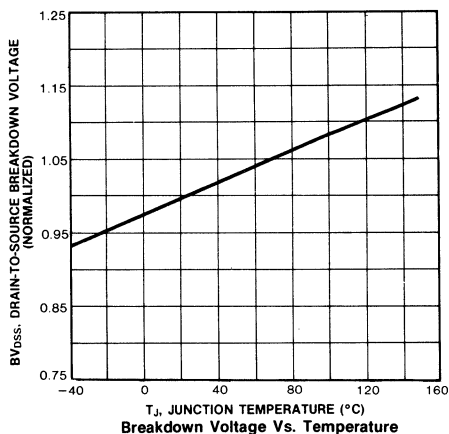
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

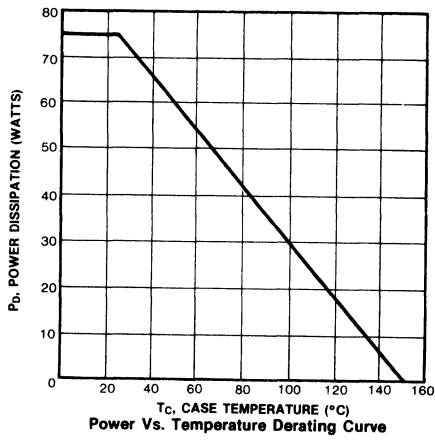
Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode) IRF530/IRFP130 IRF531/IRFP131	—	—	14	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier 
	IRF532/IRFP132 IRF533/IRFP133	—	—	12	A	
I_{SM}	Pulse Source Current(Body Diode)(3) IRF530/IRFP130 IRF531/IRFP131	—	—	56	A	
	IRF532/IRFP132 IRF533/IRFP133	—	—	48	A	
V_{SD}	Diode Forward Voltage (2) IRF530/IRFP130 IRF531/IRFP131	—	—	2.5	V	$T_C=25^\circ\text{C}$, $I_S=14\text{A}$, $V_{GS}=0\text{V}$
	IRF532/IRFP132 IRF533/IRFP133	—	—	2.3	V	$T_C=25^\circ\text{C}$, $I_S=12\text{A}$, $V_{GS}=0\text{V}$
t_{rr}	Reverse Recovery Time	—	120	250	ns	$T_J=25^\circ\text{C}$, $I_F=14\text{A}$, $dI_F/dt=100\text{A}/\mu\text{S}$

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
 (3) Repetitive rating: Pulse with limited by max. junction temperature









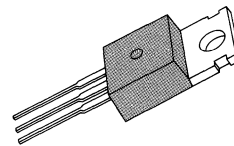
FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

PRODUCT SUMMARY

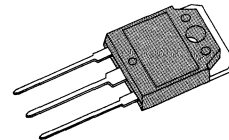
Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF540/IRFP140	100V	0.077Ω	28A
IRF541/IRFP141	80V	0.077Ω	28A
IRF542/IRFP142	100V	0.10Ω	25A
IRF543/IRFP143	80V	0.10Ω	25A

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IRF540/541/542/543

TO-3P



IRFP140/141/142/143

MAXIMUM RATINGS

Characteristics	Symbol	IRF540 IRFP140	IRF541 IRFP141	IRF542 IRFP142	IRF543 IRFP143	Unit
Drain-Source Voltage (1)	V_{DSS}	100	80	100	80	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	100	80	100	80	Vdc
Gate-Source Voltage	V_{GS}	± 20				Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	28	28	25	25	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	20	20	17	17	Adc
Drain Current—Pulsed (3)	I_{DM}	110	110	100	100	Adc
Gate Current—Pulsed	I_{GM}	± 1.5				Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	230				mJ
Avalanche Current	I_{AS}	28				A
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	125 1.0				Watts W/ $^\circ C$
Operating and Storage Junction to Case	T_J, T_{stg}	-55 to 150				$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300				$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=0.44 mH$, $V_{dd}=25V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-Source Breakdown Voltage IRF540/IRFP140 IRF542/IRFP142	100	—	—	V	V _{GS} =0V I _D =250μA
	IRF541/IRFP141 IRF543/IRFP143	80	—	—	V	
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} =V _{GS} , I _D =250μA
I _{GSS}	Gate-Source Leakage Forward	—	—	100	nA	V _{GS} =20V
I _{GSS}	Gate-Source Leakage Reverse	—	—	−100	nA	V _{GS} =−20V
I _{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	V _{DS} =Max. Rating, V _{GS} =0V
		—	—	1000	μA	V _{DS} =Max. Rating×0.8, V _{GS} =0V, T _C =125°C
I _{D(on)}	On-State Drain-Source Current (2) IRF540/IRFP140 IRF541/IRFP141	28	—	—	A	V _{DS} ≥2.8V, V _{GS} =10V
	IRF542/IRFP142 IRF543/IRFP143	25	—	—	A	
R _{DS(on)}	Static Drain-Source On-State Resistance (2) IRF540/IRFP140 IRF541/IRFP141	—	0.06	0.077	Ω	V _{GS} =10V, I _D =17A
	IRF542/IRFP142 IRF543/IRFP143	—	0.08	0.10	Ω	
g _{fs}	Forward Transconductance (2)	8.7	13	—	∅	V _{DS} ≥50V, I _D =17A
C _{iss}	Input Capacitance	—	1500	—	pF	V _{GS} =0V, V _{DS} =25V, f=1.0MHz
C _{oss}	Output Capacitance	—	500	—	pF	
C _{rss}	Reverse Transfer Capacitance	—	90	—	pF	
t _{d(on)}	Turn-On Delay Time	—	15	23	ns	V _{DD} =0.5BV _{DSS} , I _D =17A, Z _O =9.1Ω (MOSFET switching times are essentially independent of operating temperature)
t _r	Rise Time	—	72	110	ns	
t _{d(off)}	Turn-Off Delay Time	—	40	60	ns	
t _f	Fall Time	—	50	75	ns	
Q _g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	39	59	nC	V _{GS} =10V, I _D =28A, V _{DS} =0.8 Max. Rating (Gate charge is essentially independent of operating temperature.)
Q _{gs}	Gate-Source Charge	—	7.8	12	nC	
Q _{gd}	Gate-Drain ("Miller") Charge	—	19	38	nC	

THERMAL RESISTANCE

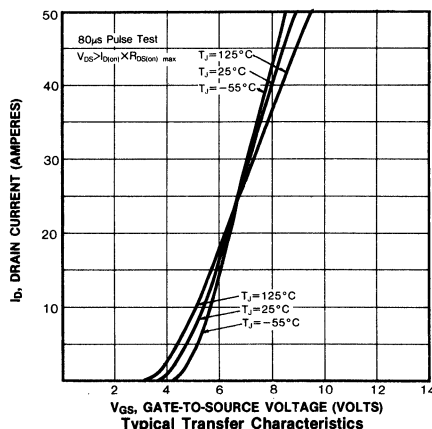
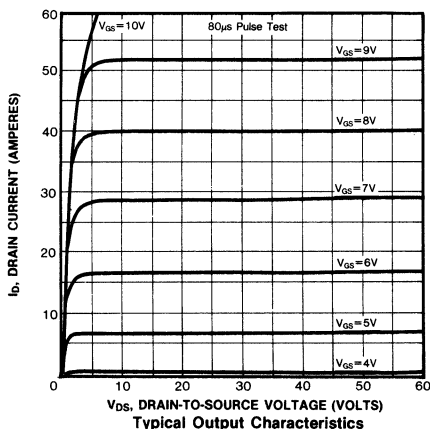
Symbol	Characteristic		IRF540-3	IRFP140-3	Unit	
R _{thJC}	Junction-to-Case	MAX	1.0	1.0	K/W	
R _{thCS}	Case-to-Sink	TYP	0.5	0.24	K/W	Mounting surface flat, smooth, and greased
R _{thJA}	Junction-to-Ambient	MAX	80	40	K/W	Free Air Operation

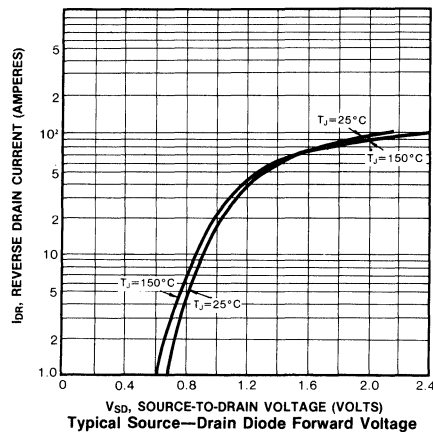
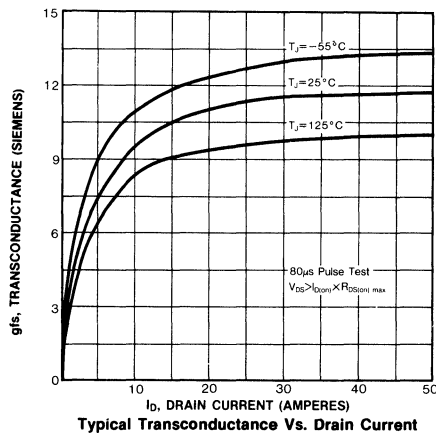
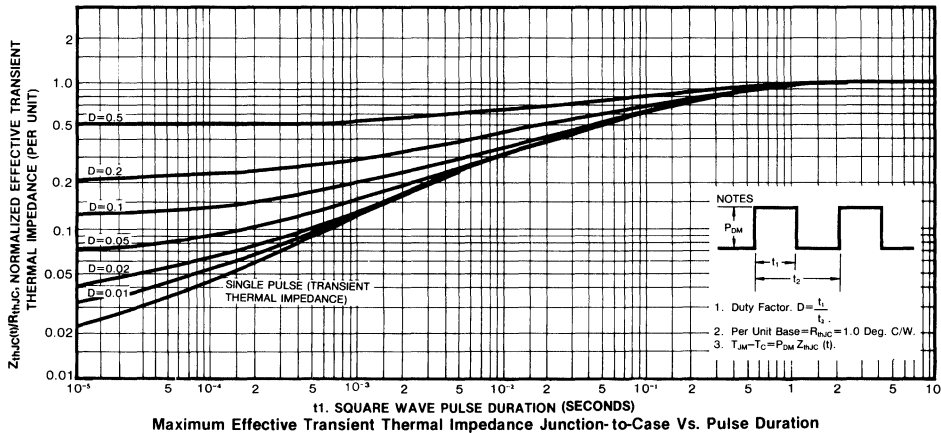
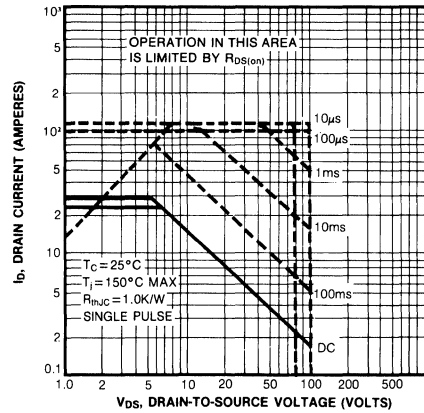
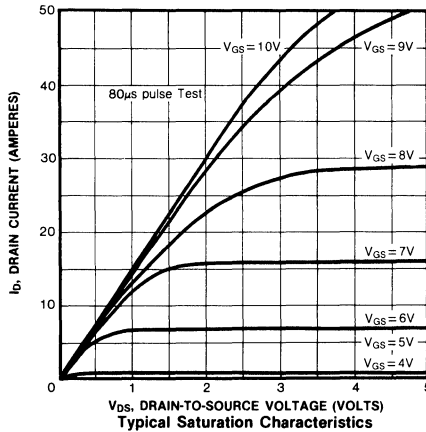
Notes: (1) T_J=25°C to 150°C
(2) Pulse test: Pulse width≤300μs, Duty Cycle≤2%
(3) Repetitive rating: Pulse width limited by max. junction temperature

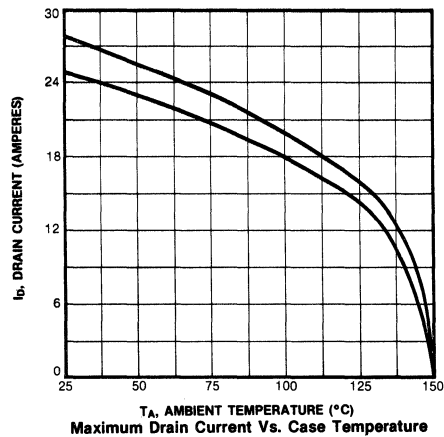
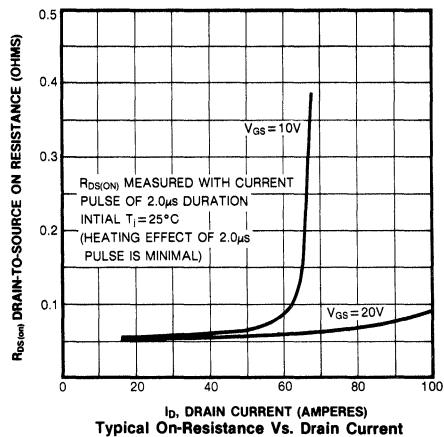
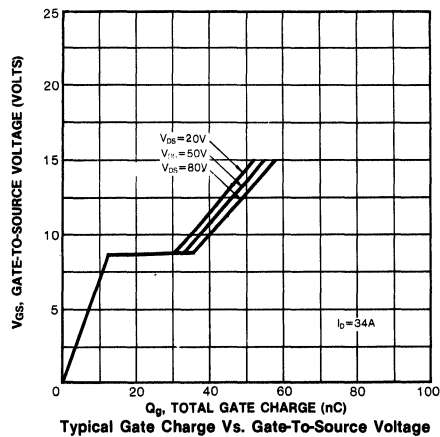
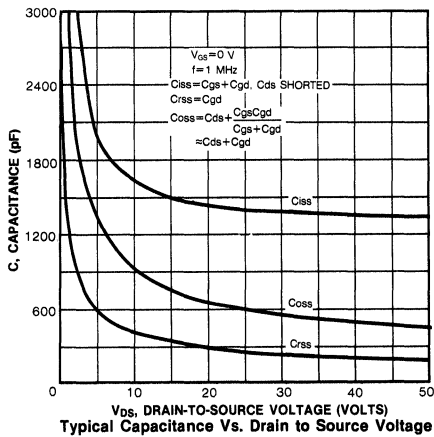
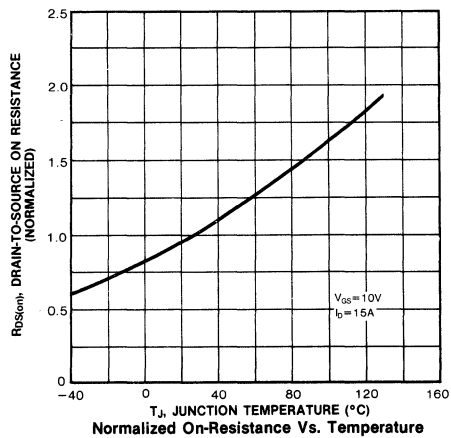
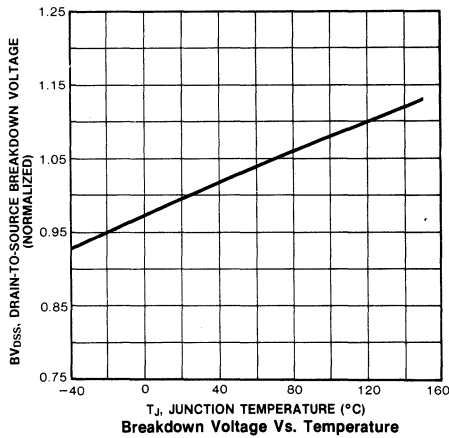
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

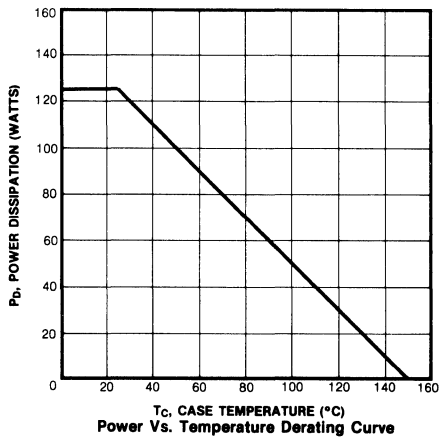
Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode) IRF540/IRFP140 IRF541/IRFP141	—	—	28	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier 
	IRF542/IRFP142 IRF543/IRFP143	—	—	25	A	
I_{SM}	Pulse Source Current(Body Diode)(3) IRF540/IRFP140 IRF541/IRFP141	—	—	110	A	
	IRF542/IRFP142 IRF543/IRFP143	—	—	100	A	
V_{SD}	Diode Forward Voltage (2) IRF540/IRFP140 IRF541/IRFP141	—	—	2.5	V	$T_C=25^\circ\text{C}$, $I_S=28\text{A}$, $V_{GS}=0\text{V}$
	IRF542/IRFP142 IRF543/IRFP143	—	—	2.3	V	$T_C=25^\circ\text{C}$, $I_S=25\text{A}$, $V_{GS}=0\text{V}$
t_{rr}	Reverse Recovery Time	—	150	300	ns	$T_J=25^\circ\text{C}$, $I_F=28\text{A}$, $dI_F/dt=100\text{A}/\mu\text{S}$

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
 (3) Repetitive rating: Pulse with limited by max. junction temperature









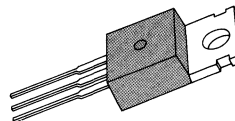
FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF610	200V	1.5Ω	3.3A
IRF611	150V	1.5Ω	3.3A
IRF612	200V	2.4Ω	2.6A
IRF613	150V	2.4Ω	2.6A

TO-220



IRF610/611/612/613

MAXIMUM RATINGS

Characteristic	Symbol	IRF610	IRF611	IRF612	IRF613	Unit
Drain-Source Voltage (1)	V_{DS}	200	150	200	150	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	200	150	200	150	Vdc
Gate-Source Voltage	V_{GS}	± 20				Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	3.3	3.3	2.6	2.6	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	2.1	2.1	1.6	1.6	Adc
Drain Current—Pulsed (3)	I_{DM}	8	8	6.5	6.5	Adc
Gate Current—Pulsed	I_{GM}	± 1.5				Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	46				mJ
Avalanche Current	I_{AS}	3.3				A
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	43 0.34				Watts W/ $^\circ C$
Operating and Storage Junction to Case	T_J, T_{stg}	-55 to 150				$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300				$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=6.4 mH$, $V_{dd}=50V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-Source Breakdown Voltage IRF610/612	200	—	—	V	V _{GS} =0V
	IRF611/613	150	—	—	V	I _D =250μA
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} =V _{GS} , I _D =250μA
I _{GSS}	Gate-Source Leakage Forward	—	—	100	nA	V _{GS} =20V
I _{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	V _{GS} =-20V
I _{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	V _{DS} =Max. Rating, V _{GS} =0V
		—	—	1000	μA	V _{DS} =Max. Rating×0.8, V _{GS} =0V, T _C =125°C
I _{D(on)}	On-State Drain-Source Current (2) IRF610/611	3.3	—	—	A	V _{DS} ≥7.9V, V _{GS} =10V
	IRF612/613	2.6	—	—	A	
R _{DS(on)}	Static Drain-Source On-State Resistance (2) IRF610/611	—	1.2	1.5	Ω	V _{GS} =10V, I _D =1.6A
	IRF612/613	—	1.5	2.4	Ω	
g _{fs}	Forward Transconductance (2)	0.8	1.4	—	∅	V _{DS} ≥50V, I _D =1.6A
C _{iss}	Input Capacitance	—	180	—	pF	V _{GS} =0V, V _{DS} =25V, f=1.0MHz
C _{oss}	Output Capacitance	—	56	—	pF	
C _{rss}	Reverse Transfer Capacitance	—	22	—	pF	
t _{d(on)}	Turn-On Delay Time	—	8.2	12	ns	V _{DD} =0.5BV _{DSS} , I _D =3.3A, Z _O =50Ω (MOSFET switching times are essentially independent of operating temperature)
t _r	Rise Time	—	17	26	ns	
t _{d(off)}	Turn-Off Delay Time	—	14	21	ns	
t _f	Fall Time	—	8.9	13	ns	
Q _g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	5.5	8.2	nC	V _{GS} =10V, I _D =3.3A, V _{DS} =0.8 Max. Rating (Gate charge is essentially independent of operating temperature.)
Q _{gs}	Gate-Source Charge	—	1.2	1.8	nC	
Q _{gd}	Gate-Drain ("Miller") Charge	—	3.0	4.5	nC	

THERMAL RESISTANCE

R _{thJC}	Junction-to-Case	—	—	2.9	K/W	
R _{thCS}	Case-to-Sink	—	0.5	—	K/W	Mounting surface flat, smooth, and greased
R _{thJA}	Junction-to-Ambient	—	—	80	K/W	Free Air Operation

Notes: (1) T_J=25°C to 150°C

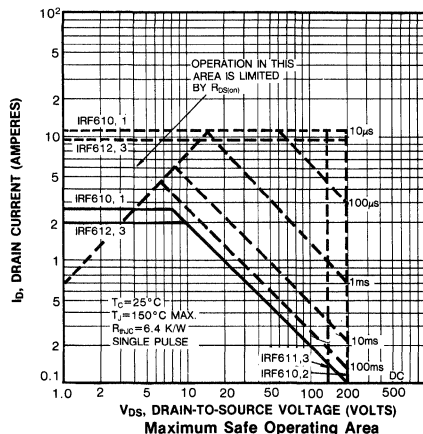
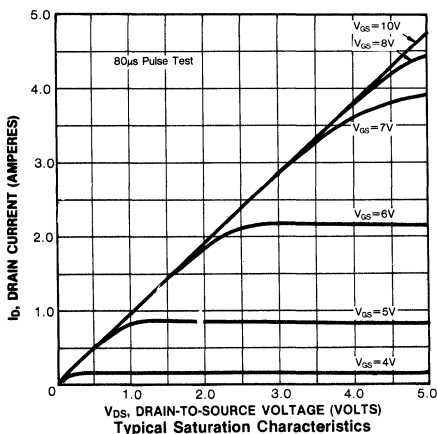
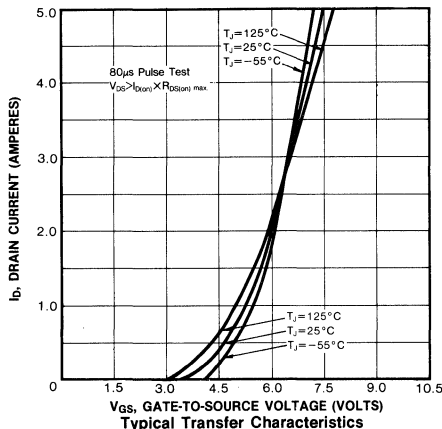
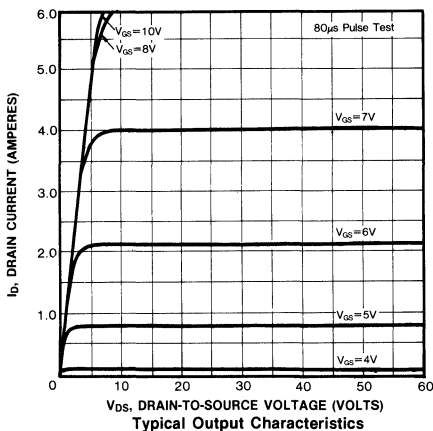
(2) Pulse test: Pulse width≤300μs, Duty Cycle≤2%

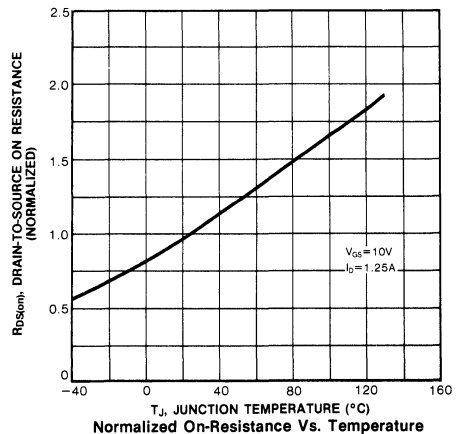
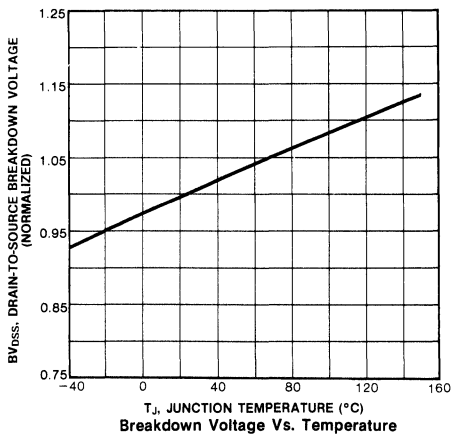
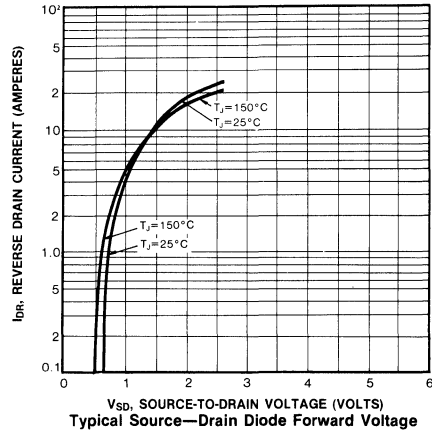
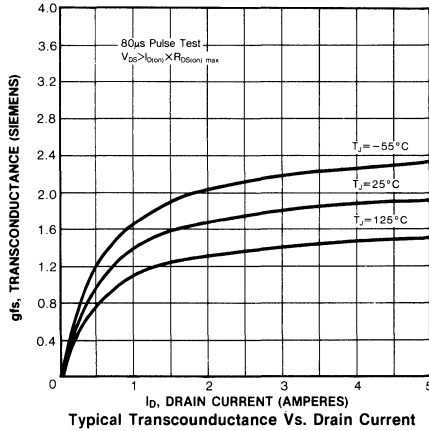
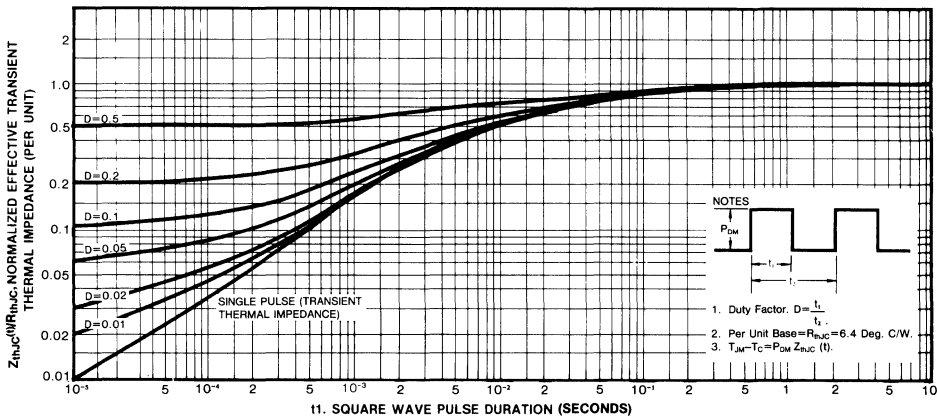
(3) Repetitive rating: Pulse width limited by max. junction temperature

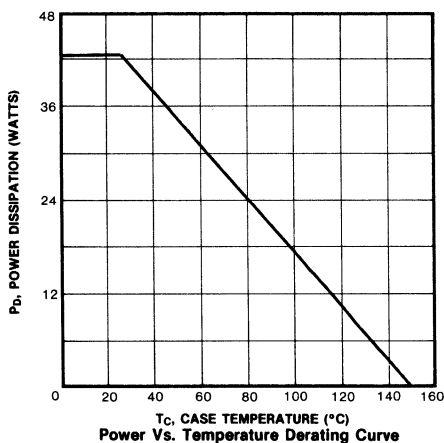
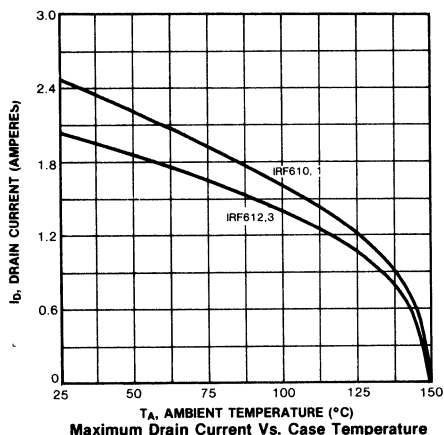
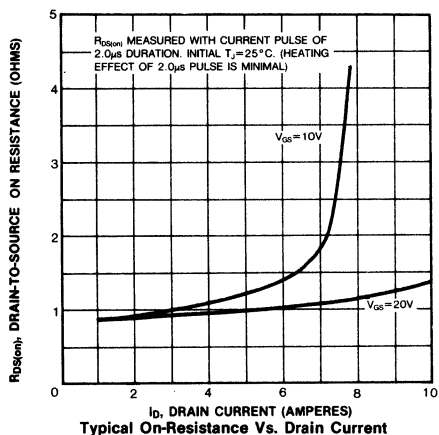
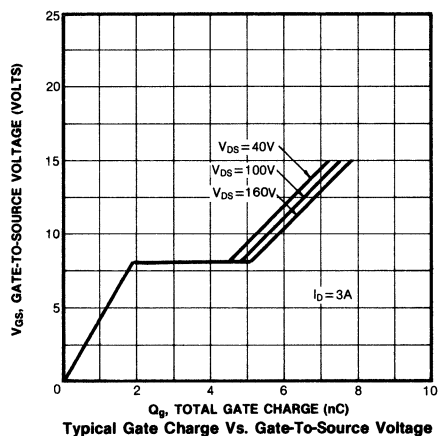
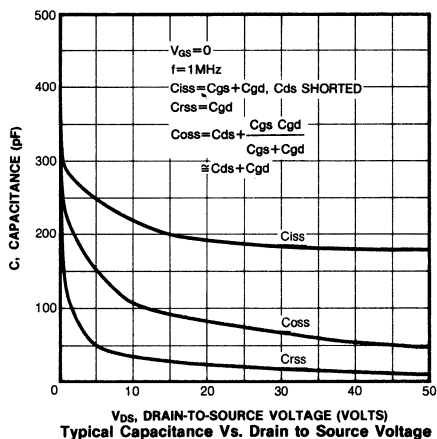
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic	Type	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	IRF610	—	—	3.3	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier 
		IRF611	—	—	2.6	A	
		IRF612	—	—	2.6	A	
I_{SM}	Pulse Source Current (Body Diode) (3)	IRF610	—	—	8.0	A	
		IRF611	—	—	6.5	A	
		IRF612	—	—	6.5	A	
V_{SD}	Diode Forward Voltage (2)	IRF610	—	—	2.5	V	$T_C=25^\circ\text{C}$, $I_S=3.3\text{A}$, $V_{GS}=0\text{V}$
		IRF611	—	—	2.0	V	$T_C=25^\circ\text{C}$, $I_S=2.6\text{A}$, $V_{GS}=0\text{V}$
		IRF612	—	—	2.0	V	$T_C=25^\circ\text{C}$, $I_S=2.6\text{A}$, $V_{GS}=0\text{V}$
t_{rr}	Reverse Recovery Time		—	150	310	ns	$T_J=25^\circ\text{C}$, $I_F=3.3\text{A}$, $dI_F/dt=100\text{A}/\mu\text{s}$

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
 (3) Repetitive rating: Pulse with limited by max. junction temperature

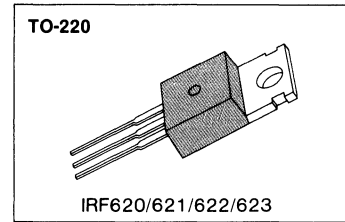






FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability



PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF620	200V	0.80Ω	5.0A
IRF621	150V	0.80Ω	5.0A
IRF622	200V	1.2Ω	4.0A
IRF623	150V	1.2Ω	4.0A

MAXIMUM RATINGS

Characteristics	Symbol	IRF620	IRF621	IRF622	IRF623	Unit
Drain-Source Voltage (1)	V_{DS}	200	150	200	150	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	200	150	200	150	Vdc
Gate-Source Voltage	V_{GS}	± 20				Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	5.0	5.0	4.0	4.0	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	3.0	3.0	16	16	Adc
Drain Current—Pulsed (3)	I_{DM}	20	20	16	16	Adc
Gate Current—Pulsed	I_{GM}	± 1.5				Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	85				mJ
Avalanche Current	I_{AS}	5.0				A
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	40 0.32				Watts W/ $^\circ C$
Operating and Storage Junction to Case	T_J, T_{stg}	-55 to 150				$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300				$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=5\text{ mH}$, $V_{dd}=50V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-Source Breakdown Voltage IRF620 IRF621	200	—	—	V	V _{GS} =0V I _D =250μA
	IRF622 IRF623	150	—	—	V	
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} =V _{GS} , I _D =250μA
I _{GSS}	Gate-Source Leakage Forward	—	—	100	nA	V _{GS} =20V
I _{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	V _{GS} =-20V
I _{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	V _{DS} =Max. Rating, V _{GS} =0V
		—	—	1000	μA	V _{DS} =Max. Rating×0.8, V _{GS} =0V, T _C =125°C
I _{D(on)}	On-State Drain-Source Current (2) IRF620 IRF621	5.0	—	—	A	V _{DS} ≥6V, V _{GS} =10V
	IRF622 IRF623	4.0	—	—	A	
R _{DS(on)}	Static Drain-Source On-State Resistance (2) IRF620 IRF621	—	0.4	0.8	Ω	V _{GS} =10V, I _D =2.5A
	IRF622 IRF623	—	0.8	1.2	Ω	
g _{fs}	Forward Transconductance (2)	1.3	2.8	—	Ω	V _{DS} ≥50V, I _D =2.5A
C _{iss}	Input Capacitance	—	450	—	pF	V _{GS} =0V, V _{DS} =25V, f=1.0MHz
C _{oss}	Output Capacitance	—	150	—	pF	
C _{rss}	Reverse Transfer Capacitance	—	50	—	pF	
t _{d(on)}	Turn-On Delay Time	—	20	40	ns	V _{DD} =0.5BV _{DSS} , I _D =2.5A, Z _O =50Ω (MOSFET switching times are essentially independent of operating temperature)
t _r	Rise Time	—	30	60	ns	
t _{d(off)}	Turn-Off Delay Time	—	50	100	ns	
t _f	Fall Time	—	30	60	ns	
Q _g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	12.5	15	nC	V _{GS} =10V, I _D =6.0A, V _{DS} =0.8 Max. Rating (Gate charge is essentially independent of operating temperature.)
Q _{gs}	Gate-Source Charge	—	4.0	—	nC	
Q _{gd}	Gate-Drain ("Miller") Charge	—	8.5	—	nC	

THERMAL RESISTANCE

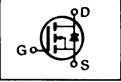
Symbol	Characteristic		IRF620-3	Unit	
R _{thJC}	Junction-to-Case	MAX	3.12	K/W	
R _{thCS}	Case-to-Sink	TYP	0.5	K/W	Mounting surface flat, smooth, and greased
R _{thJA}	Junction-to-Ambient	MAX	80	K/W	Free Air Operation

Notes: (1) T_J=25°C to 150°C

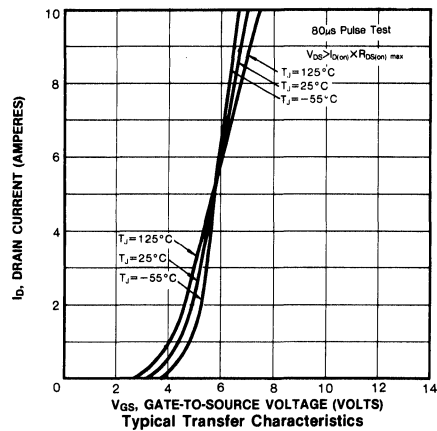
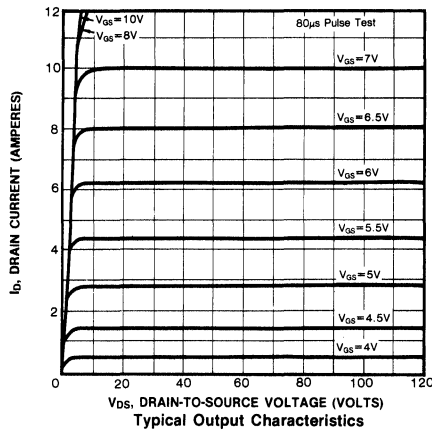
(2) Pulse test: Pulse width≤300μs, Duty Cycle≤2%

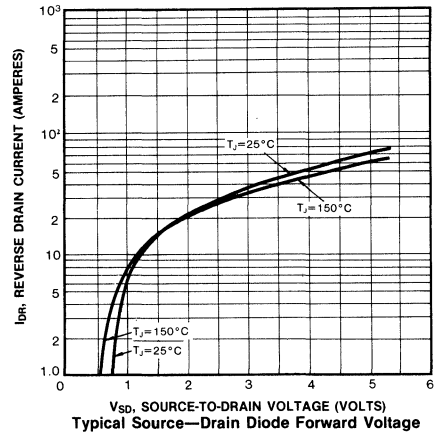
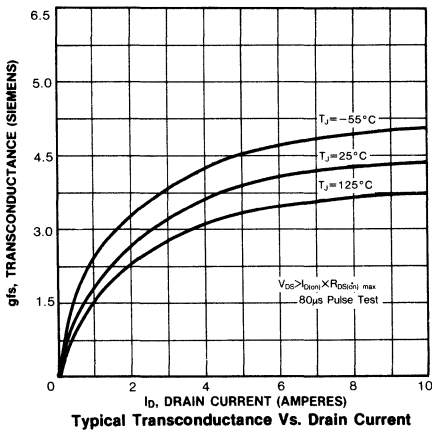
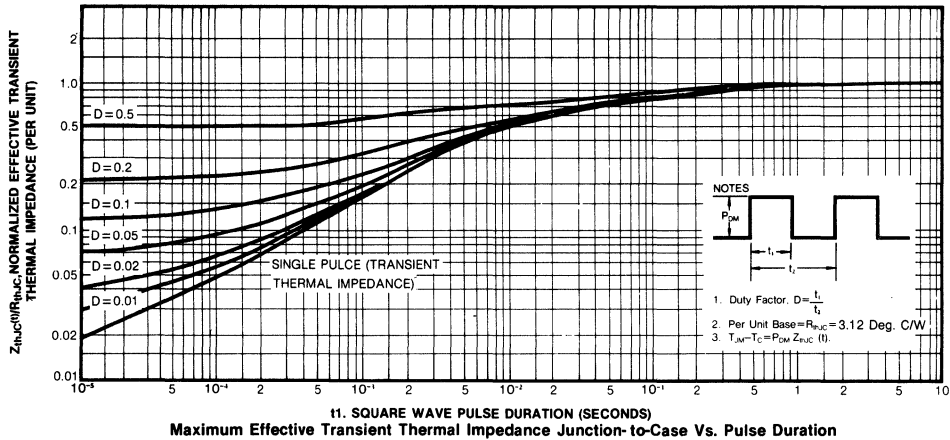
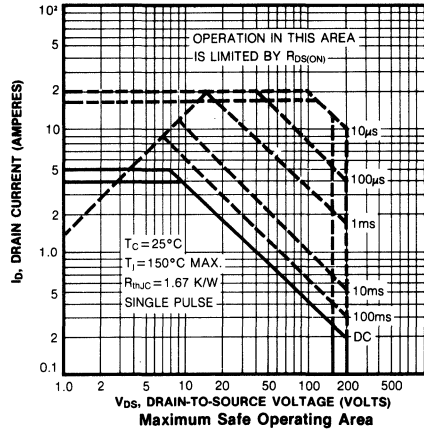
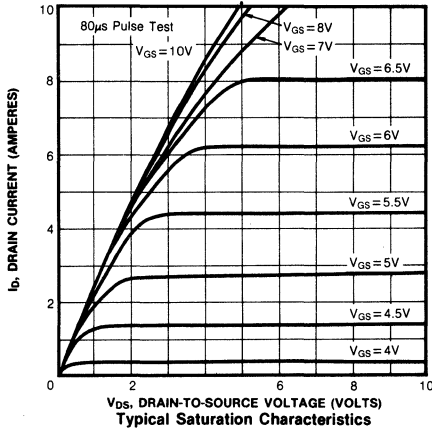
(3) Repetitive rating: Pulse width limited by max. junction temperature

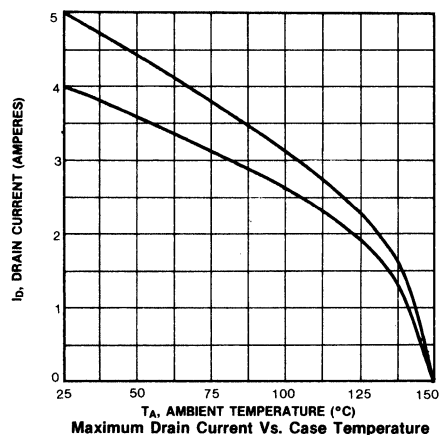
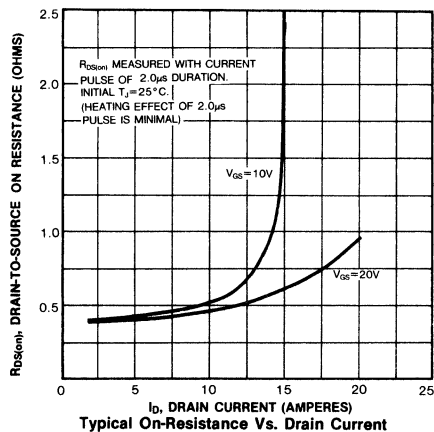
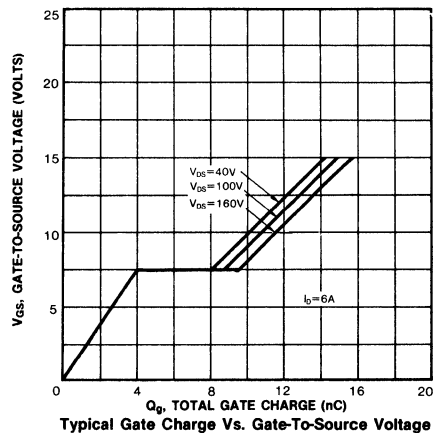
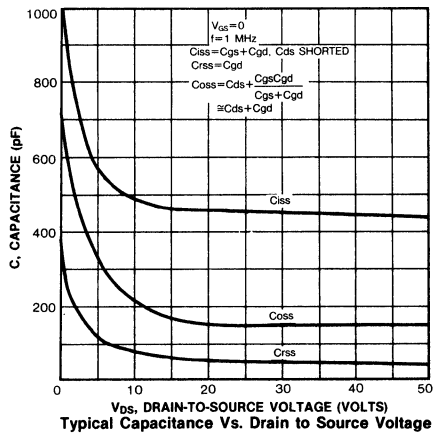
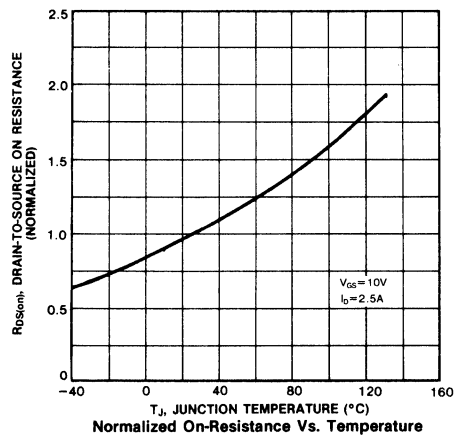
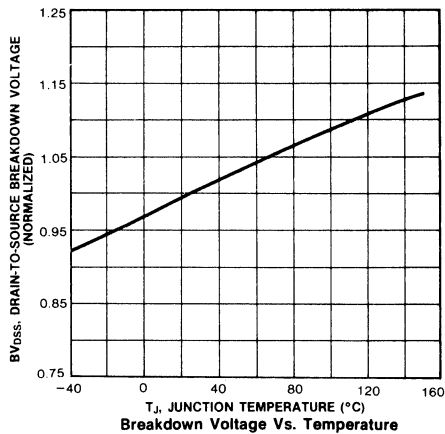
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

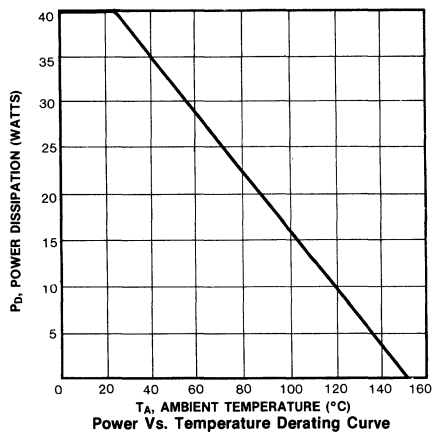
Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode) IRF620 IRF621	—	—	5.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier 
	IRF622 IRF623	—	—	4.0	A	
I_{SM}	Pulse Source Current(Body Diode)(3) IRF620 IRF621	—	—	20	A	
	IRF622 IRF623	—	—	16	A	
V_{SD}	Diode Forward Voltage (2) IRF620 IRF621	—	—	1.8	V	$T_C=25^\circ\text{C}$, $I_S=5.0\text{A}$, $V_{GS}=0\text{V}$
	IRF622 IRF623	—	—	1.6	V	$T_C=25^\circ\text{C}$, $I_S=4.0\text{A}$, $V_{GS}=0\text{V}$
t_{rr}	Reverse Recovery Time	—	350	—	ns	$T_J=150^\circ\text{C}$, $I_F=5.0\text{A}$, $dI_F/dt=100\text{A}/\mu\text{S}$

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
 (3) Repetitive rating: Pulse with limited by max. junction temperature





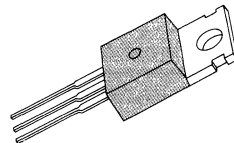




FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

TO-220



IRF624/625

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF624	250V	1.1 Ω	3.8A
IRF625	250V	1.5 Ω	3.3A

MAXIMUM RATINGS

Characteristic	Symbol	IRF624	IRF625	Unit
Drain-Source Voltage (1)	V_{DS}	250	250	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	250	250	Vdc
Gate-Source Voltage	V_{GS}	± 20		Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	3.8	3.3	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	2.4	2.1	Adc
Drain Current—Pulsed (3)	I_{DM}	15	13	Adc
Gate Current—Pulsed	I_{GM}	± 1.5		Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	110		mJ
Avalanche Current	I_{AS}	3.8		A
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	40 0.32		Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300		$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=12\text{ mH}$, $V_{dd}=50V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$ unless otherwise specified)

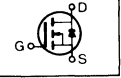
Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage	250	—	—	V	$V_{GS}=0V$ $I_D=250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}$, $I_D=250\mu A$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS}=20V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	$V_{GS}=-20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS}=\text{Max. Rating}$, $V_{GS}=0V$
		—	—	1000	μA	$V_{DS}=\text{Max. Rating} \times 0.8$, $V_{GS}=0V$, $T_C=125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2) IRF624	3.8	—	—	A	$V_{DS} \geq 5.7V$, $V_{GS}=10V$
	IRF625	3.3	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance (2) IRF624	—	—	1.1	Ω	$V_{GS}=10V$, $I_D=2.1A$
	IRF625	—	—	1.5	Ω	
g_{fs}	Forward Transconductance (2)	1.4	2.1	—	S	$V_{DS} \geq 50V$, $I_D=1.9A$
C_{iss}	Input Capacitance	—	390	—	pF	$V_{GS}=0V$, $V_{DS}=25V$, $f=1.0\text{MHz}$
C_{oss}	Output Capacitance	—	150	—	pF	
C_{rss}	Reverse Transfer Capacitance	—	50	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	11	17	ns	$V_{DD}=0.5BV_{DSS}$, $I_D=3.8A$, $Z_\theta=18\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	24	36	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	21	32	ns	
t_f	Fall Time	—	13	20	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	15	22	nC	$V_{GS}=10V$, $I_D=3.8A$, $V_{DS}=0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	4.0	6.0	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	7.2	11	nC	

THERMAL RESISTANCE

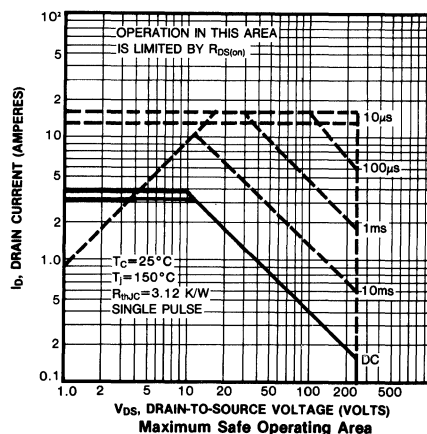
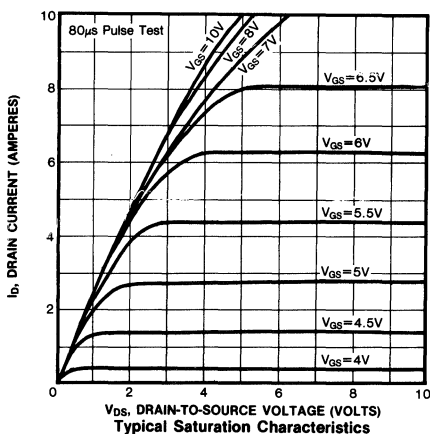
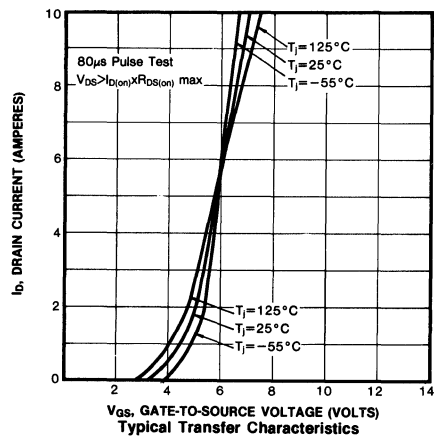
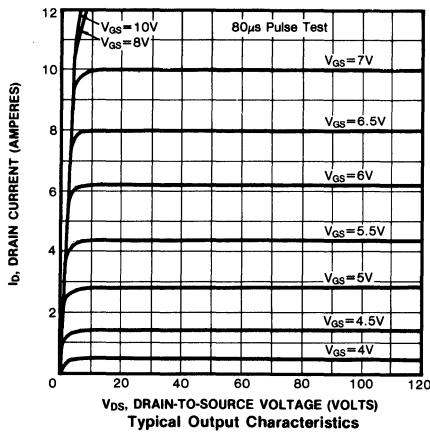
R_{thJC}	Junction-to-Case	—	—	3.12	K/W	
R_{thCS}	Case-to-Sink	—	1.0	—	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	—	—	80	K/W	Free Air Operation

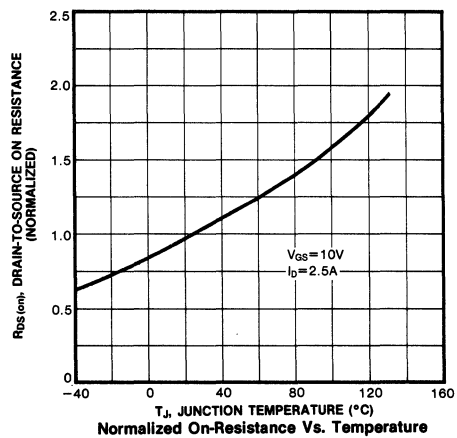
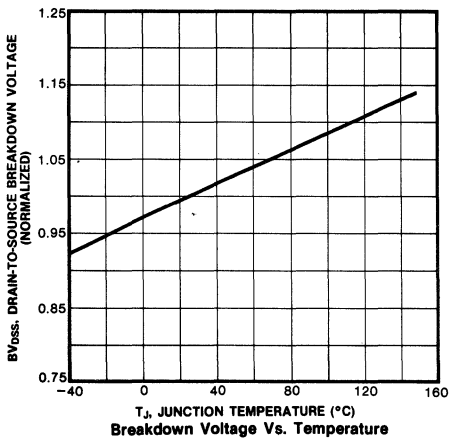
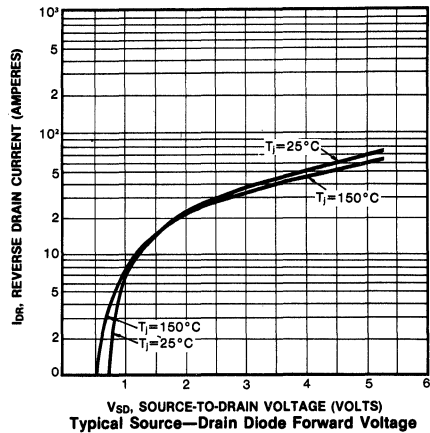
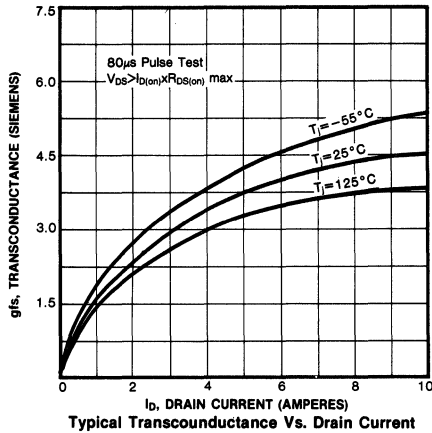
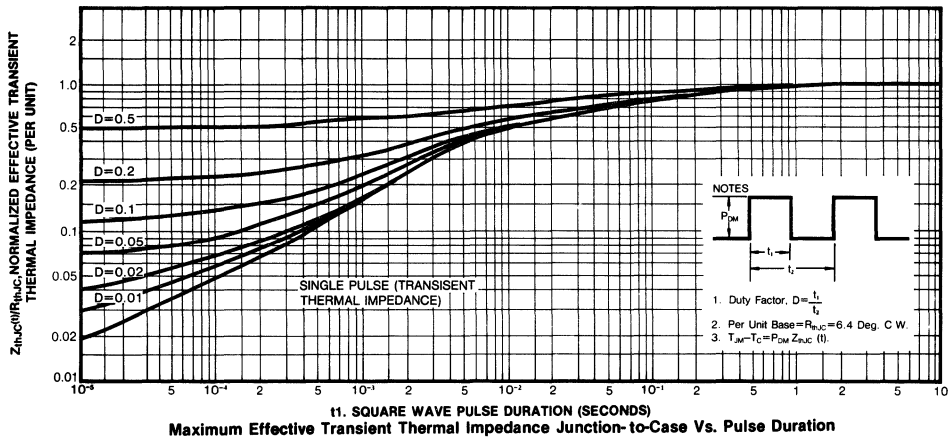
- Notes:** (1) $T_J=25^\circ\text{C}$ to 150°C
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse width limited by max. junction temperature

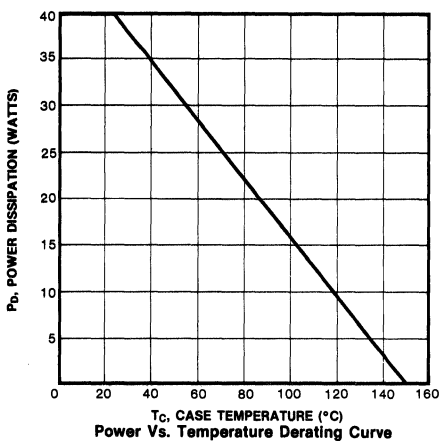
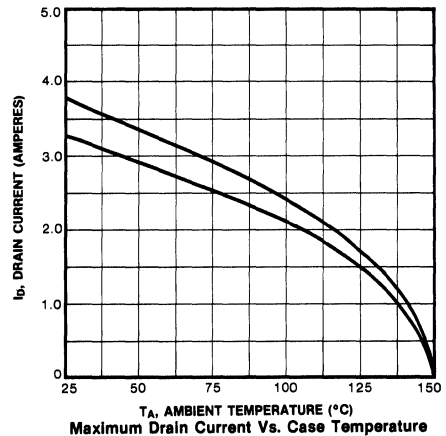
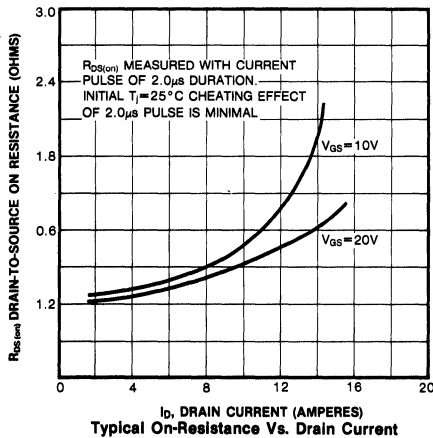
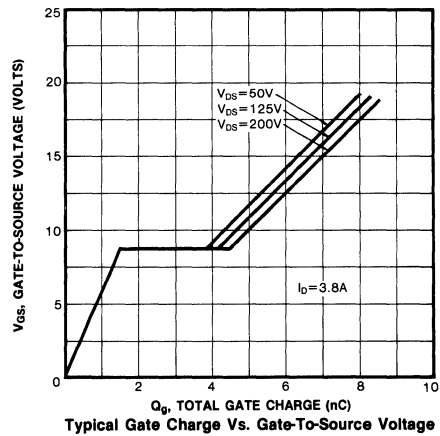
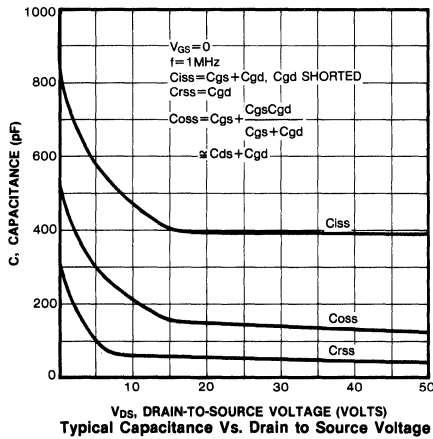
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic	Type	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	IRF624	—	—	3.8	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier 
		IRF625	—	—	3.3	V	
I_{SM}	Pulse Source Current (Body Diode) (3)	IRF624	—	—	15	A	
		IRF625	—	—	13	V	
V_{SD}	Diode Forward Voltage (2)		—	—	1.8	V	$T_C = 25^\circ\text{C}$, $I_S = 3.8\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time		—	180	—	ns	$T_J = 25^\circ\text{C}$, $I_F = 3.8\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{s}$

Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature







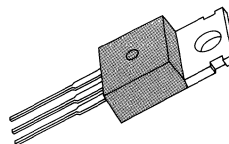
FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

PRODUCT SUMMARY

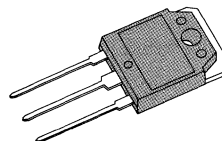
Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF630/IRFP230	200V	0.4Ω	9.0A
IRF631/IRFP231	150V	0.4Ω	9.0A
IRF632/IRFP232	200V	0.4Ω	8.0A
IRF633/IRFP233	150V	0.6Ω	8.0A

TO-220



IRF630/631/632/633

TO-3P



IRFP230/231/232/233

MAXIMUM RATINGS

Characteristics	Symbol	IRF630 IRFP230	IRF631 IRFP231	IRF632 IRFP232	IRF633 IRFP233	Unit
Drain-Source Voltage (1)	V_{DS}	200	150	200	150	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	200	150	200	150	Vdc
Gate-Source Voltage	V_{GS}	± 20				Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	9.0	9.0	8.0	8.0	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	6.0	6.0	5.0	5.0	Adc
Drain Current—Pulsed (3)	I_{DM}	36	36	32	32	Adc
Gate Current—Pulsed	I_{GM}	± 1.5				Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	170				mJ
Avalanche Current	I_{AS}	9.0				A
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	75 0.6				Watts W/ $^\circ C$
Operating and Storage Junction to Case	T_J, T_{stg}	-55 to 150				$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300				$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=4\text{ mH}$, $V_{dd}=50V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage IRF630/IRFP230 IRF632/IRFP232	200	—	—	V	$V_{GS}=0V$ $I_D=250\mu A$
	IRF631/IRFP231 IRF633/IRFP233	150	—	—	V	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}$, $I_D=250\mu A$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS}=20V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	$V_{GS}=-20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS}=\text{Max. Rating}$, $V_{GS}=0V$
		—	—	1000	μA	$V_{DS}=\text{Max. Rating} \times 0.8$, $V_{GS}=0V$, $T_C=125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2) IRF630/IRFP230 IRF631/IRFP231	9.0	—	—	A	$V_{DS} \geq 5.4V$, $V_{GS}=10V$
	IRF632/IRFP232 IRF633/IRFP233	8.0	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance (2) IRF630/IRFP230 IRF631/IRFP231	—	0.25	0.4	Ω	$V_{GS}=10V$, $I_D=5.0A$
	IRF632/IRFP232 IRF633/IRFP233	—	0.4	0.6	Ω	
g_{fs}	Forward Transconductance (2)	3.0	4.6	—	Ω	$V_{DS} \geq 50V$, $I_D=5.0A$
C_{iss}	Input Capacitance	—	750	—	pF	$V_{GS}=0V$, $V_{DS}=25V$, $f=1.0\text{MHz}$
C_{oss}	Output Capacitance	—	120	—	pF	
C_{rss}	Reverse Transfer Capacitance	—	45	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	—	30	ns	$V_{DD}=0.5BV_{DSS}$, $I_D=5.0A$, $Z_O=15\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	—	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	—	50	ns	
t_f	Fall Time	—	—	40	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	19	30	nC	$V_{GS}=10V$, $I_D=12A$, $V_{DS}=0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	50	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	14	—	nC	

THERMAL RESISTANCE

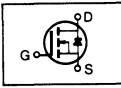
Symbol	Characteristic		IRF630-3	IRFP230-3	Unit	
R_{thJC}	Junction-to-Case	MAX	1.67	1.67	K/W	
R_{thCS}	Case-to-Sink	TYP	1.0	0.24	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	MAX	80	40	K/W	Free Air Operation

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C

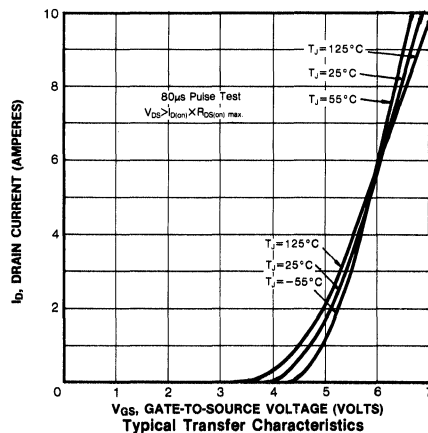
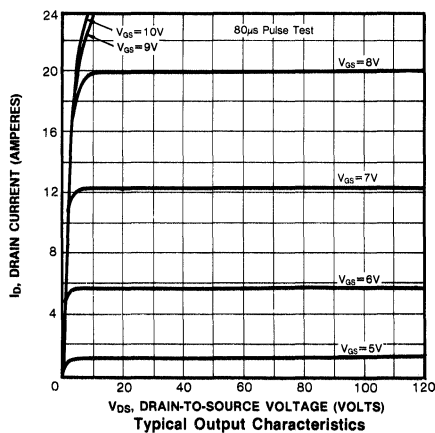
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

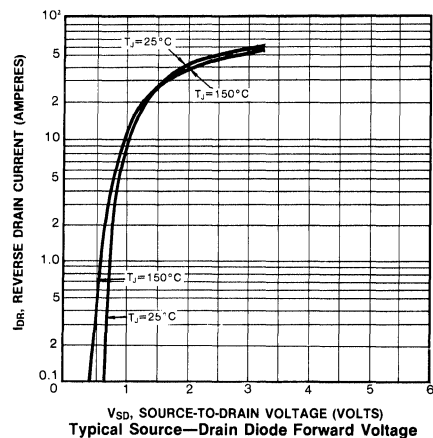
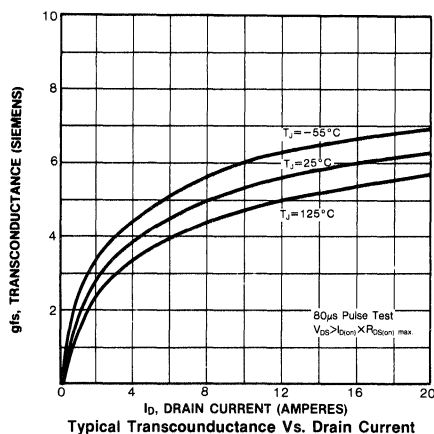
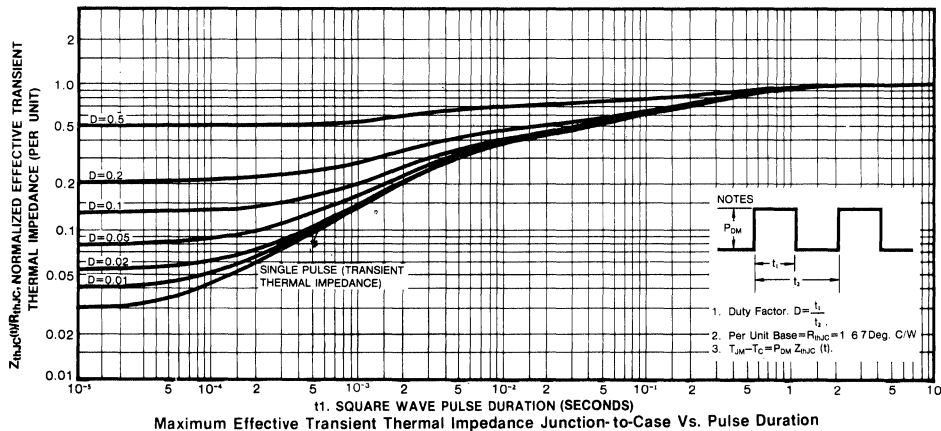
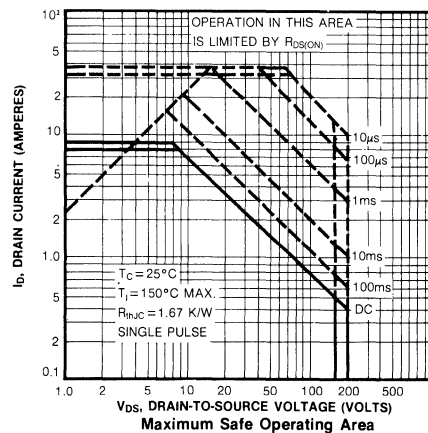
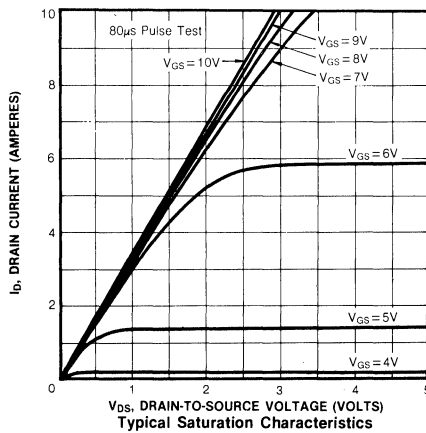
(3) Repetitive rating: Pulse width limited by max. junction temperature

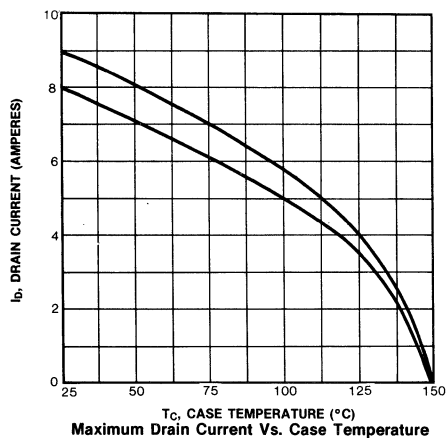
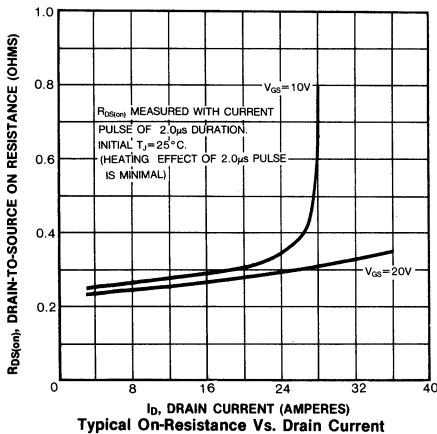
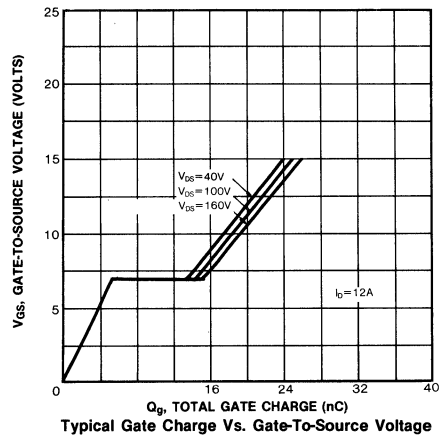
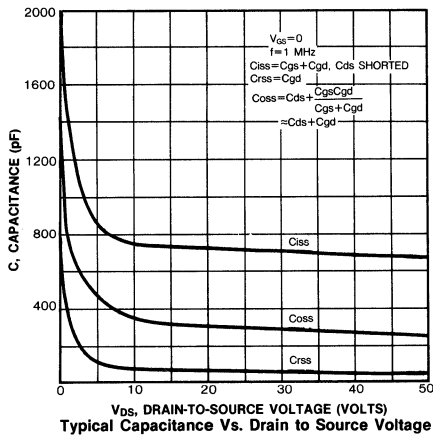
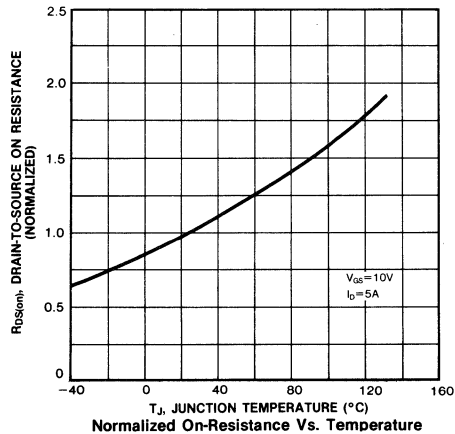
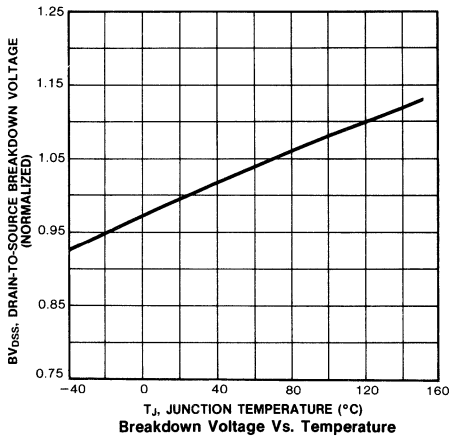
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

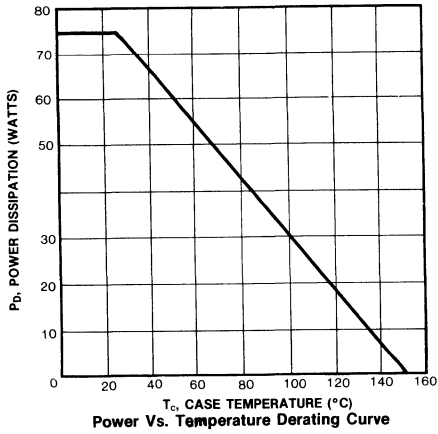
Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode) IRF630/IRFP230 IRF631/IRFP231	—	—	9.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier 
	IRF632/IRFP232 IRF633/IRFP233	—	—	8.0	A	
I_{SM}	Pulse Source Current(Body Diode)(3) IRF630/IRFP230 IRF631/IRFP231	—	—	36	A	
	IRF632/IRFP232 IRF633/IRFP233	—	—	32	A	
V_{SD}	Diode Forward Voltage (2) IRF630/IRFP230 IRF631/IRFP231	—	—	2.0	V	$T_C=25^\circ\text{C}$, $I_S=9.0\text{A}$, $V_{GS}=0\text{V}$
	IRF632/IRFP232 IRF633/IRFP233	—	—	1.8	V	$T_C=25^\circ\text{C}$, $I_S=8.0\text{A}$, $V_{GS}=0\text{V}$
t_{rr}	Reverse Recovery Time	—	450	—	ns	$T_J=150^\circ\text{C}$, $I_F=9.0\text{A}$, $dI_F/dt=100\text{A}/\mu\text{S}$

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
 (3) Repetitive rating: Pulse with limited by max. junction temperature







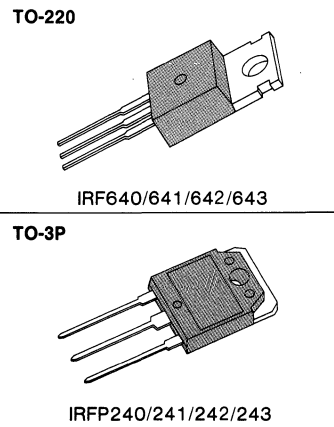


FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF640/IRFP140	200V	0.18 Ω	18A
IRF641/IRFP241	150V	0.18 Ω	18A
IRF642/IRFP242	200V	0.22 Ω	16A
IRF643/IRFP243	150V	0.22 Ω	16A



MAXIMUM RATINGS

Characteristics	Symbol	IRF640 IRFP240	IRF641 IRFP241	IRF642 IRFP242	IRF643 IRFP243	Unit
Drain-Source Voltage (1)	V_{DS}	200	150	200	150	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	200	150	200	150	Vdc
Gate-Source Voltage	V_{GS}	± 20				Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	18	18	16	16	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	11	11	10	10	Adc
Drain Current—Pulsed (3)	I_{DM}	72	72	64	64	Adc
Gate Current—Pulsed	I_{GM}	± 1.5				Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	580				mJ
Avalanche Current	I_{AS}	18				A
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	125 1.0				Watts W/ $^\circ C$
Operating and Storage Junction to Case	T_J, T_{stg}	-55 to 150				$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300				$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=2.7 mH$, $V_{dd}=50V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage IRF640/IRFP240 IRF642/IRFP242	200	—	—	V	$V_{GS}=0V$ $I_D=250\mu A$
	IRF641/IRFP241 IRF643/IRFP243	150	—	—	V	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}$, $I_D=250\mu A$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS}=20V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	$V_{GS}=-20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS}=\text{Max. Rating}$, $V_{GS}=0V$
		—	—	1000	μA	$V_{DS}=\text{Max. Rating} \times 0.8$, $V_{GS}=0V$, $T_C=125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2) IRF540/IRFP240 IRF541/IRFP241	18	—	—	A	$V_{DS} \geq 4.0V$, $V_{GS}=10V$
	IRF542/IRFP242 IRF543/IRFP243	16	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance (2) IRF640/IRFP240 IRF641/IRFP241	—	0.13	0.18	Ω	$V_{GS}=10V$, $I_D=10A$
	IRF642/IRFP242 IRF643/IRFP243	—	0.20	0.22	Ω	
g_{fs}	Forward Transconductance (2)	6.0	9.5	—	Ω	$V_{DS} \geq 50V$, $I_D=10A$
C_{iss}	Input Capacitance	—	1400	—	pF	$V_{GS}=0V$, $V_{DS}=25V$, $f=1.0\text{MHz}$
C_{oss}	Output Capacitance	—	240	—	pF	
C_{rss}	Reverse Transfer Capacitance	—	95	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	—	30	ns	$V_{DD}=0.5BV_{DSS}$, $I_D=10A$, $Z_O=4.7\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	—	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	—	80	ns	
t_f	Fall Time	—	—	60	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	44	60	nC	$V_{GS}=10V$, $I_D=22A$, $V_{DS}=0.8$ Max. Rating (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	?	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	35	—	nC	

THERMAL RESISTANCE

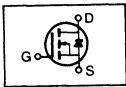
Symbol	Characteristic		IRF640-3	IRFP240-3	Unit	
R_{thJC}	Junction-to-Case	MAX	1.0	1.0	K/W	
R_{thCS}	Case-to-Sink	TYP	1.0	0.24	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	MAX	80	40	K/W	Free Air Operation

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C

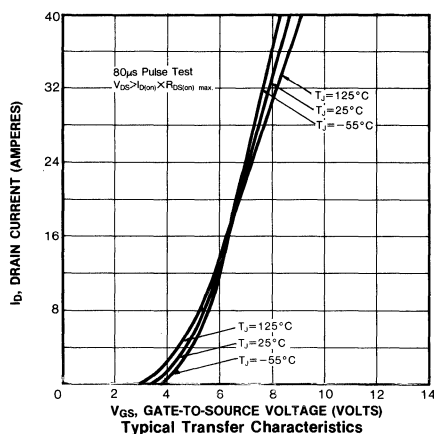
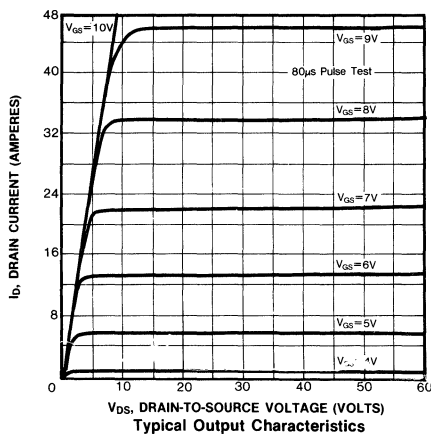
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

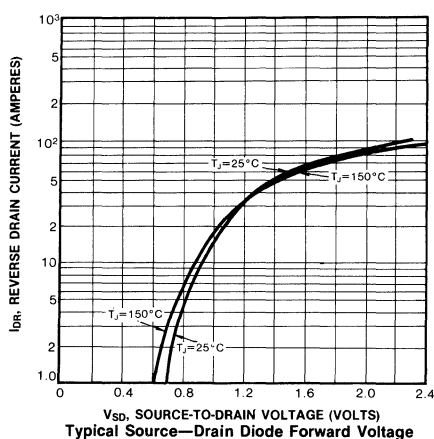
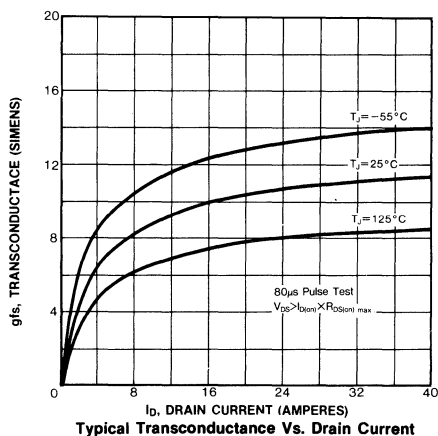
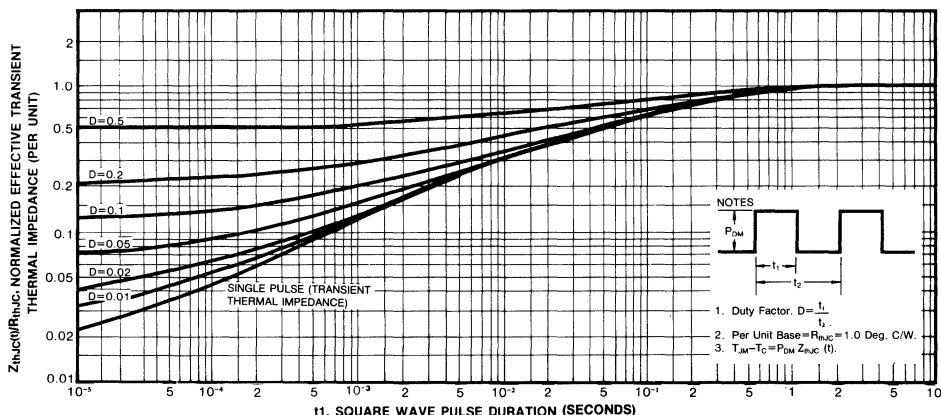
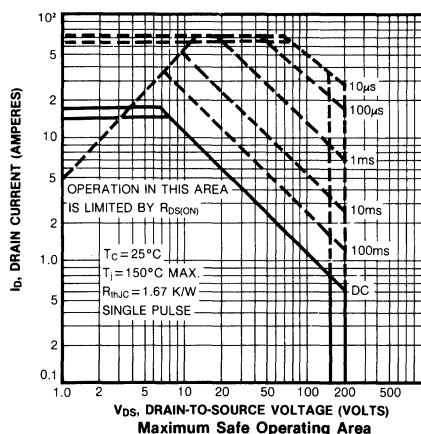
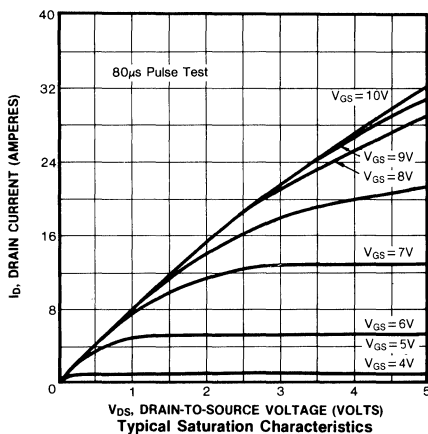
(3) Repetitive rating: Pulse width limited by max. junction temperature

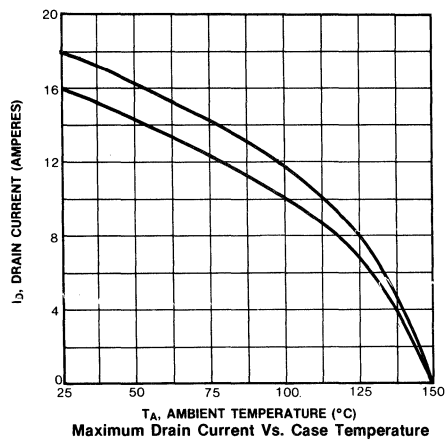
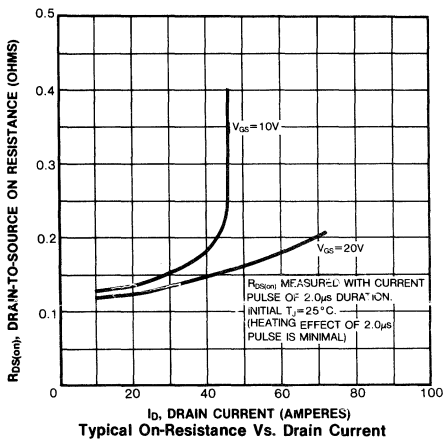
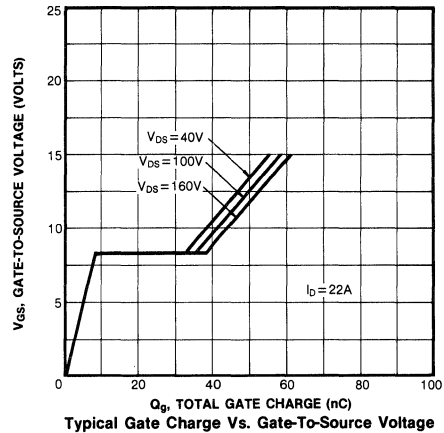
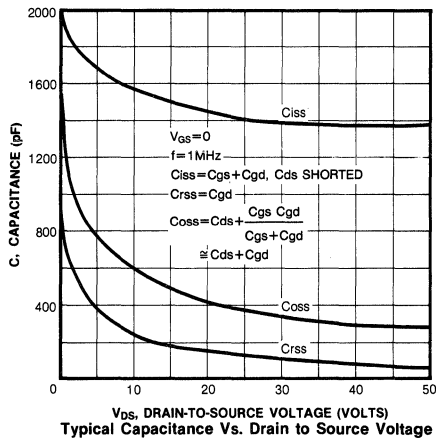
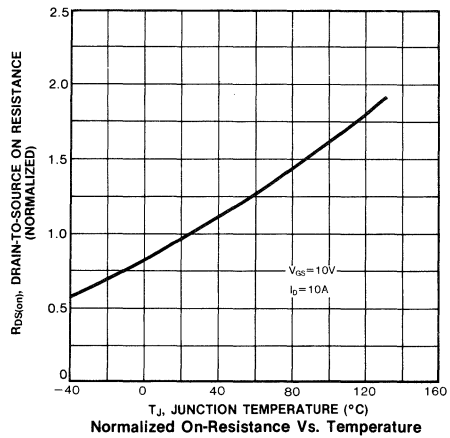
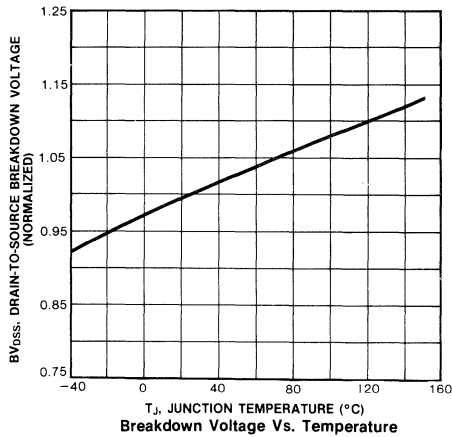
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

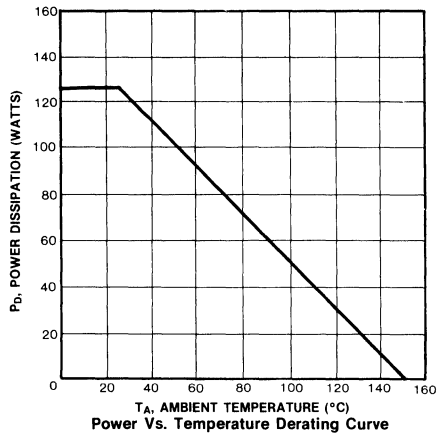
Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode) IRF640/IRFP240 IRF641/IRFP241	—	—	18	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier 
	IRF642/IRFP242 IRF643/IRFP243	—	—	16	A	
I_{SM}	Pulse Source Current(Body Diode)(3) IRF640/IRFP240 IRF641/IRFP241	—	—	72	A	
	IRF642/IRFP242 IRF643/IRFP243	—	—	64	A	
V_{SD}	Diode Forward Voltage (2) IRF640/IRFP240 IRF641/IRFP241	—	—	2.0	V	$T_C=25^\circ\text{C}$, $I_S=18\text{A}$, $V_{GS}=0\text{V}$
	IRF642/IRFP242 IRF643/IRFP243	—	—	1.9	V	$T_C=25^\circ\text{C}$, $I_S=16\text{A}$, $V_{GS}=0\text{V}$
t_{rr}	Reverse Recovery Time	—	650	—	ns	$T_J=25^\circ\text{C}$, $I_F=18\text{A}$, $dI_F/dt=100\text{A}/\mu\text{S}$

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature









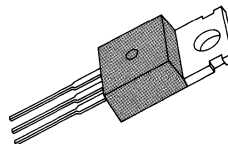
FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

PRODUCT SUMMARY

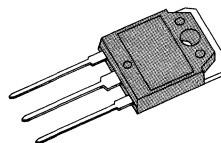
Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF644/IRFP244	250V	0.28 Ω	14A
IRF645/IRFP245	250V	0.34 Ω	13A

TO-220



IRF644/645

TO-3P



IRFP244/245

MAXIMUM RATINGS

Characteristic	Symbol	IRF644 IRFP244	IRF645 IRFP245	Unit
Drain-Source Voltage (1)	V_{DSS}	250	250	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	250	250	Vdc
Gate-Source Voltage	V_{GS}	± 20		Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	14	13	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	8.8	8.0	Adc
Drain Current—Pulsed (3)	I_{DM}	56	52	Adc
Gate Current—Pulsed	I_{GM}	± 1.5		Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	550		mJ
Avalanche Current	I_{AS}	15		A
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	125 1.0		Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300		$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=4 mH$, $V_{dd}=50V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage	250	—	—	V	$V_{GS}=0V$ $I_D=250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}$, $I_D=250\mu A$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS}=20V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	$V_{GS}=-20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS}=\text{Max. Rating}$, $V_{GS}=0V$
		—	—	1000	μA	$V_{DS}=\text{Max. Rating} \times 0.8$, $V_{GS}=0V$, $T_C=125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2) IRF644/IRFP244	14	—	—	A	$V_{DS} \geq 4.7V$, $V_{GS}=10V$
	IRF645/IRFP245	13	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance (2)	—	0.23	0.28	Ω	$V_{GS}=10V$, $I_D=8.0A$
		—	0.28	0.34	Ω	
g_{fs}	Forward Transconductance (2)	6.7	10.2	—	S	$V_{DS} \geq 50V$, $I_D=8.0A$
C_{iss}	Input Capacitance	—	1472	—	pF	$V_{GS}=0V$, $V_{DS}=25V$, $f=1.0\text{MHz}$
C_{oss}	Output Capacitance	—	190	—	pF	
C_{rss}	Reverse Transfer Capacitance	—	69	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	16	20	ns	$V_{DD}=0.5BV_{DSS}$, $I_D=14A$, $Z_O=9.1\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	67	100	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	53	80	ns	
t_f	Fall Time	—	49	74	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	39	59	nC	$V_{GS}=10V$, $I_D=14A$, $V_{DS}=0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	6.6	9.9	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	20	30	nC	

THERMAL RESISTANCE

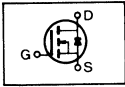
Symbol	Characteristic		IRF644-5	IRFP244-4	Unit	Test Conditions
R_{thJC}	Junction-to-Case	MAX	1.0	1.0	K/W	
R_{thCS}	Case-to-Sink	TYP	0.5	0.24	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	MAX	80	40	K/W	Free Air Operation

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C

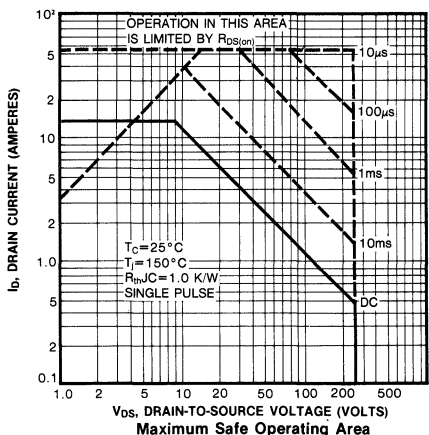
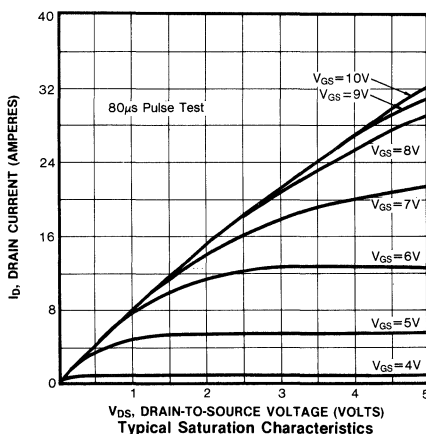
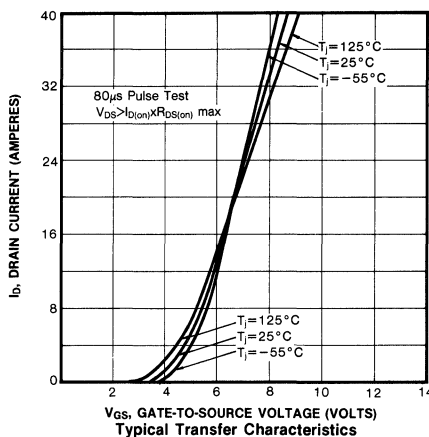
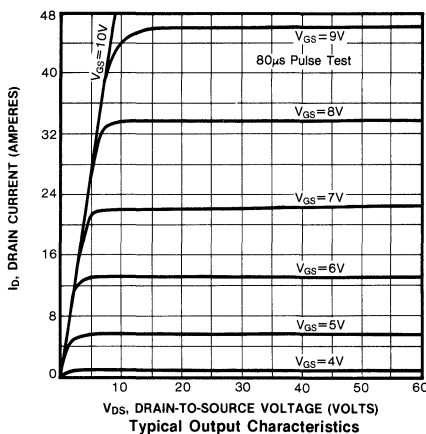
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

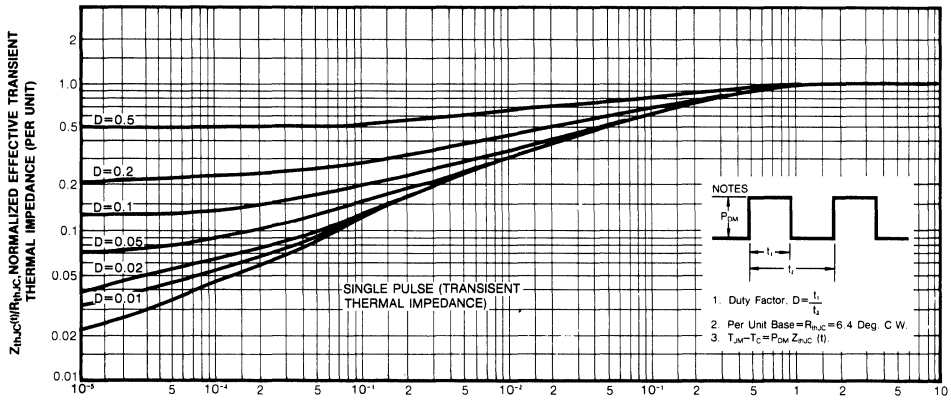
(3) Repetitive rating: Pulse width limited by max. junction temperature

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

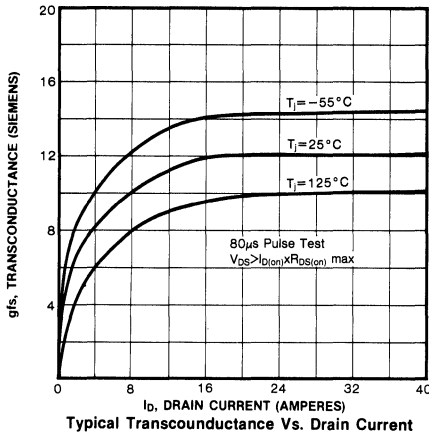
Symbol	Characteristic	Type	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	IRF644/ IRFP244	—	—	14	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier 
		IRF645/ IRFP245	—	—	13	V	
I_{SM}	Pulse Source Current (Body Diode) (3)	IRF644/ IRFP244	—	—	56	A	
		IRF645/ IRFP245	—	—	52	V	
V_{SD}	Diode Forward Voltage (2)		—	—	1.8	V	$T_C=25^\circ\text{C}$, $I_S=14\text{A}$, $V_{GS}=0\text{V}$
t_{rr}	Reverse Recovery Time		—	300	—	ns	$T_J=25^\circ\text{C}$, $I_F=14\text{A}$, $dI_F/dt=100\text{A}/\mu\text{s}$

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
 (3) Repetitive rating: Pulse with limited by max. junction temperature

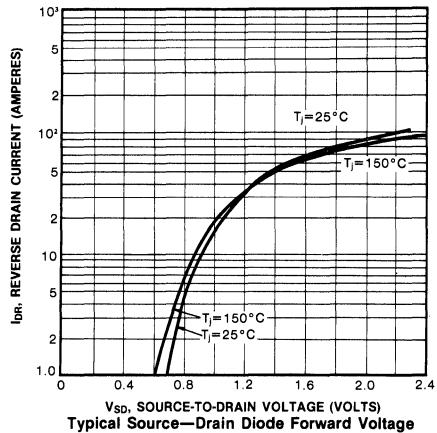




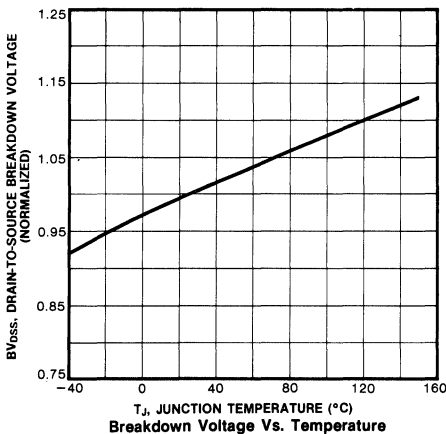
11. SQUARE WAVE PULSE DURATION (SECONDS)
Maximum Effective Transient Thermal Impedance Junction-to-Case Vs. Pulse Duration



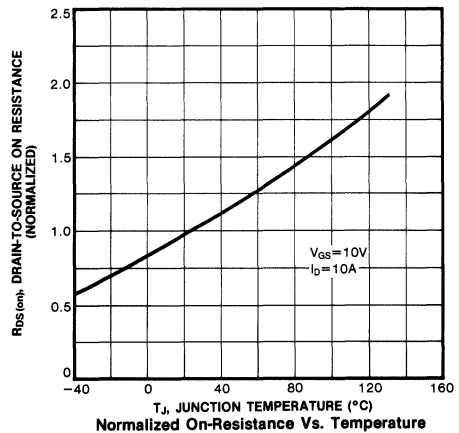
Typical Transconductance Vs. Drain Current



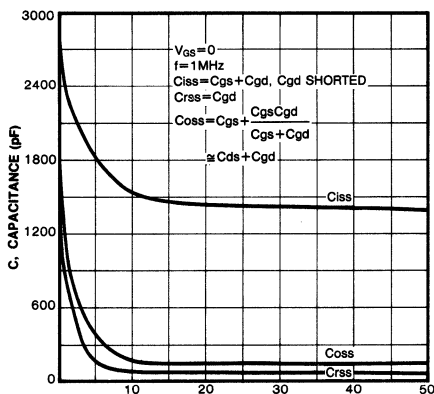
Typical Source-Drain Diode Forward Voltage



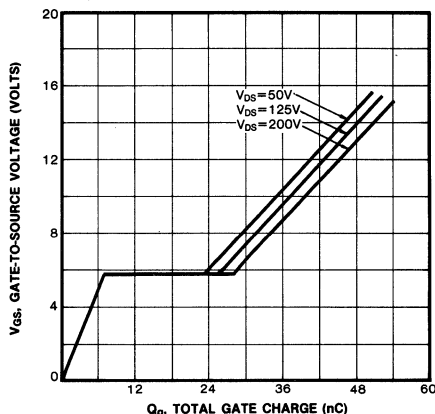
Breakdown Voltage Vs. Temperature



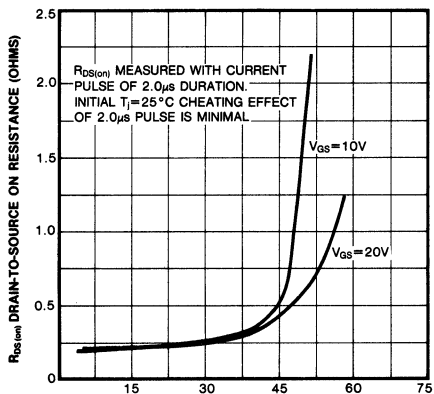
Normalized On-Resistance Vs. Temperature



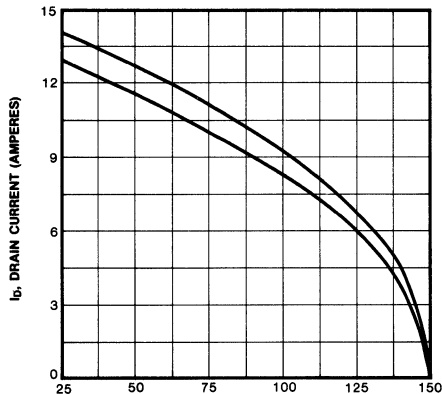
Typical Capacitance Vs. Drain to Source Voltage



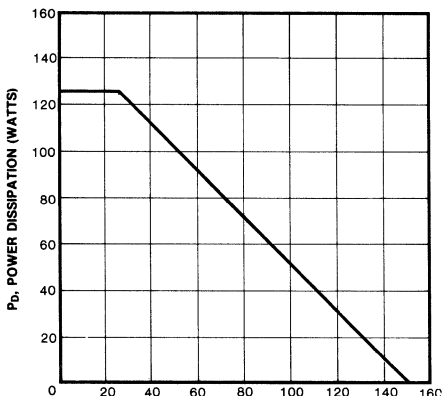
Typical Gate Charge Vs. Gate-To-Source Voltage



Typical On-Resistance Vs. Drain Current



Maximum Drain Current Vs. Case Temperature

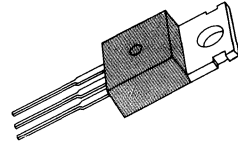


Power Vs. Temperature Derating Curve

FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

TO-220



IRF710/711/712/713

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF710	400V	3.6Ω	2.0A
IRF711	350V	3.6Ω	2.0A
IRF712	400V	5.0Ω	1.7A
IRF713	350V	5.0Ω	1.7A

MAXIMUM RATINGS

Characteristic	Symbol	IRF710	IRF711	IRF712	IRF713	Unit
Drain-Source Voltage (1)	V_{DSS}	400	350	400	350	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	400	350	400	350	Vdc
Gate-Source Voltage	V_{GS}	± 20				Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	2.0	2.0	1.7	1.7	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	1.2	1.2	1.1	1.1	Adc
Drain Current—Pulsed (3)	I_{DM}	5.0	5.0	4.3	4.3	Adc
Gate Current—Pulsed	I_{GM}	± 1.5				Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	120				mJ
Avalanche Current	I_{AS}	2.0				A
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	36 0.27				Watts W/ $^\circ C$
Operating and Storage Junction to Case	T_J, T_{stg}	-55 to 150				$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300				$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=53mH$, $V_{dd}=50V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-Source Breakdown Voltage IRF710/712	400	—	—	V	V _{GS} =0V
	IRF711/713	350	—	—	V	I _D =250μA
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} =V _{GS} , I _D =250μA
I _{GSS}	Gate-Source Leakage Forward	—	—	100	nA	V _{GS} =20V
I _{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	V _{GS} =-20V
I _{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	V _{DS} =Max. Rating, V _{GS} =0V
		—	—	1000	μA	V _{DS} =Max. Rating×0.8, V _{GS} =0V, T _C =125°C
I _{D(on)}	On-State Drain-Source Current (2) IRF710/711	2.0	—	—	A	V _{DS} ≥10V, V _{GS} =10V
	IRF712/713	1.7	—	—	A	
R _{DS(on)}	Static Drain-Source On-State Resistance (2) IRF710/711	—	3.2	3.6	Ω	V _{GS} =10V, I _D =1.1A
	IRF712/713	—	3.5	5.0	Ω	
g _{fs}	Forward Transconductance (2)	0.5	1.0	—	∅	V _{DS} ≥50V, I _D =1.1A
C _{iss}	Input Capacitance	—	180	—	pF	V _{GS} =0V, V _{DS} =25V, f=1.0MHz
C _{oss}	Output Capacitance	—	40	—	pF	
C _{rss}	Reverse Transfer Capacitance	—	14	—	pF	
t _{d(on)}	Turn-On Delay Time	—	7.9	12	ns	V _{DD} =0.5BV _{DSS} , I _D =2.0A, Z _O =24Ω (MOSFET switching times are essentially independent of operating temperature)
t _r	Rise Time	—	9.9	15	ns	
t _{d(off)}	Turn-Off Delay Time	—	21	32	ns	
t _f	Fall Time	—	11	17	ns	
Q _g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	7.7	12	nC	V _{GS} =10V, I _D =2.0A, V _{DS} =0.8 Max. Rating (Gate charge is essentially independent of operating temperature.)
Q _{gs}	Gate-Source Charge	—	1.2	1.9	nC	
Q _{gd}	Gate-Drain ("Miller") Charge	—	4.0	5.9	nC	

THERMAL RESISTANCE

R _{thJC}	Junction-to-Case	—	—	3.5	KW	
R _{thCS}	Case-to-Sink	—	0.5	—	K/W	Mounting surface flat, smooth, and greased
R _{thJA}	Junction-to-Ambient	—	—	80	K/W	Free Air Operation

Notes: (1) T_J=25°C to 150°C

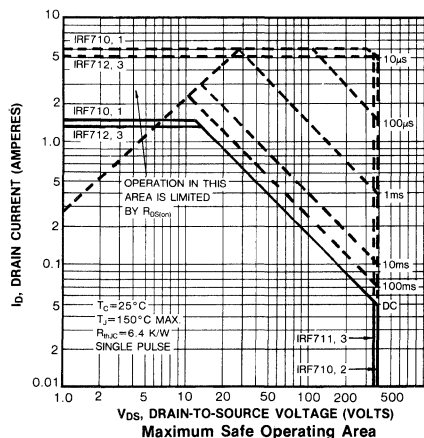
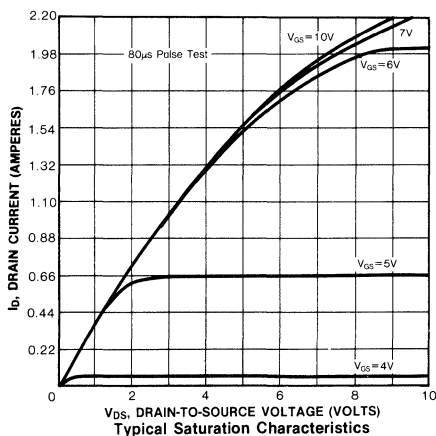
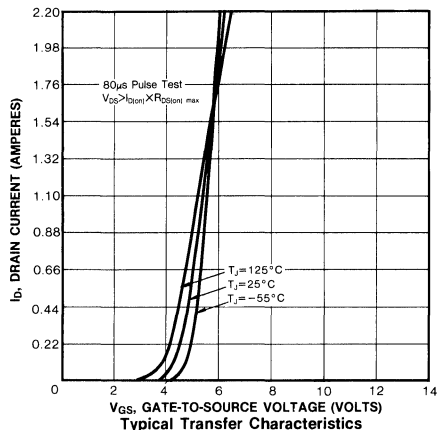
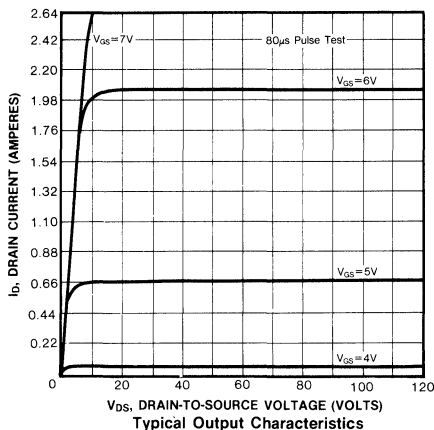
(2) Pulse test: Pulse width≤300μs, Duty Cycle≤2%

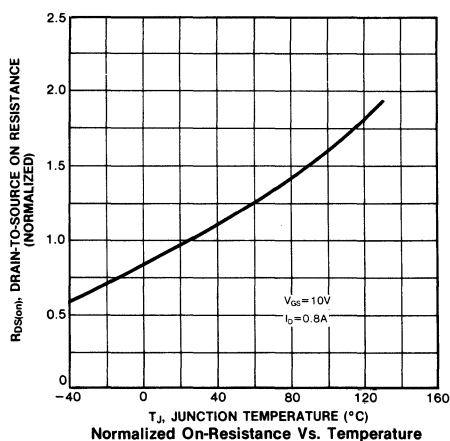
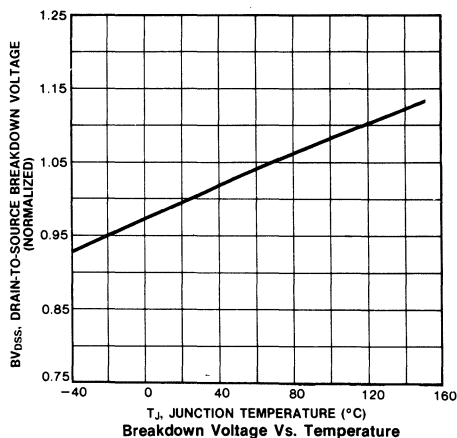
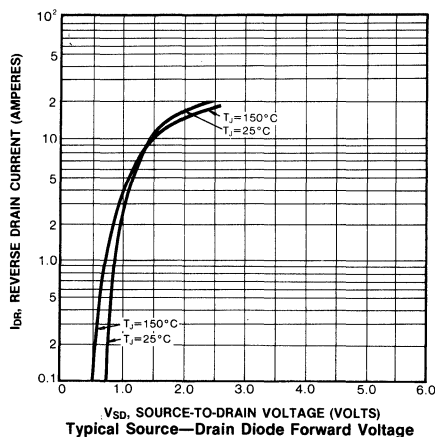
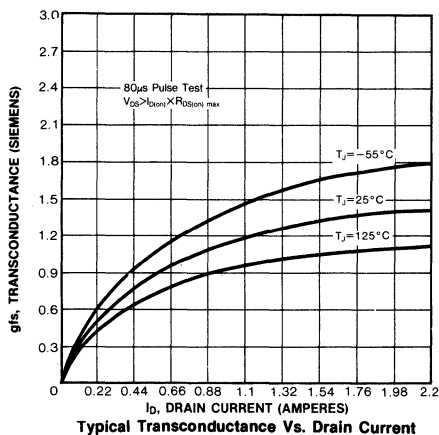
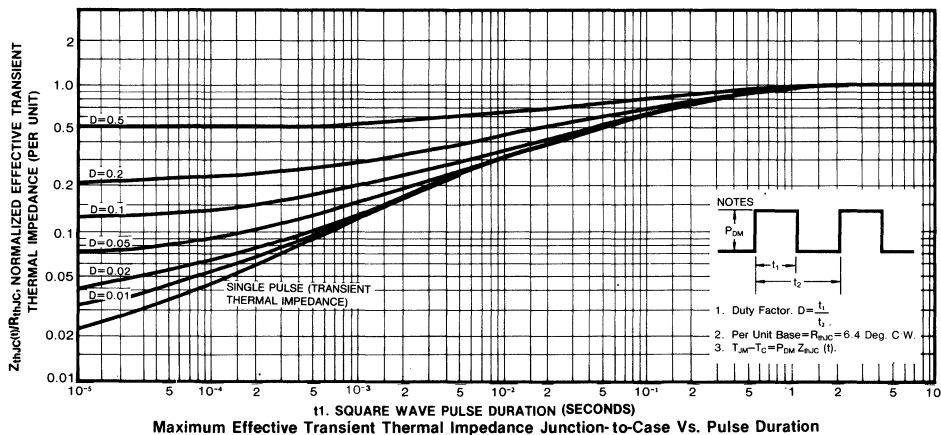
(3) Repetitive rating: Pulse width limited by max. junction temperature

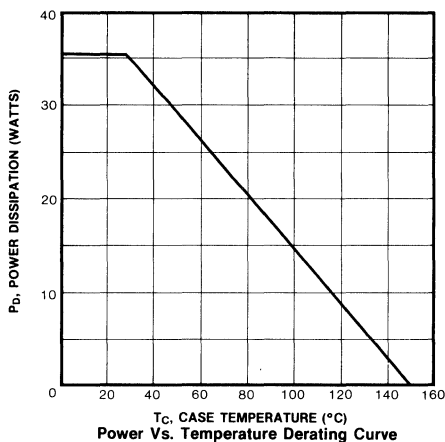
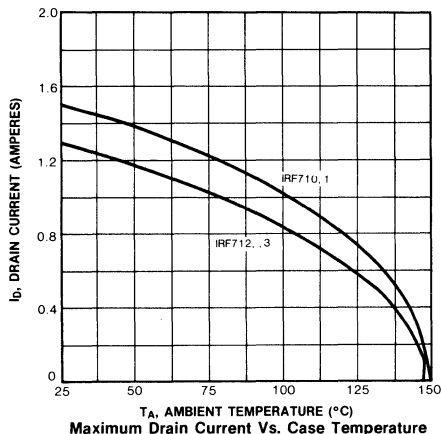
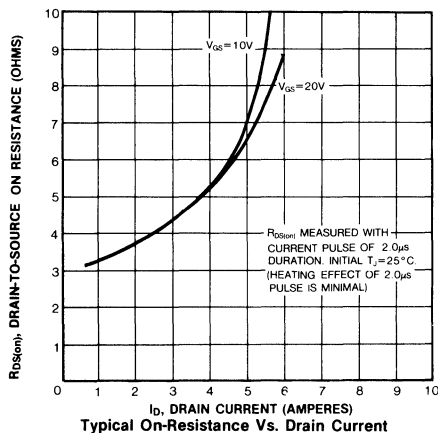
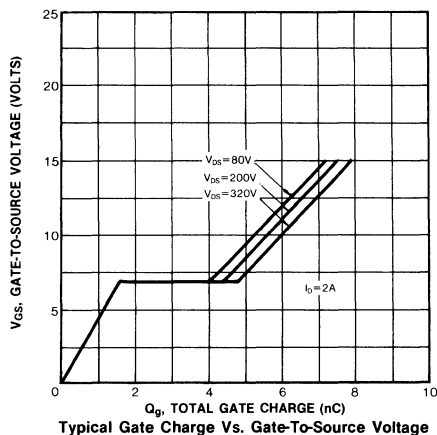
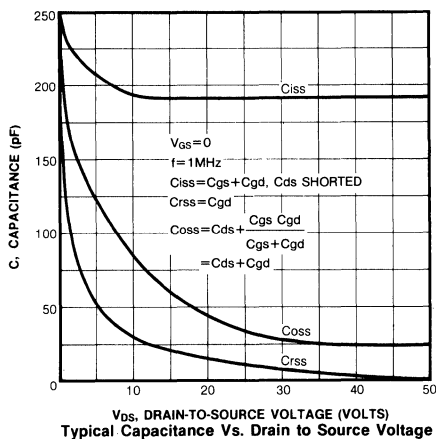
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic	Type	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	IRF710	—	—	2.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier 
		IRF711	—	—	2.0	A	
		IRF712	—	—	1.7	A	
		IRF713	—	—	1.7	A	
I_{SM}	Pulse Source Current (Body Diode) (3)	IRF710	—	—	5.0	A	
		IRF711	—	—	5.0	A	
		IRF712	—	—	4.3	A	
		IRF713	—	—	4.3	A	
V_{SR}	Diode Forward Voltage (2)	IRF710	—	—	1.6	V	$T_C=25^\circ\text{C}$, $I_S=2.0\text{A}$, $V_{GS}=0\text{V}$
		IRF711	—	—	1.6	V	$T_C=25^\circ\text{C}$, $I_S=2.0\text{A}$, $V_{GS}=0\text{V}$
		IRF712	—	—	1.5	v	$T_C=25^\circ\text{C}$, $I_S=1.7\text{A}$, $V_{GS}=0\text{V}$
		IRF713	—	—	1.5	v	$T_C=25^\circ\text{C}$, $I_S=1.7\text{A}$, $V_{GS}=0\text{V}$
t_{rr}	Reverse Recovery Time		—	240	520	ns	$T_J=25^\circ\text{C}$, $I_F=2.0\text{A}$, $dI_F/dt=100\text{A}/\mu\text{s}$

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature



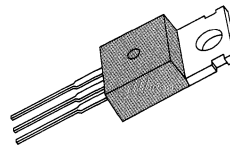




FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

TO-220



IRF720/721/722/723

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF720	400V	1.8Ω	3.3A
IRF721	350V	1.8Ω	3.3A
IRF722	400V	2.5Ω	2.8A
IRF723	350V	2.5Ω	2.8A

MAXIMUM RATINGS

Characteristics	Symbol	IRF720	IRF721	IRF722	IRF723	Unit
Drain-Source Voltage (1)	V_{DSS}	400	350	400	350	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	400	350	400	350	Vdc
Gate-Source Voltage	V_{GS}	± 20				Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	3.3	3.3	2.8	2.8	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	2.1	2.1	1.8	1.8	Adc
Drain Current—Pulsed (3)	I_{DM}	13	13	11	11	Adc
Gate Current—Pulsed	I_{GM}	± 1.5				Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	190				mJ
Avalanche Current	I_{AS}	3.3				A
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	50 0.40				Watts W/ $^\circ C$
Operating and Storage Junction to Case	T_J, T_{stg}	-55 to 150				$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300				$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=31\text{ mH}$, $V_{dd}=50V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-Source Breakdown Voltage IRF720 IRF722	400	—	—	V	V _{GS} =0V I _D =250μA
	IRF721 IRF723	350	—	—	V	
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} =V _{GS} , I _D =250μA
I _{GSS}	Gate-Source Leakage Forward	—	—	100	nA	V _{GS} =20V
I _{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	V _{GS} =-20V
I _{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	V _{DS} =Max. Rating, V _{GS} =0V
		—	—	1000	μA	V _{DS} =Max. Rating×0.8, V _{GS} =0V, T _C =125°C
I _{D(on)}	On-State Drain-Source Current (2) IRF720 IRF721	3.3	—	—	A	V _{DS} ≥8.2V, V _{GS} =10V
	IRF722 IRF723	2.8	—	—	A	
R _{DS(on)}	Static Drain-Source On-State Resistance (2) IRF720 IRF721	—	1.4	1.8	Ω	V _{GS} =10V, I _D =1.8A
	IRF722 IRF723	—	1.8	2.5	Ω	
g _{fs}	Forward Transconductance (2)	1.0	2.2	—	∅	V _{DS} ≥50V, I _D =1.8A
C _{iss}	Input Capacitance	—	400	—	pF	V _{GS} =0V, V _{DS} =25V, f=1.0MHz
C _{oss}	Output Capacitance	—	59.3	—	pF	
C _{rss}	Reverse Transfer Capacitance	—	27	—	pF	
t _{d(on)}	Turn-On Delay Time	—	10	15	ns	V _{DD} =0.5BV _{DSS} , I _D =3.3A, Z _O =18Ω (MOSFET switching times are essentially independent of operating temperature)
t _r	Rise Time	—	14	20	ns	
t _{d(off)}	Turn-Off Delay Time	—	30	45	ns	
t _f	Fall Time	—	13	20	ns	
Q _g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	12.5	15	nC	V _{GS} =10V, I _D =9.2A, V _{DS} =0.8 Max. Rating (Gate charge is essentially independent of operating temperature.)
Q _{gs}	Gate-Source Charge	—	2.8	—	nC	
Q _{gd}	Gate-Drain ("Miller") Charge	—	9.7	—	nC	

THERMAL RESISTANCE

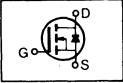
Symbol	Characteristic		IRF720-3	Unit	
R _{thJC}	Junction-to-Case	MAX	2.5	K/W	
R _{thCS}	Case-to-Sink	TYP	0.5	K/W	Mounting surface flat, smooth, and greased
R _{thJA}	Junction-to-Ambient	MAX	80	K/W	Free Air Operation

Notes: (1) T_J=25°C to 150°C

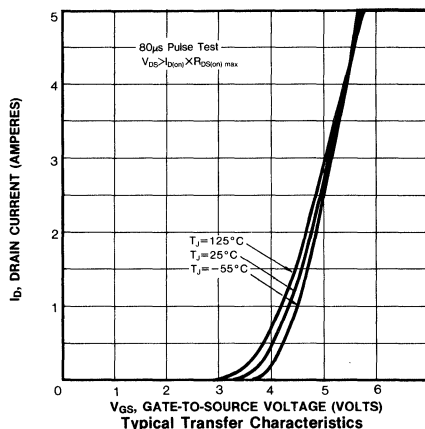
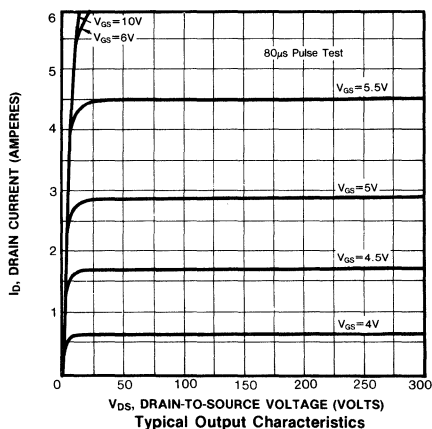
(2) Pulse test: Pulse width≤300μs, Duty Cycle≤2%

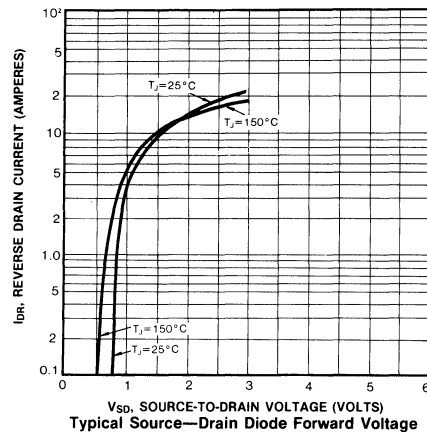
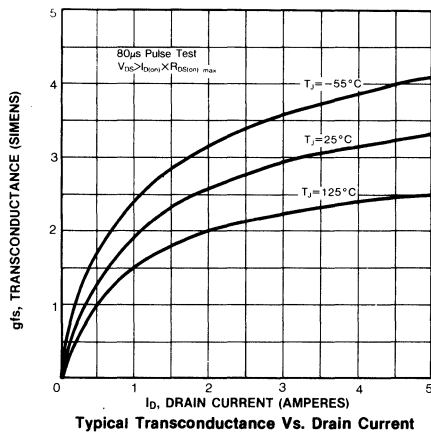
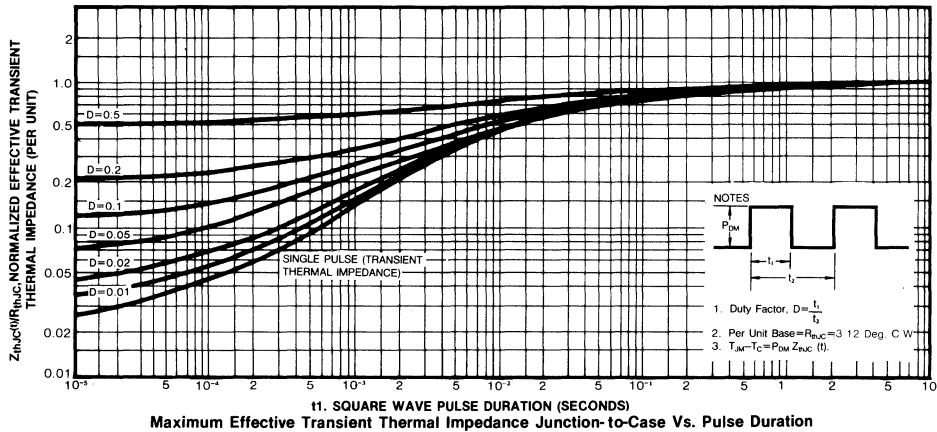
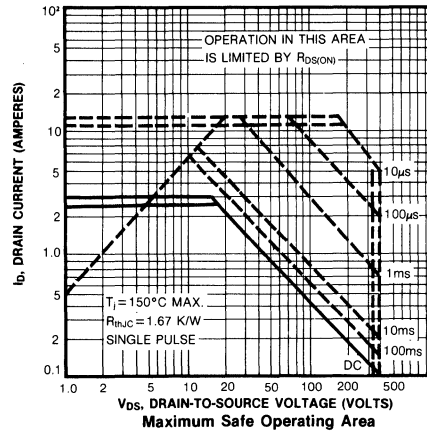
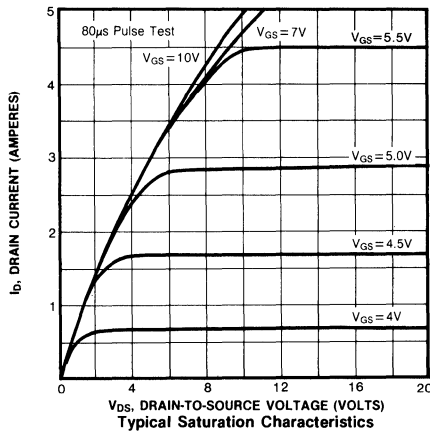
(3) Repetitive rating: Pulse width limited by max. junction temperature

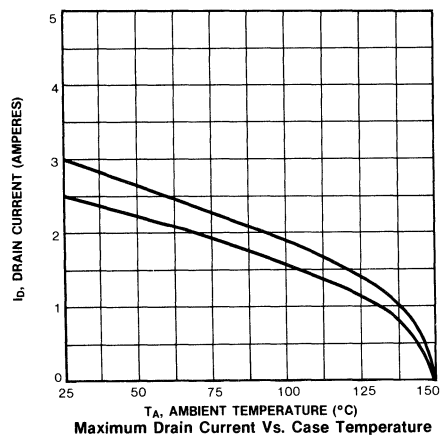
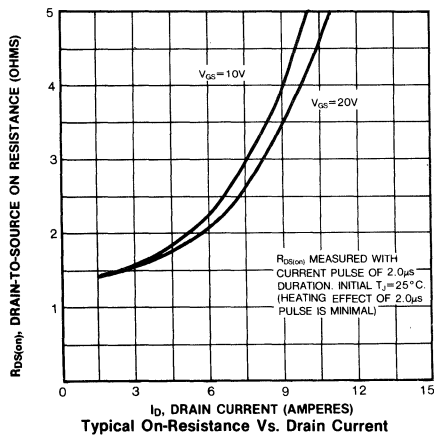
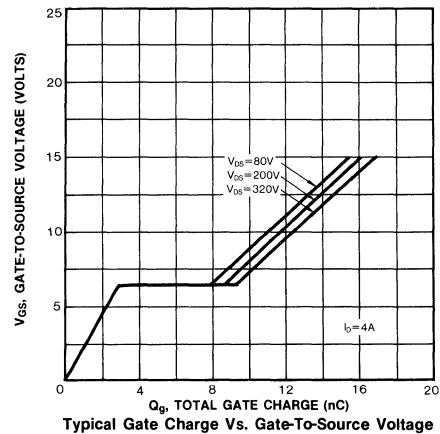
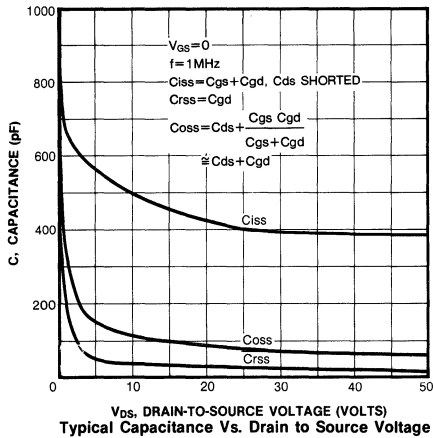
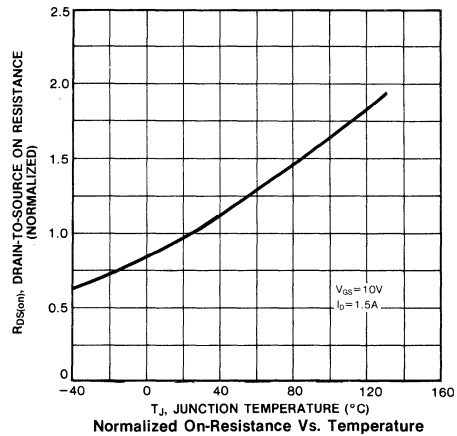
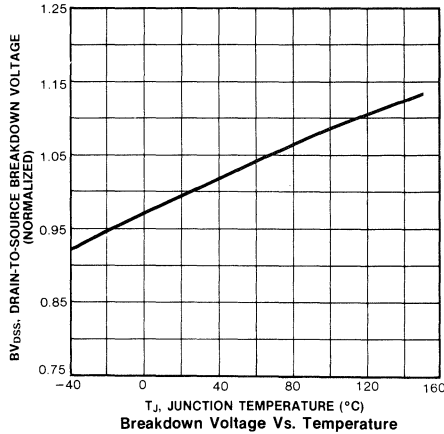
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

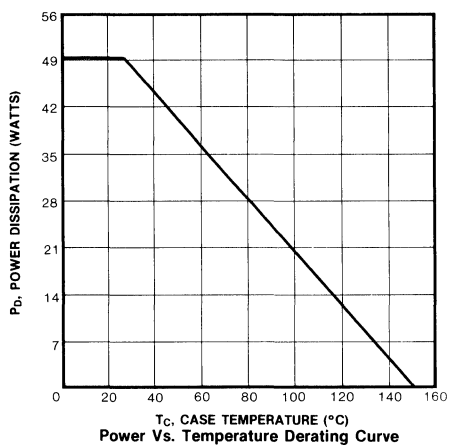
Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode) IRF720 IRF721	—	—	3.3	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier 
	IRF722 IRF723	—	—	2.8	A	
I_{SM}	Pulse Source Current(Body Diode)(3) IRF720 IRF721	—	—	13	A	
	IRF722 IRF723	—	—	11	A	
V_{SD}	Diode Forward Voltage (2) IRF720 IRF721	—	—	1.8	V	$T_C=25^\circ\text{C}$, $I_S=3.3\text{A}$, $V_{GS}=0\text{V}$
	IRF722 IRF723	—	—	1.7	V	$T_C=25^\circ\text{C}$, $I_S=2.8\text{A}$, $V_{GS}=0\text{V}$
t_{rr}	Reverse Recovery Time	—	270		ns	$T_J=25^\circ\text{C}$, $I_F=3.3\text{A}$, $dI_F/dt=100\text{A}/\mu\text{S}$

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
 (3) Repetitive rating: Pulse with limited by max. junction temperature









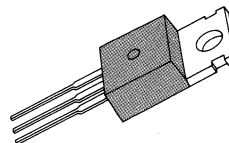
FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

PRODUCT SUMMARY

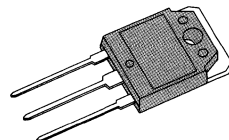
Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF730/IRFP330	400V	1.0 Ω	5.5A
IRF731/IRFP331	350V	1.0 Ω	5.5A
IRF732/IRFP332	400V	1.5 Ω	4.5A
IRF733/IRFP333	350V	1.5 Ω	4.5A

TO-220



IRF730/731/732/733

TO-3P



IRFP330/331/332/333

MAXIMUM RATINGS

Characteristics	Symbol	IRF730 IRFP330	IRF731 IRFP331	IRF732 IRFP332	IRF733 IRFP333	Unit
Drain-Source Voltage (1)	V_{DSS}	400	350	400	350	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	400	350	400	350	Vdc
Gate-Source Voltage	V_{GS}	± 20				Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	5.5	5.5	4.5	4.5	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	3.5	3.5	3.0	3.0	Adc
Drain Current—Pulsed (3)	I_{DM}	32	32	18	18	Adc
Gate Current—Pulsed	I_{GM}	± 1.5				Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	290				mJ
Avalanche Current	I_{AS}	5.5				A
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	75 0.6				Watts W/ $^\circ C$
Operating and Storage Junction to Case	T_J, T_{stg}	-55 to 150				$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300				$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=17\text{ mH}$, $V_{dd}=50V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage IRF730/IRFP330 IRF732/IRFP332	400	—	—	V	$V_{GS}=0V$ $I_D=250\mu A$
	IRF731/IRFP331 IRF733/IRFP333	350	—	—	V	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}$, $I_D=250\mu A$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS}=20V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	$V_{GS}=-20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS}=\text{Max. Rating}$, $V_{GS}=0V$
		—	—	1000	μA	$V_{DS}=\text{Max. Rating}\times 0.8$, $V_{GS}=0V$, $T_C=125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2) IRF730/IRFP330 IRF731/IRFP331	5.5	—	—	A	$V_{DS}\geq 8.2V$, $V_{GS}=10V$
	IRF732/IRFP332 IRF733/IRFP333	4.5	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance (2) IRF730/IRFP330 IRF731/IRFP331	—	0.8	1.0	Ω	$V_{GS}=10V$, $I_D=3.0A$
	IRF732/IRFP332 IRF733/IRFP333	—	1.0	1.5	Ω	
g_{fs}	Forward Transconductance (2)	2.9	4.4	—	Ω	$V_{DS}\geq 50V$, $I_D=3.0A$
C_{iss}	Input Capacitance	—	780	—	pF	$V_{GS}=0V$, $V_{DS}=25V$, $f=1.0\text{MHz}$
C_{oss}	Output Capacitance	—	99	—	pF	
C_{rss}	Reverse Transfer Capacitance	—	43	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	11	17	ns	$V_{DD}=0.5BV_{DSS}$, $I_D=5.5A$, $Z_O=12\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	19	29	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	37	56	ns	
t_f	Fall Time	—	16	24	ns	$V_{GS}=10V$, $I_D=5.5A$, $V_{DS}=0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature.)
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	18	30	nC	
Q_{gs}	Gate-Source Charge	—	40	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	14	—	nC	

THERMAL RESISTANCE

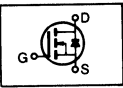
Symbol	Characteristic		IRF730-3	IRFP330-3	Unit	
R_{thJC}	Junction-to-Case	MAX	1.67	1.67	K/W	
R_{thCS}	Case-to-Sink	TYP	0.50	0.24	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	MAX	80	40	K/W	Free Air Operation

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C

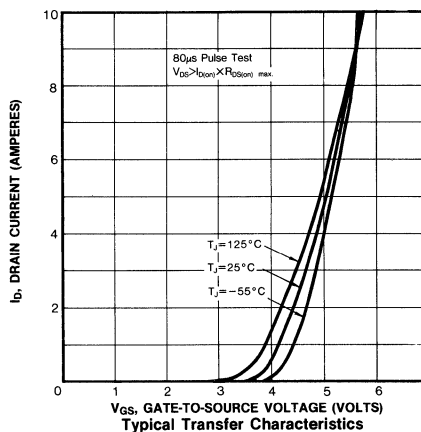
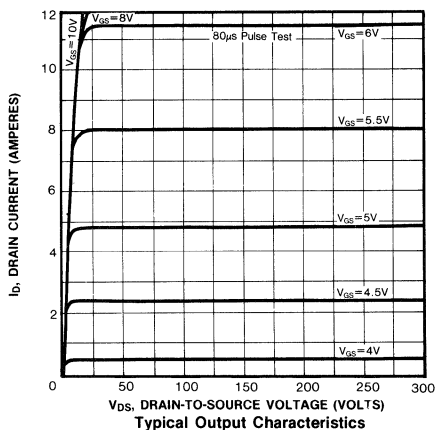
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

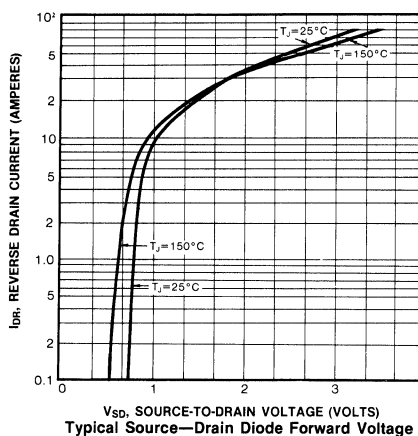
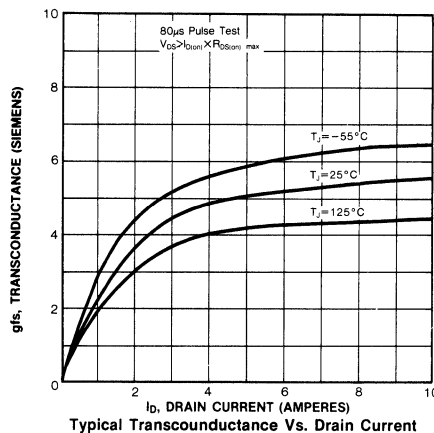
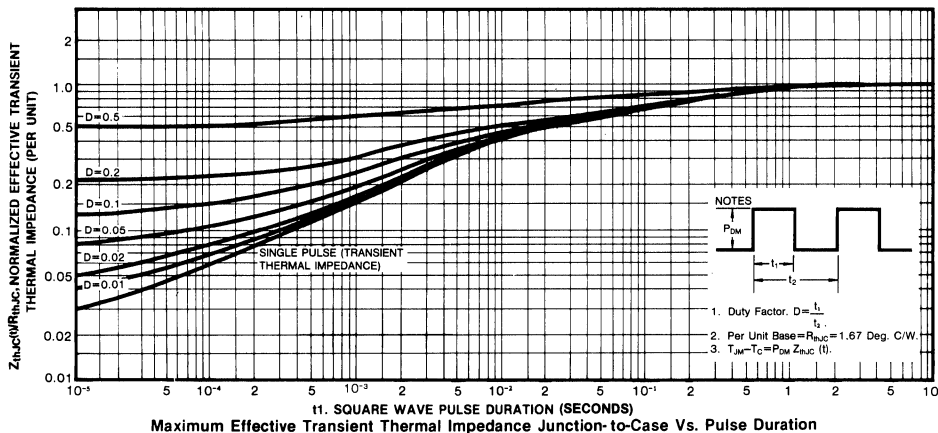
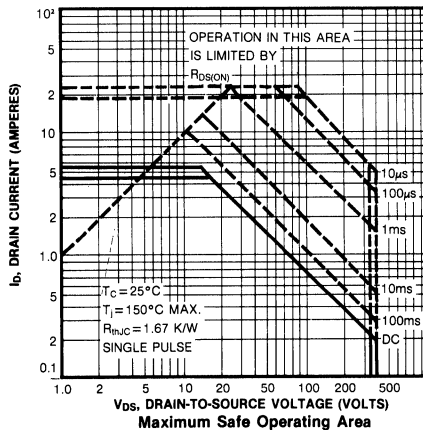
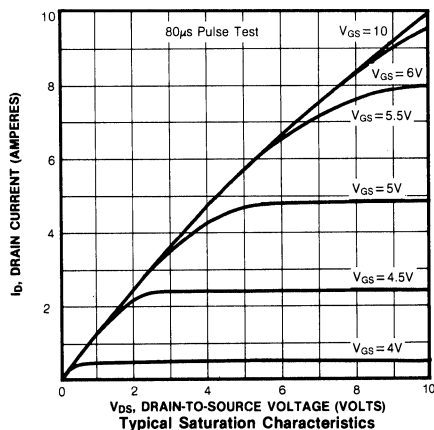
(3) Repetitive rating: Pulse width limited by max. junction temperature

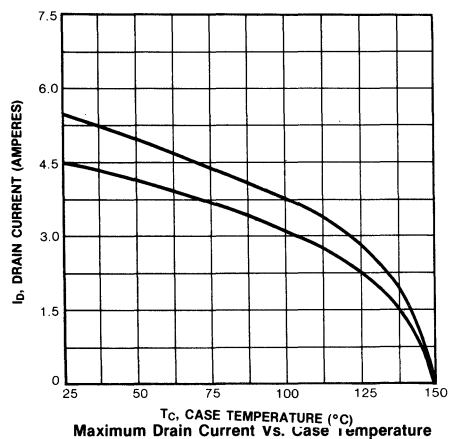
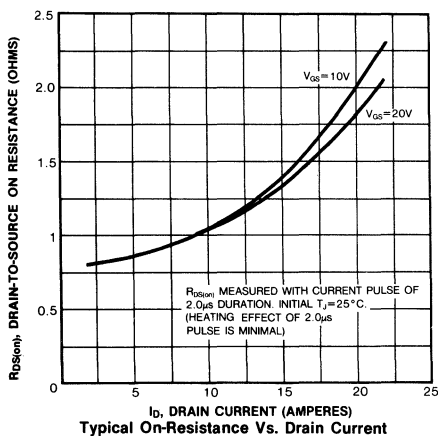
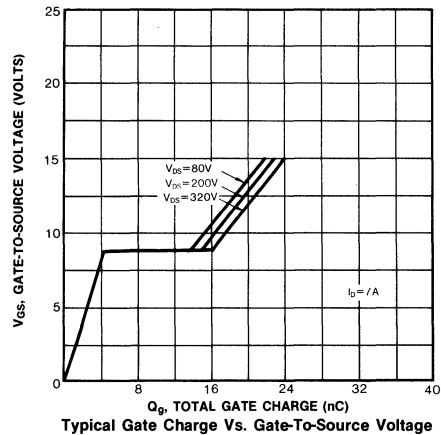
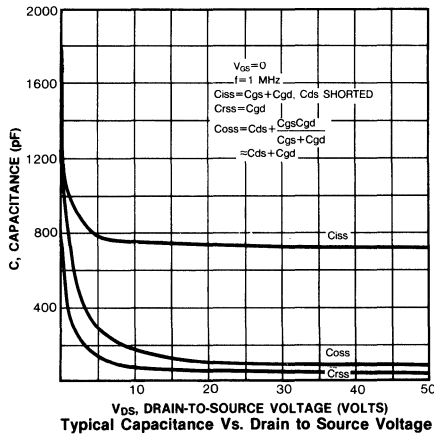
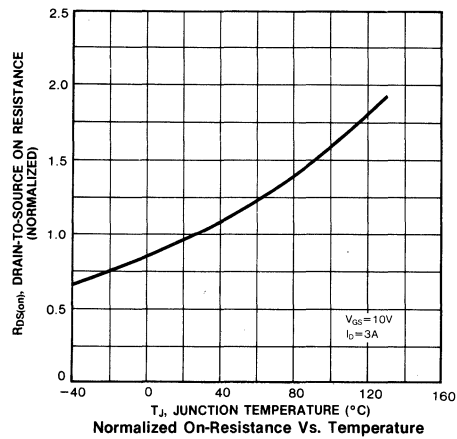
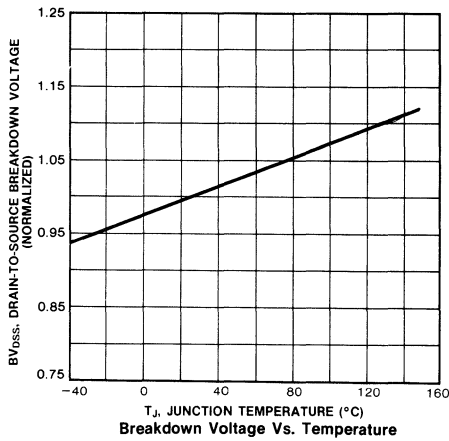
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

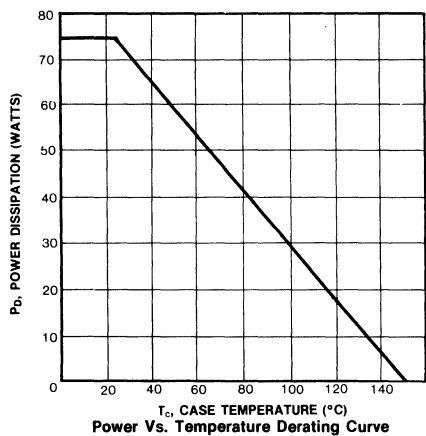
Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode) IRF730/IRFP330 IRF731/IRFP331	—	—	5.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier 
	IRF732/IRFP332 IRF733/IRFP333	—	—	4.5	A	
I_{SM}	Pulse Source Current(Body Diode)(3) IRF730/IRFP330 IRF731/IRFP331	—	—	22	A	
	IRF732/IRFP332 IRF733/IRFP333	—	—	18	A	
V_{SD}	Diode Forward Voltage (2) IRF730/IRFP330 IRF731/IRFP331	—	—	1.8	V	$T_C=25^\circ\text{C}$, $I_S=5.5\text{A}$, $V_{GS}=0\text{V}$
	IRF732/IRFP332 IRF733/IRFP333	—	—	1.6	V	$T_C=25^\circ\text{C}$, $I_S=4.5\text{A}$, $V_{GS}=0\text{V}$
t_{rr}	Reverse Recovery Time	—	310	660	ns	$T_J=25^\circ\text{C}$, $I_F=5.5\text{A}$, $dI_F/dt=100\text{A}/\mu\text{S}$

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature









2

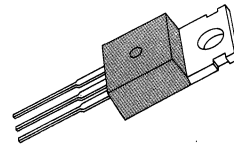
FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

PRODUCT SUMMARY

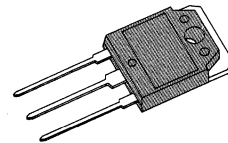
Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF740/IRFP340	400V	0.55Ω	10A
IRF741/IRFP341	350V	0.55Ω	10A
IRF742/IRFP342	400V	0.80Ω	8.3A
IRF743/IRFP343	350V	0.80Ω	8.3A

TO-220



IRF740/741/742/743

TO-3P



IRFP340/341/342/343

MAXIMUM RATINGS

Characteristics	Symbol	IRF740 IRFP340	IRF741 IRFP341	IRF742 IRFP342	IRF743 IRFP343	Unit
Drain-Source Voltage (1)	V_{DSS}	400	350	400	350	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	400	350	400	350	Vdc
Gate-Source Voltage	V_{GS}	± 20				Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	10	10	8.3	8.3	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	6.3	6.3	5.2	5.2	Adc
Drain Current—Pulsed (3)	I_{DM}	40	40	33	33	Adc
Gate Current—Pulsed	I_{GM}	± 1.5				Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	520				mJ
Avalanche Current	I_{AS}	10				A
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	125 1.0				Watts W/ $^\circ C$
Operating and Storage Junction to Case	T_J, T_{stg}	-55 to 150				$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300				$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=9.1\text{ mH}$, $V_{dd}=50V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage IRF740/IRFP340 IRF742/IRFP342	400	—	—	V	$V_{GS}=0V$ $I_D=250\mu A$
	IRF741/IRFP341 IRF743/IRFP343	350	—	—	V	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}$, $I_D=250\mu A$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS}=20V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	$V_{GS}=-20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS}=\text{Max. Rating}$, $V_{GS}=0V$
		—	—	1000	μA	$V_{DS}=\text{Max. Rating} \times 0.8$, $V_{GS}=0V$, $T_C=125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2) IRF740/IRFP340 IRF741/IRFP341	10	—	—	A	$V_{DS} \geq 8V$, $V_{GS}=10V$
	IRF742/IRFP342 IRF743/IRFP343	8.3	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance (2) IRF740/IRFP340 IRF741/IRFP341	—	—	0.55	Ω	$V_{GS}=10V$, $I_D=5.2A$
	IRF742/IRFP342 IRF743/IRFP343	—	—	0.80	Ω	
g_{fs}	Forward Transconductance (2)	5.8	87	—	μ	$V_{DS} \geq 50V$, $I_D=5.2A$
C_{iss}	Input Capacitance	—	1500	—	pF	$V_{GS}=0V$, $V_{DS}=25V$, $f=1.0\text{MHz}$
C_{oss}	Output Capacitance	—	178	—	pF	
C_{rss}	Reverse Transfer Capacitance	—	75	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	14	21	ns	$V_{DD}=0.5BV_{DSS}$, $I_D=10A$, $Z_O=9.1\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	27	41	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	50	75	ns	
t_f	Fall Time	—	24	36	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	42	63	nC	$V_{GS}=10V$, $I_D=10A$, $V_{DS}=0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	6.0	9.0	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	21	32	nC	

THERMAL RESISTANCE

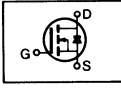
Symbol	Characteristic		IRF740-3	IRFP340-3	Unit	
R_{thJC}	Junction-to-Case	MAX	1.0	1.0	K/W	
R_{thCS}	Case-to-Sink	TYP	0.5	0.24	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	MAX	80	40	K/W	Free Air Operation

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C

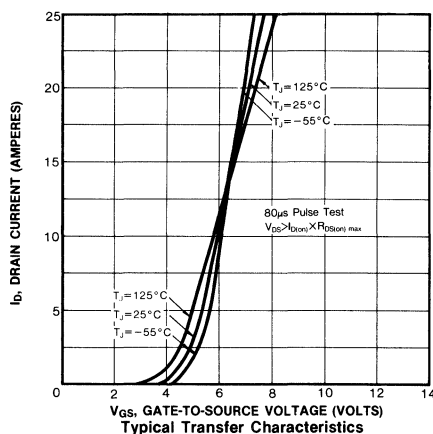
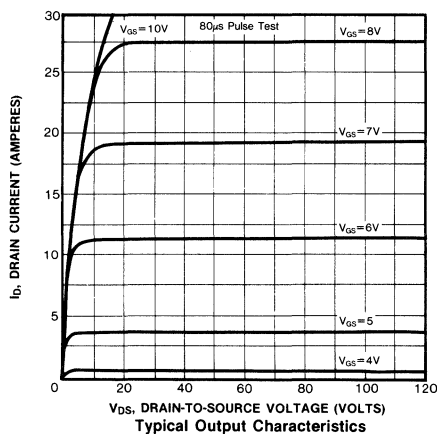
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

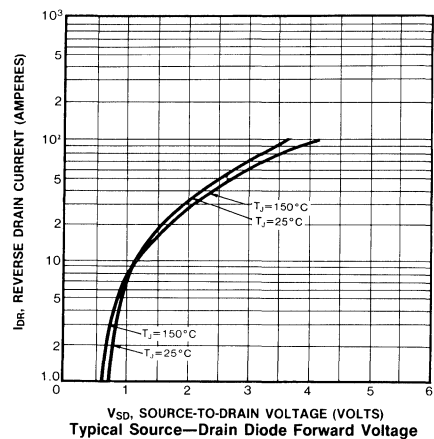
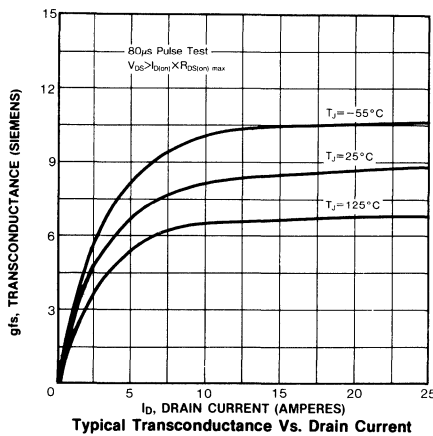
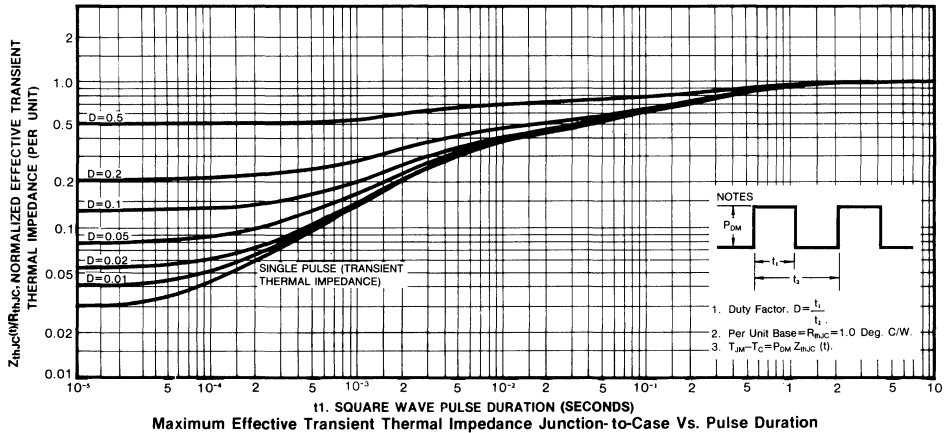
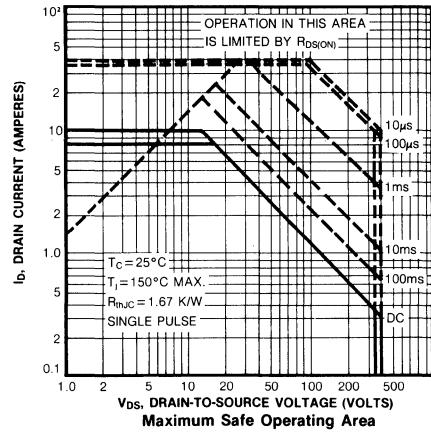
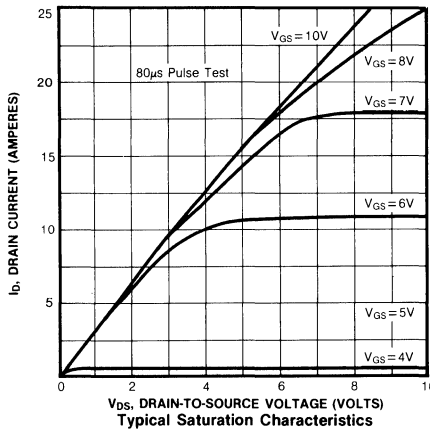
(3) Repetitive rating: Pulse width limited by max. junction temperature

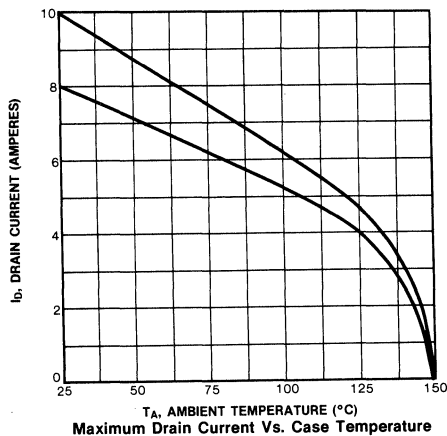
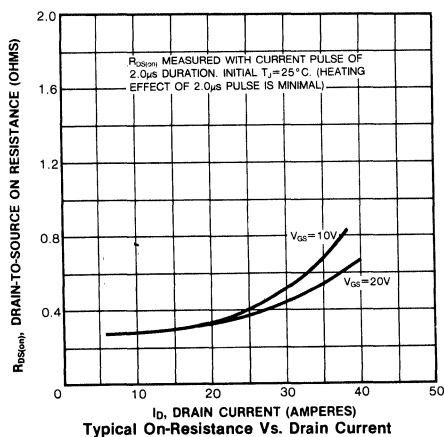
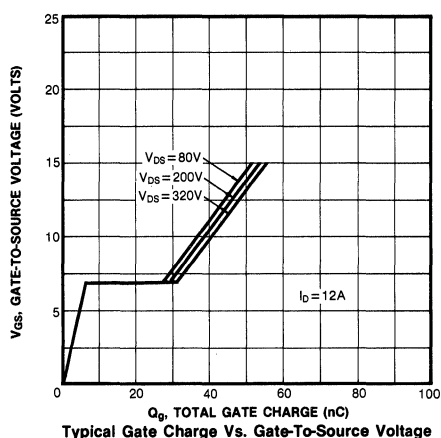
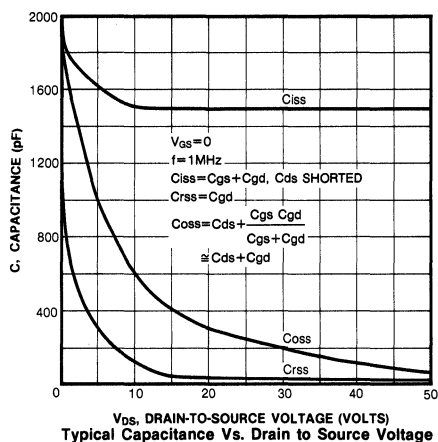
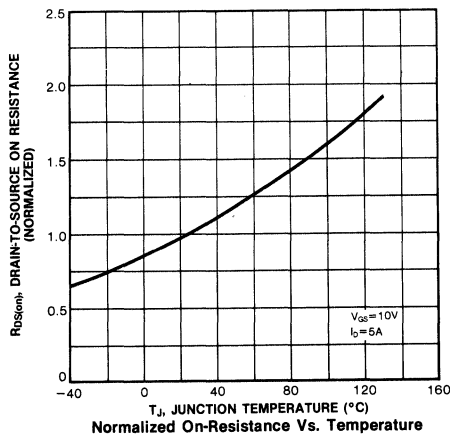
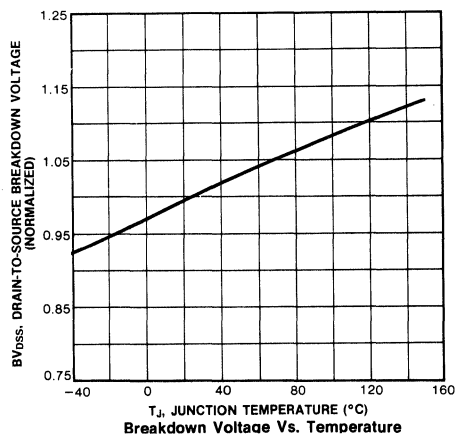
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

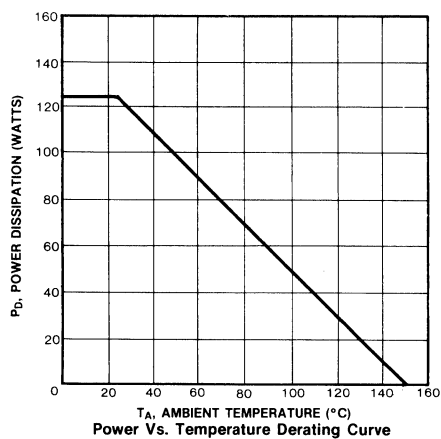
Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode) IRF740/IRFP340 IRF741/IRFP341	—	—	10	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier 
	IRF742/IRFP342 IRF743/IRFP343	—	—	8.0	A	
I_{SM}	Pulse Source Current(Body Diode)(3) IRF740/IRFP340 IRF741/IRFP341	—	—	40	A	
	IRF742/IRFP342 IRF743/IRFP343	—	—	32	A	
V_{SD}	Diode Forward Voltage (2) IRF740/IRFP340 IRF741/IRFP341	—	—	2.0	V	$T_C=25^\circ\text{C}$, $I_S=10\text{A}$, $V_{GS}=0\text{V}$
	IRF742/IRFP342 IRF743/IRFP343	—	—	1.9	V	$T_C=25^\circ\text{C}$, $I_S=8.0\text{A}$, $V_{GS}=0\text{V}$
t_{rr}	Reverse Recovery Time	—	370		ns	$T_J=25^\circ\text{C}$, $I_F=10\text{A}$, $dI_F/dt=100\text{A}/\mu\text{S}$

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature





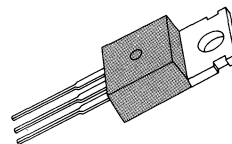




FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

TO-220



IRF820/821/822/823

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF820	500V	3.0Ω	2.5A
IRF821	450V	3.0Ω	2.5A
IRF822	500V	4.0Ω	2.2A
IRF823	450V	4.0Ω	2.2A

MAXIMUM RATINGS

Characteristics	Symbol	IRF820	IRF821	IRF822		Unit
Drain-Source Voltage (1)	V_{DS}	500	450	500	450	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	500	450	500	450	Vdc
Gate-Source Voltage	V_{GS}	± 20				Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	2.5	2.5	2.2	2.2	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	1.6	1.6	1.4	1.4	Adc
Drain Current—Pulsed (3)	I_{DM}	8.0	8.0	7.0	7.0	Adc
Gate Current—Pulsed	I_{GM}	± 1.5				Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	210				mJ
Avalanche Current	I_{AS}	2.5				A
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	50 0.4				Watts W/ $^\circ C$
Operating and Storage Junction to Case	T_J, T_{stg}	-55 to 150				$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300				$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=60\text{ mH}$, $V_{dd}=50V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage IRF820 IRF822	500	—	—	V	$V_{GS} = 0V$ $I_D = 250\mu A$
	IRF821 IRF823	450	—	—	V	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu A$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS} = 20V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	$V_{GS} = -20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0V$
		—	—	1000	μA	$V_{DS} = \text{Max. Rating} \times 0.8$, $V_{GS} = 0V$, $T_C = 125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2) IRF820 IRF821	2.5	—	—	A	$V_{DS} \geq 10V$, $V_{GS} = 10V$
	IRF822 IRF823	2.0	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance (2) IRF820 IRF821	—	2.5	3.0	Ω	$V_{GS} = 10V$, $I_D = 1.4A$
	IRF822 IRF823	—	3.0	4.0	Ω	
g_{fs}	Forward Transconductance (2)	1.5	2.3	—	$\mathcal{U}$	$V_{DS} \geq 10V$, $I_D = 1.4A$
C_{iss}	Input Capacitance	—	390	—	pF	$V_{GS} = 0V$, $V_{DS} = 25V$, $f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	52	—	pF	
C_{rss}	Reverse Transfer Capacitance	—	22	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	10	15	ns	$V_{DD} = 0.5BV_{DSS}$, $I_D = 2.5A$, $Z_O = 18\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	12	18	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	28	42	ns	
t_f	Fall Time	—	12	18	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	13	19	nC	$V_{GS} = 10V$, $I_D = 2.5A$, $V_{DS} = 0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	2.2	3.3	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	6.8	10	nC	

THERMAL RESISTANCE

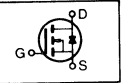
Symbol	Characteristic		IRF820-3	Unit	
R_{thJC}	Junction-to-Case	MAX	2.5	K/W	
R_{thCS}	Case-to-Sink	TYP	0.5	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	MAX	80	K/W	Free Air Operation

Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C

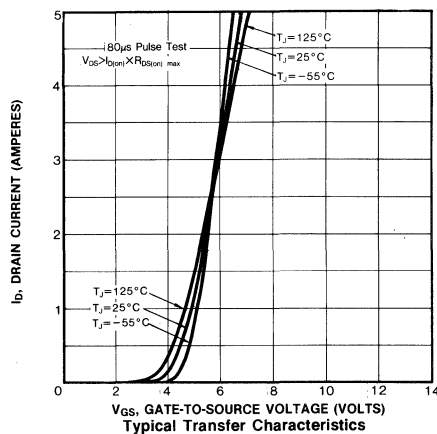
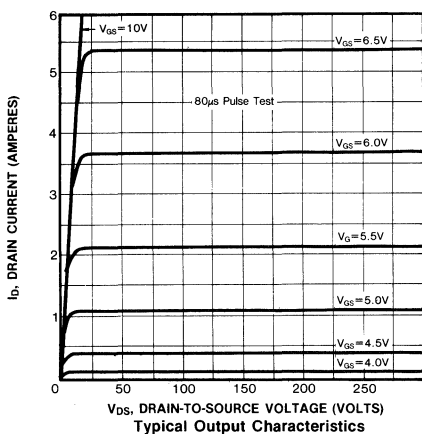
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

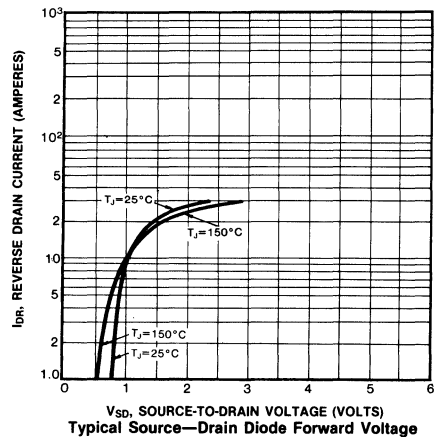
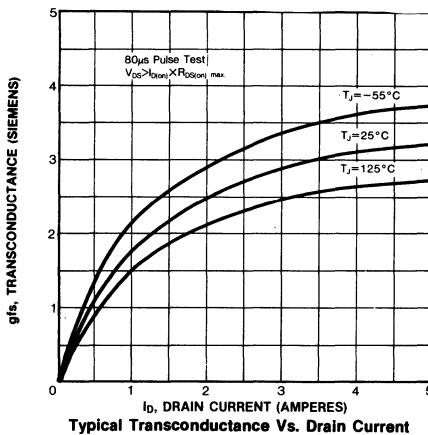
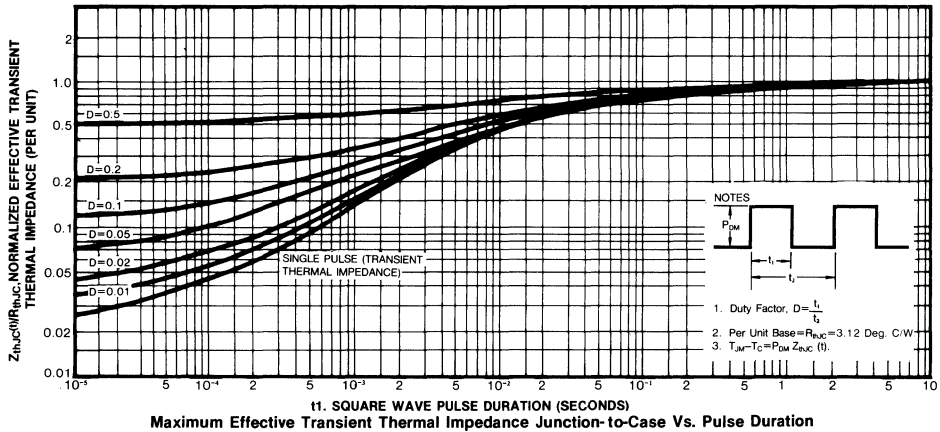
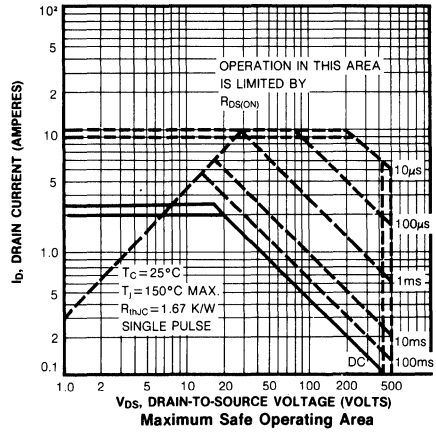
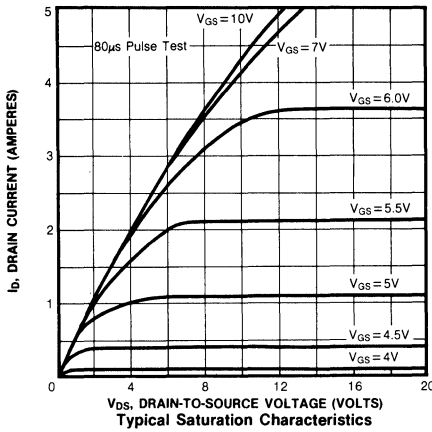
(3) Repetitive rating: Pulse width limited by max. junction temperature

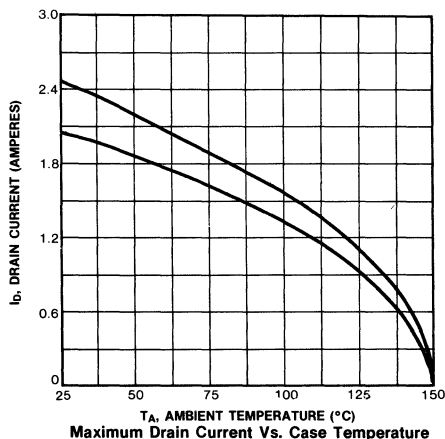
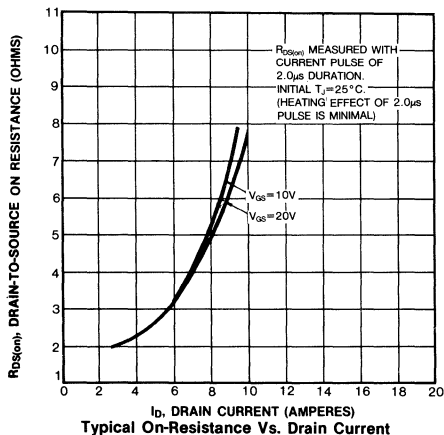
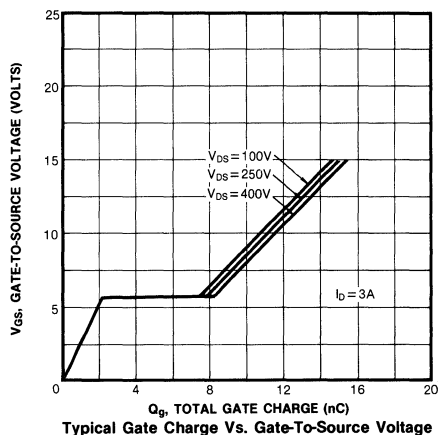
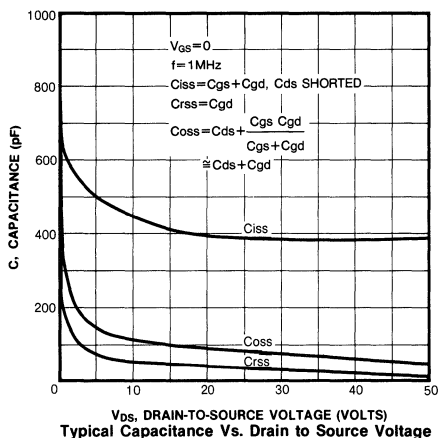
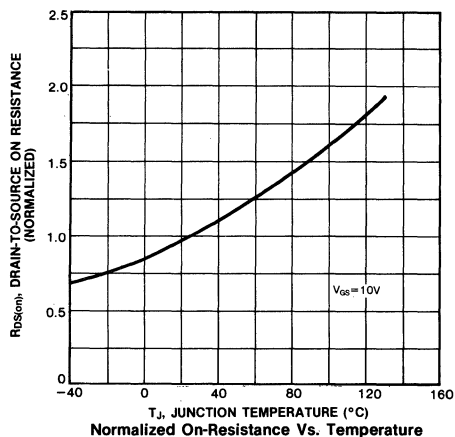
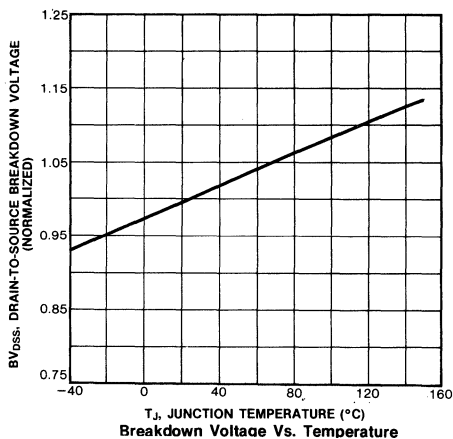
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

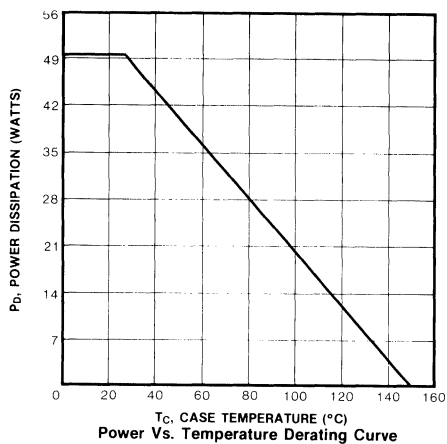
Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode) IRF820 IRF821	—	—	2.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier 
	IRF822 IRF823	—	—	2.2	A	
I_{SM}	Pulse Source Current(Body Diode)(3) IRF820 IRF821	—	—	8.0	A	
	IRF822 IRF823	—	—	7.0	A	
V_{SD}	Diode Forward Voltage (2) IRF820 IRF821	—	—	1.6	V	$T_C=25^\circ\text{C}$, $I_S=2.5\text{A}$, $V_{GS}=0\text{V}$
	IRF822 IRF823	—	—	1.5	V	$T_C=25^\circ\text{C}$, $I_S=2.2\text{A}$, $V_{GS}=0\text{V}$
t_{rr}	Reverse Recovery Time	—	270	540	ns	$T_J=25^\circ\text{C}$, $I_F=2.5\text{A}$, $dI_F/dt=100\text{A}/\mu\text{S}$

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
 (3) Repetitive rating: Pulse with limited by max. junction temperature









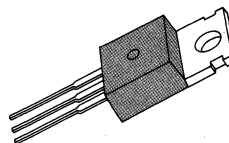
FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

PRODUCT SUMMARY

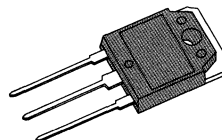
Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF830/IRFP430	500V	1.5Ω	4.5A
IRF831/IRFP431	450V	1.5Ω	4.5A
IRF832/IRFP432	500V	2.0Ω	4.0A
IRF833/IRFP433	450V	2.0Ω	4.0A

TO-220



IRF830/831/832/833

TO-3P



IRFP430/431/432/433

MAXIMUM RATINGS

Characteristics	Symbol	IRF830 IRFP430	IRF831 IRFP431	IRF832 IRFP432	IRF833 IRFP433	Unit
Drain-Source Voltage (1)	V_{DSS}	500	450	500	450	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	500	450	500	450	Vdc
Gate-Source Voltage	V_{GS}	± 20				Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	4.5	4.5	4.0	4.0	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	3.0	3.0	2.5	2.5	Adc
Drain Current—Pulsed (3)	I_{DM}	18	18	16	16	Adc
Gate Current—Pulsed	I_{GM}	± 1.5				Adc
Single Pulsed Avalanche Energy(4)	E_{AS}	280				mJ
Avalanche Current	I_{AS}	4.5				A
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	75 0.6				Watts W/ $^\circ C$
Operating and Storage Junction to Case	T_J, T_{stg}	-55 to 150				$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300				$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=25\text{ mH}$, $V_{dd}=50V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV_{DS}	Drain-Source Breakdown Voltage IRF830/IRFP430 IRF832/IRFP432	500	—	—	V	$V_{GS}=0V$ $I_D=250\mu A$
	IRF831/IRFP431 IRF833/IRFP433	450	—	—	V	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}$, $I_D=250\mu A$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS}=20V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	$V_{GS}=-20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS}=\text{Max. Rating}$, $V_{GS}=0V$
		—	—	1000	μA	$V_{DS}=\text{Max. Rating} \times 0.8$, $V_{GS}=0V$, $T_C=125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2) IRF830/IRFP430 IRF831/IRFP431	4.5	—	—	A	$V_{DS} \geq 9V$, $V_{GS}=10V$
	IRF832/IRFP432 IRF833/IRFP433	4.0	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance (2) IRF830/IRFP430 IRF831/IRFP431	—	0.95	1.5	Ω	$V_{GS}=10V$, $I_D=2.5A$
	IRF832/IRFP432 IRF833/IRFP433	—	1.4	2.0	Ω	
g_{fs}	Forward Transconductance (2)	2.5	3.2	—	μ	$V_{DS} \geq 50V$, $I_D=2.5A$
C_{iss}	Input Capacitance	—	780	—	pF	$V_{GS}=0V$, $V_{DS}=25V$, $f=1.0\text{MHz}$
C_{oss}	Output Capacitance	—	86	—	pF	
C_{rss}	Reverse Transfer Capacitance	—	38	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	11	17	ns	$V_{DD}=0.5BV_{DS}$, $I_D=4.5A$, $Z_O=12\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	15	23	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	35	53	ns	
t_f	Fall Time	—	15	23	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	21	32	nC	$V_{GS}=10V$, $I_D=4.5A$, $V_{DS}=0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	3.2	4.8	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	11	17	nC	

THERMAL RESISTANCE

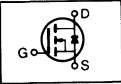
Symbol	Characteristic		IRF830-3	IRFP430-3	Unit	
R_{thJC}	Junction-to-Case	MAX.	1.67	1.67	K/W	
R_{thCS}	Case-to-Sink	TYP	0.50	0.24	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	MAX	80	40	K/W	Free Air Operation

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C

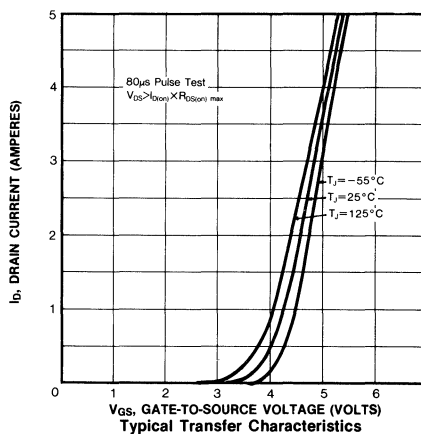
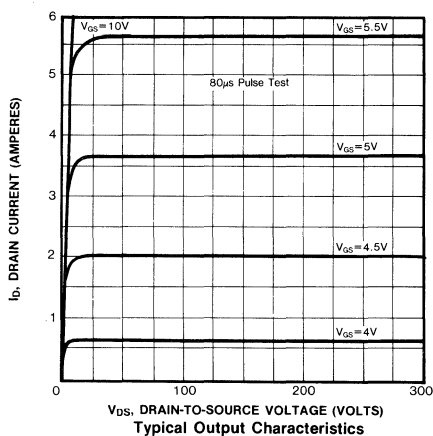
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

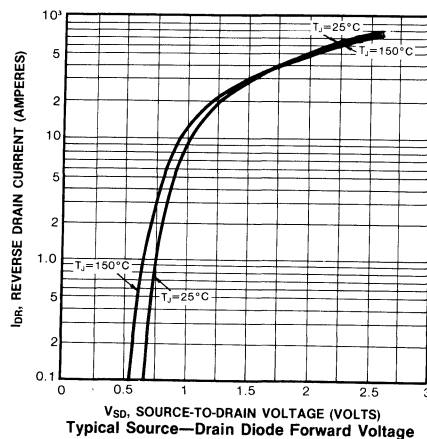
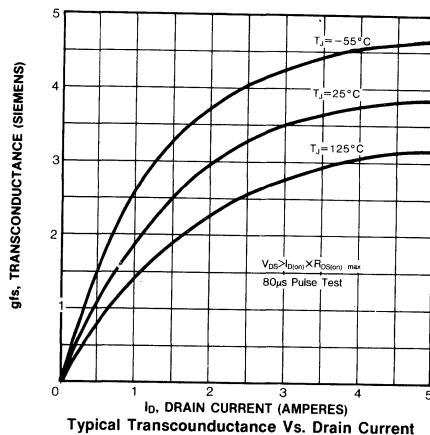
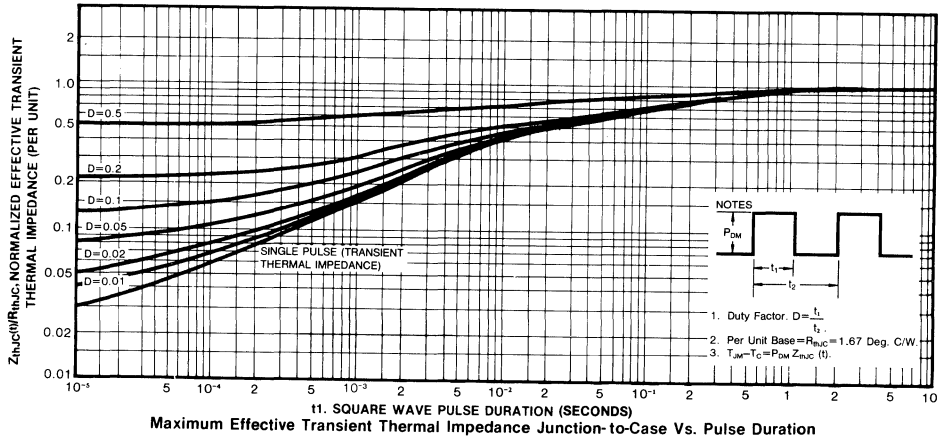
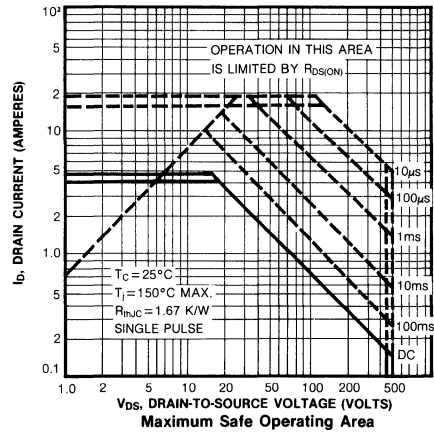
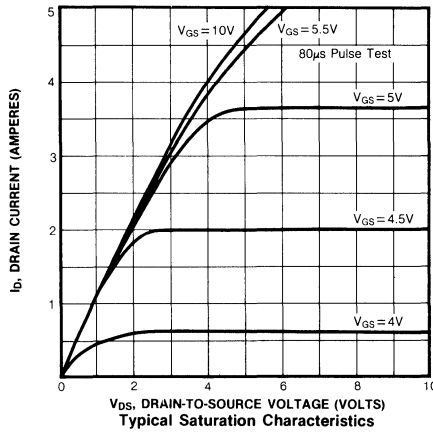
(3) Repetitive rating: Pulse width limited by max. junction temperature

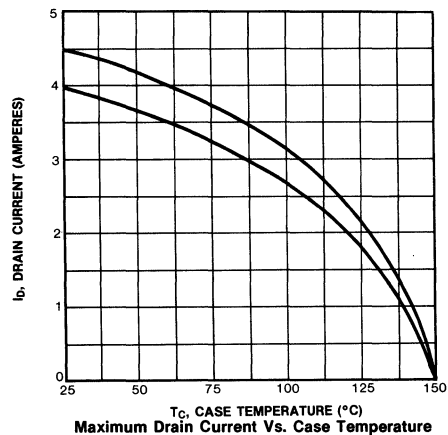
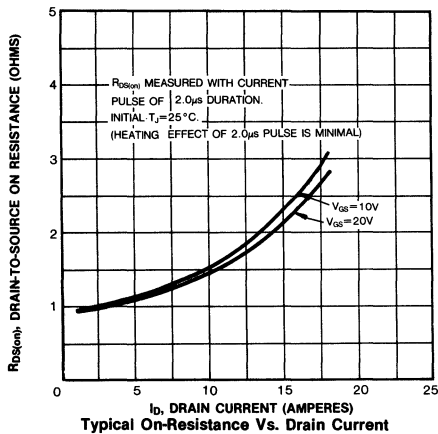
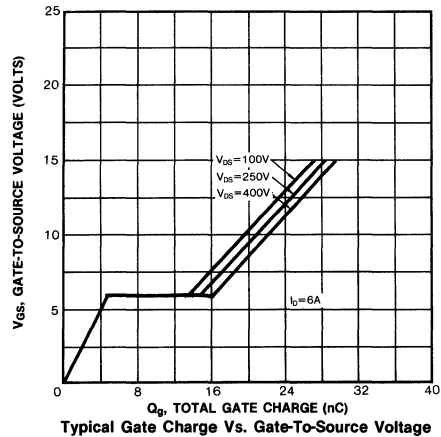
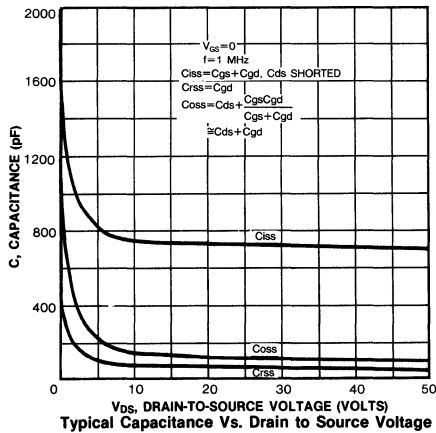
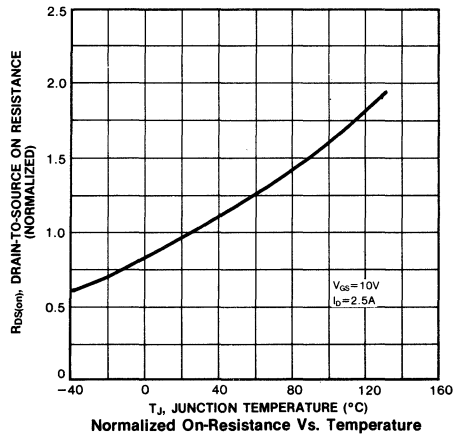
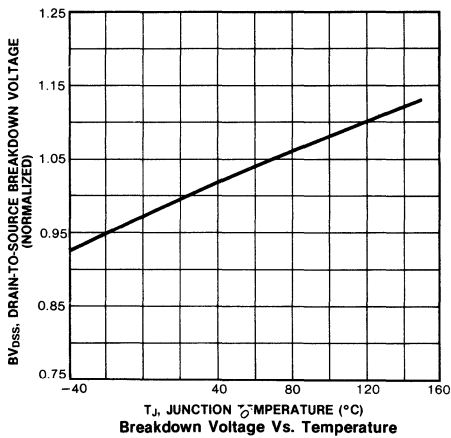
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

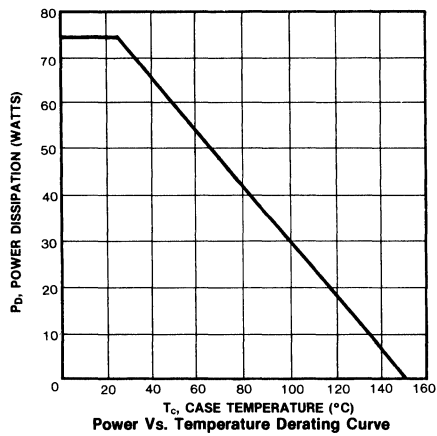
Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode) IRF830/IRFP430 IRF831/IRFP431	—	—	4.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier 
	IRF832/IRFP432 IRF833/IRFP433	—	—	4.0	A	
I_{SM}	Pulse Source Current(Body Diode)(3) IRF830/IRFP430 IRF831/IRFP431	—	—	18	A	
	IRF832/IRFP432 IRF833/IRFP433	—	—	16	A	
V_{SD}	Diode Forward Voltage (2) IRF830/IRFP430 IRF831/IRFP431	—	—	1.6	V	$T_C=25^\circ\text{C}$, $I_S=4.5\text{A}$, $V_{GS}=0\text{V}$
	IRF832/IRFP432 IRF833/IRFP433	—	—	1.5	V	$T_C=25^\circ\text{C}$, $I_S=4.0\text{A}$, $V_{GS}=0\text{V}$
t_{rr}	Reverse Recovery Time	—	370	760	ns	$T_J=25^\circ\text{C}$, $I_F=4.5\text{A}$, $dI_F/dt=100\text{A}/\mu\text{S}$

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
 (3) Repetitive rating: Pulse with limited by max. junction temperature









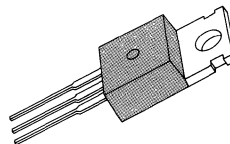
FEATURES

- Lower $R_{DS(ON)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

PRODUCT SUMMARY

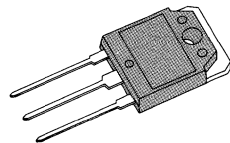
Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF840/IRFP440	500V	0.85Ω	8.0A
IRF841/IRFP441	450V	0.85Ω	8.0A
IRF842/IRFP442	500V	1.10Ω	7.0A
IRF843/IRFP443	450V	1.10Ω	7.0A

TO-220



IRF840/841/842/843

TO-3P



IRFP440/441/442/443

MAXIMUM RATINGS

Characteristics	Symbol	IRF840 IRFP440	IRF841 IRFP441	IRF842 IRFP442	IRF843 IRFP443	Unit
Drain-Source Voltage (1)	V_{DS}	500	450	500	450	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	500	450	500	450	Vdc
Gate-Source Voltage	V_{GS}	± 20				Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	8.0	8.0	7.0	7.0	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	5.0	5.0	4.0	4.0	Adc
Drain Current—Pulsed (3)	I_{DM}	32	32	28	28	Adc
Gate Current—Pulsed	I_{GM}	± 1.5				Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	510				mJ
Avalanche Current	I_{AS}	8.0				A
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	125 1.0				Watts W/ $^\circ C$
Operating and Storage Junction to Case	T_J, T_{stg}	-55 to 150				$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300				$^\circ C$

- Notes:** (1) $T_J=25^\circ C$ to $150^\circ C$
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature
(4) $L=1.4$ mH, $V_{dd}=50V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV_{DS}	Drain-Source Breakdown Voltage IRF840/IRFP440 IRF842/IRFP442	500	—	—	V	$V_{GS}=0V$ $I_D=250\mu A$
	IRF841/IRFP441 IRF843/IRFP443	450	—	—	V	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}$, $I_D=250\mu A$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS}=20V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	$V_{GS}=-20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS}=\text{Max. Rating}$, $V_{GS}=0V$
		—	—	1000	μA	$V_{DS}=\text{Max. Rating} \times 0.8$, $V_{GS}=0V$, $T_C=125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2) IRF840/IRFP440 IRF841/IRFP441	8.0	—	—	A	$V_{DS} \geq 8.8V$, $V_{GS}=10V$
	IRF842/IRFP442 IRF843/IRFP443	7.0	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance (2) IRF840/IRFP440 IRF841/IRFP441	—	0.76	0.85	Ω	$V_{GS}=10V$, $I_D=4.0A$
	IRF842/IRFP442 IRF843/IRFP443	—	0.85	1.1	Ω	
g_{fs}	Forward Transconductance (2)	4.0	6.5	—	S	$V_{DS} \geq 50V$, $I_D=4.0A$
C_{iss}	Input Capacitance	—	1510	—	pF	$V_{GS}=0V$, $V_{DS}=25V$, $f=1.0\text{MHz}$
C_{oss}	Output Capacitance	—	154	—	pF	
C_{rss}	Reverse Transfer Capacitance	—	66	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	14	21	ns	$V_{DD}=0.5BV_{DS}$, $I_D=8.0A$, $Z_O=19\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	23	35	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	49	74	ns	
t_f	Fall Time	—	20	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	42	63	nC	$V_{GS}=10V$, $I_D=8.0A$, $V_{DS}=0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	6.2	9.3	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	22	32	nC	

THERMAL RESISTANCE

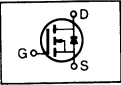
Symbol	Characteristic		IRF840-3	IRFP440-3	Unit	
R_{thJC}	Junction-to-Case	MAX	1.0	1.0	K/W	
R_{thCS}	Case-to-Sink	TYP	0.5	0.24	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	MAX	80	40	K/W	Free Air Operation

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C

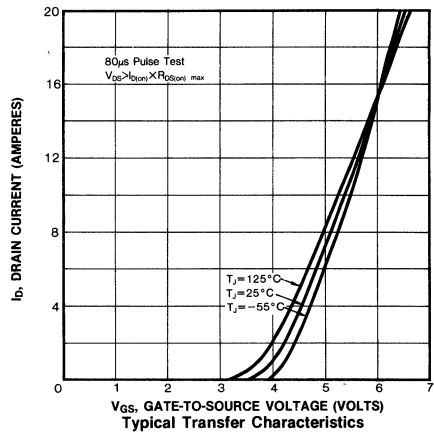
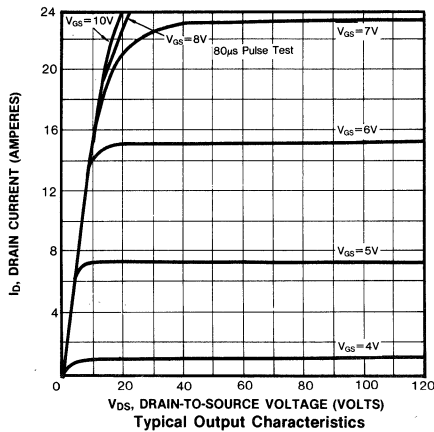
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

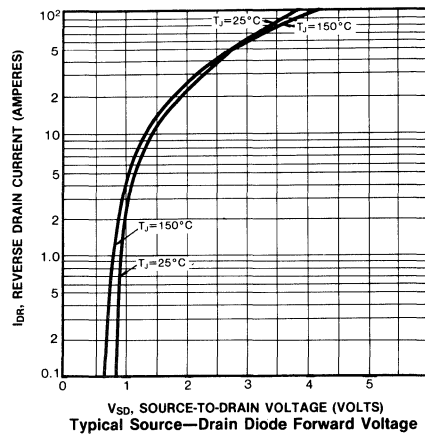
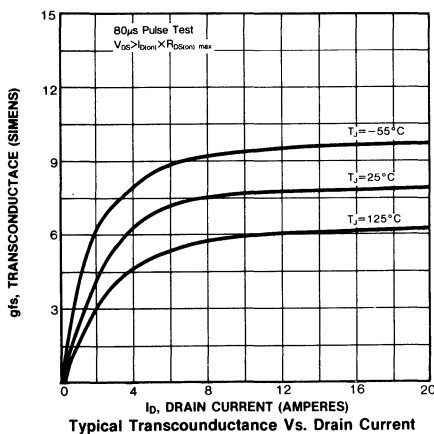
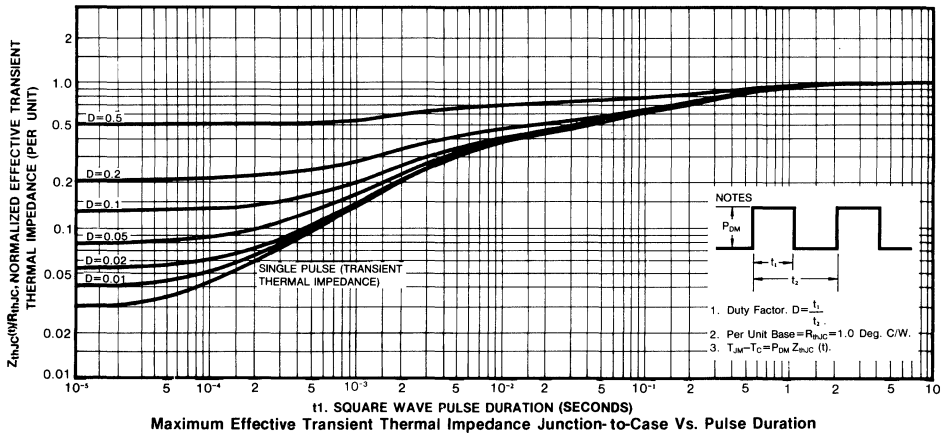
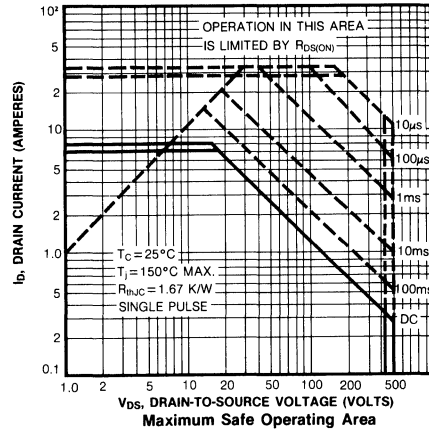
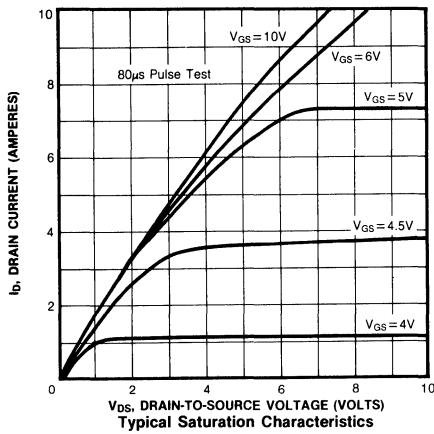
(3) Repetitive rating: Pulse width limited by max. junction temperature

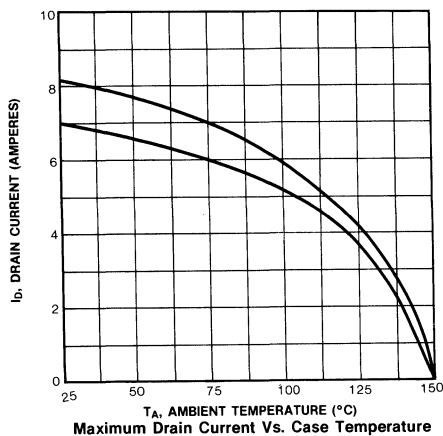
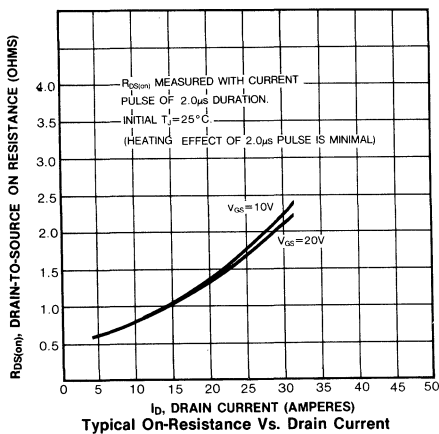
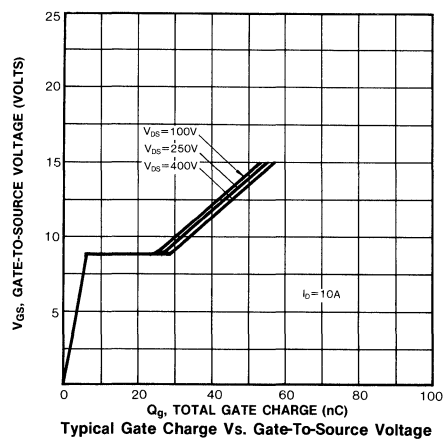
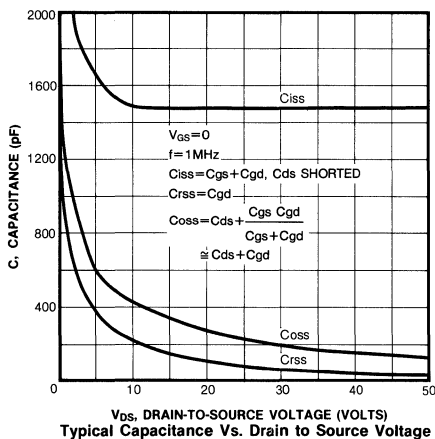
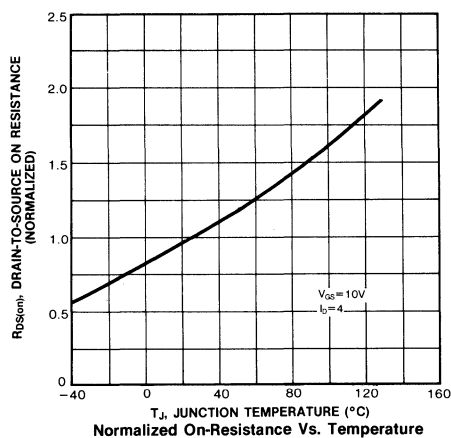
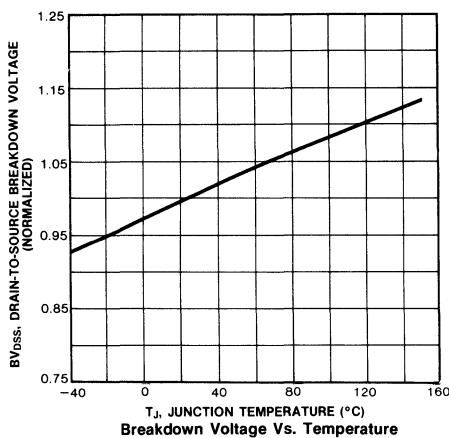
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

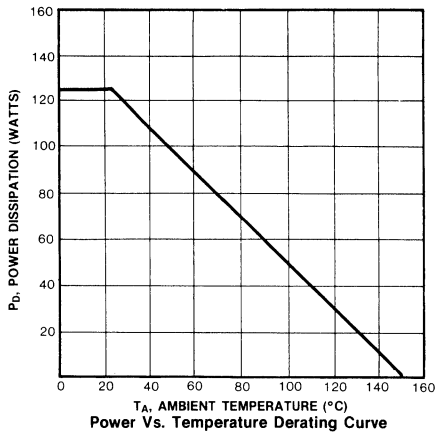
Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode) IRF840/IRFP440 IRF841/IRFP441	—	—	8.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier 
	IRF842/IRFP442 IRF843/IRFP443	—	—	7.0	A	
I_{SM}	Pulse Source Current(Body Diode)(3) IRF840/IRFP440 IRF841/IRFP441	—	—	32	A	
	IRF842/IRFP442 IRF843/IRFP443	—	—	28	A	
V_{SD}	Diode Forward Voltage (2) IRF840/IRFP440 IRF841/IRFP441	—	—	2.0	V	$T_C=25^{\circ}\text{C}$, $I_S=8.0\text{A}$, $V_{GS}=0\text{V}$
	IRF842/IRFP442 IRF843/IRFP443	—	—	1.9	V	$T_C=25^{\circ}\text{C}$, $I_S=7.0\text{A}$, $V_{GS}=0\text{V}$
t_{rr}	Reverse Recovery Time	—	460	970	ns	$T_J=25^{\circ}\text{C}$, $I_F=8.0\text{A}$, $dI_F/dt=100\text{A}/\mu\text{S}$

Notes: (1) $T_J=25^{\circ}\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature





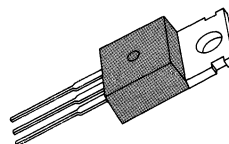




FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

TO-220



IRF9510/9511/9512/9513

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF9510	-100V	1.2Ω	-3.0
IRF9511	-60V	1.2Ω	-3.0
IRF9512	-100V	1.6Ω	-2.5A
IRF9513	-60V	1.6Ω	-2.5A

MAXIMUM RATINGS

Characteristic	Symbol	IRF9510	IRF9511	IRF9512	IRF9513	Unit
Drain-Source Voltage (1)	V_{DSS}	-100	-60	-100	-60	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	-100	-60	-100	-60	Vdc
Gate-Source Voltage	V_{GS}	± 20				Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	-6.0	-6.0	-5.0	-5.0	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	-4.0	-4.0	-2.5	-3.5	Adc
Drain Current—Pulsed (3)	I_{DM}	-24	-24	-20	-20	Adc
Gate Current—Pulsed	I_{GM}	± 1.5				Adc
Single Pulsed Avalanche Energy(4)	E_{AS}	167				mJ
Avalanche Current	I_{AS}	-3.0				A
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	20 0.16				Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150				$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300				$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=29mH$, $V_{dd}=-25V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-Source Breakdown Voltage IRF9510/9512	-100	—	—	V	V _{GS} =0V I _D =-250μA
	IRF9511/9513	-60	—	—	V	
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} =V _{GS} , I _D =-250μA
I _{GSS}	Gate-Source Leakage Forward	—	—	100	nA	V _{GS} =-20V
I _{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	V _{GS} =20V
I _{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	V _{DS} =Max. Rating, V _{GS} =0V
		—	—	1000	μA	V _{DS} =Max. Rating×0.8, V _{GS} =0V, T _C =125°C
I _{D(on)}	On-State Drain-Source Current (2) IRF9510/9511	-3.0	—	—	A	V _{DS} ≤-4.8V, V _{GS} =10V
	IRF9512/9513	-2.5	—	—	A	
R _{DS(on)}	Static Drain-Source On-State Resistance (2) IRF9510/9511	—	—	1.2	Ω	V _{GS} =-10V, I _D =-1.5A
	IRF9512/9513	—	—	1.6	Ω	
g _{fs}	Forward Transconductance (2)	0.76	—	—	∩	V _{DS} ≤-50V, I _D =-1.5A
C _{iss}	Input Capacitance	—	250	—	pF	V _{GS} =0V, V _{DS} =-25V, f=1.0MHz
C _{oss}	Output Capacitance	—	92	—	pF	
C _{rss}	Reverse Transfer Capacitance	—	51	—	pF	
t _{d(on)}	Turn-On Delay Time	—	15	39	ns	V _{DD} =0.5BV _{DSS} , I _D =-1.5A, Z _O =50Ω (MOSFET switching times are essentially independent of operating temperature)
t _r	Rise Time	—	30	60	ns	
t _{d(off)}	Turn-Off Delay Time	—	20	40	ns	
t _f	Fall Time	—	20	40	ns	
Q _g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	11	—	nC	V _{GS} =-15V, I _D =-4.0A, V _{DS} =0.8 Max. Rating (Gate charge is essentially independent of operating temperature.)
Q _{gs}	Gate-Source Charge	—	4.0	—	nC	
Q _{gd}	Gate-Drain ("Miller") Charge	—	7.0	—	nC	

THERMAL RESISTANCE

R _{thJC}	Junction-to-Case	—	—	6.4	K/W	
R _{thCS}	Case-to-Sink	—	1.0	—	K/W	Mounting surface flat, smooth, and greased
R _{thJA}	Junction-to-Ambient	—	—	80	K/W	Free Air Operation

Notes: (1) T_J=25°C to 150°C

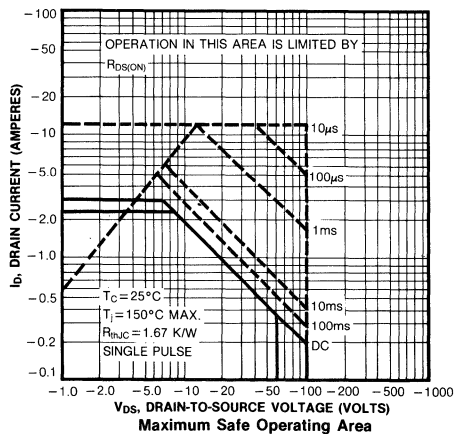
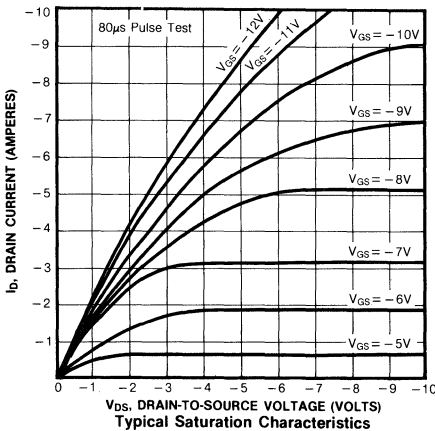
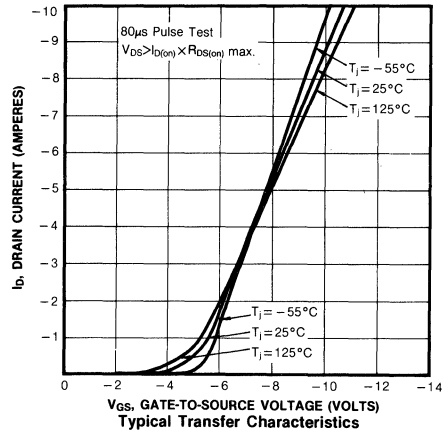
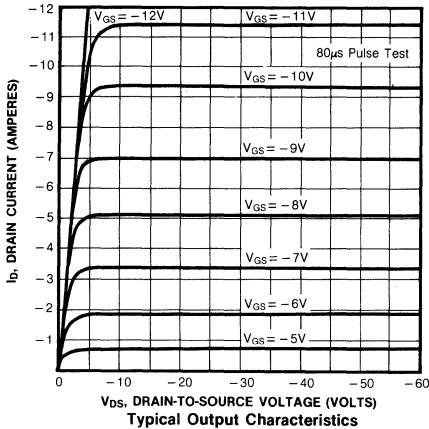
(2) Pulse test: Pulse width≤300μs, Duty Cycle≤2%

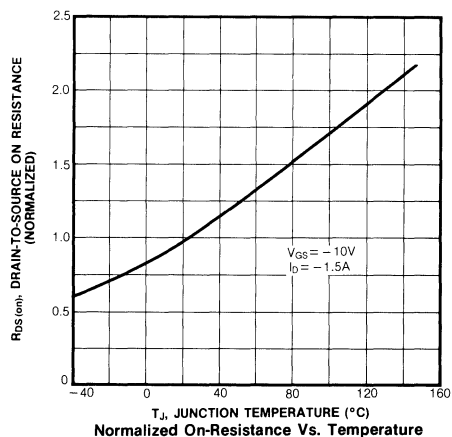
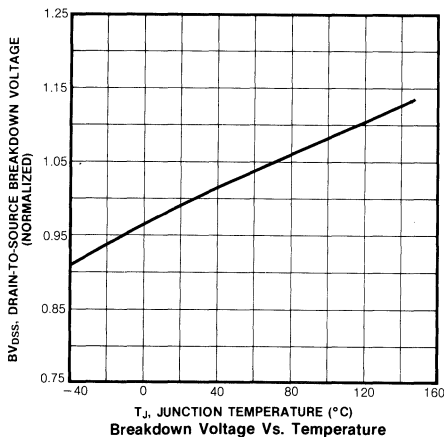
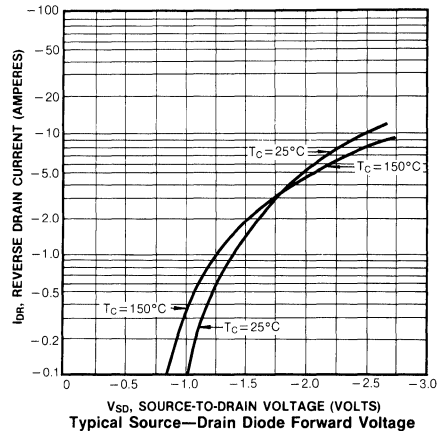
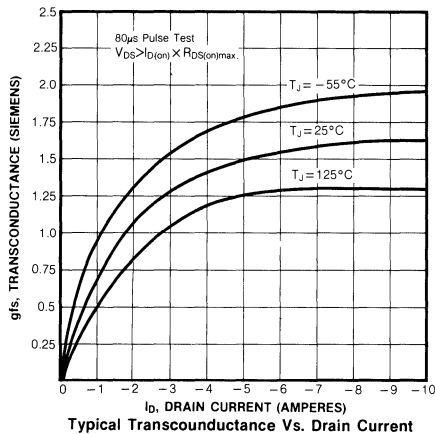
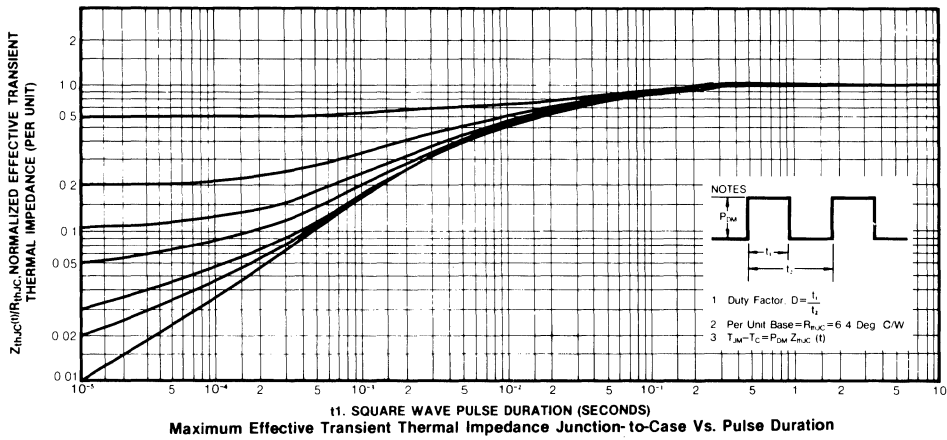
(3) Repetitive rating: Pulse width limited by max. junction temperature

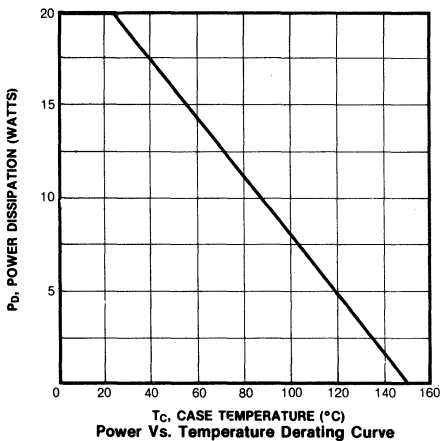
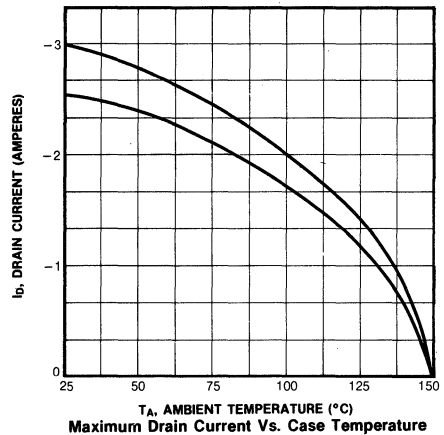
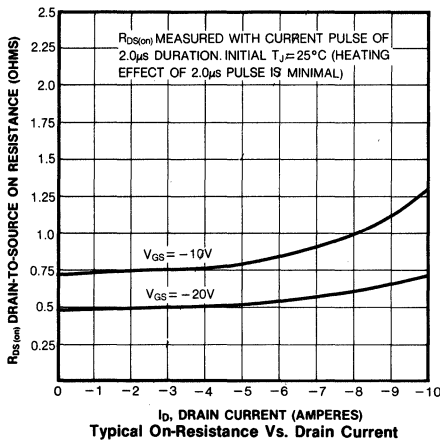
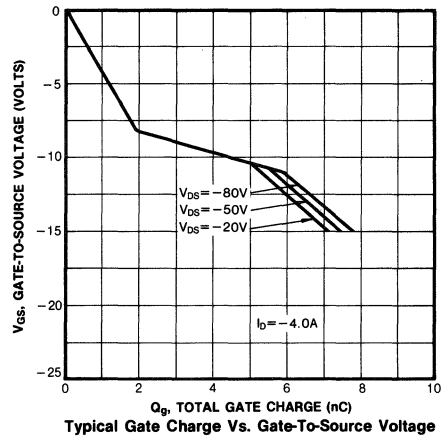
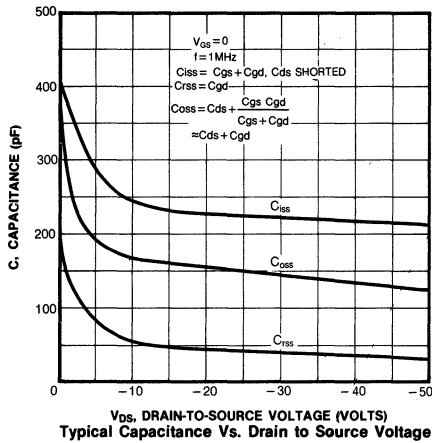
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode) IRF9510/9511	—	—	-3.0	A	Modified MOSFET showing the integral reverse P-N junction rectifier 
	IRF9512/9513	—	—	-2.5	A	
I_{SM}	Pulse Source Current (Body Diode)(3) IRF9510/9511	—	—	12	A	$T_C = 25^\circ\text{C}$, $I_S = -3.0\text{A}$, $V_{GS} = 0\text{V}$
	IRF9512/9513	—	—	10	A	
V_{SD}	Diode Forward Voltage (2) IRF9510/9511	—	—	-5.5	V	$T_C = 25^\circ\text{C}$, $I_S = -2.5\text{A}$, $V_{GS} = 0\text{V}$
	IRF9512/9513	—	—	-5.3	V	$T_C = 25^\circ\text{C}$, $I_S = -2.5\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	120	—	ns	$T_J = 150^\circ\text{C}$, $I_F = -3.0\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$

Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature



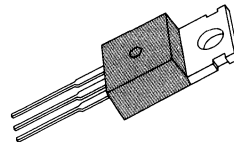




FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

TO-220



IRF9520/9521/9522/9523

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF9520	-100V	0.6Ω	-6.0A
IRF9512	-60V	0.6Ω	-6.0A
IRF9525	-100V	0.8Ω	-5.0A
IRF9523	-60V	0.8Ω	-5.0A

MAXIMUM RATINGS

Characteristic	Symbol	IRF9520	IRF9521	IRF9522	IRF9523	Unit
Drain-Source Voltage (1)	V_{DSS}	-100	-60	-100	-60	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	-100	-60	-100	-60	Vdc
Gate-Source Voltage	V_{GS}	± 20				Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	-6.0	-6.0	-5.0	-5.0	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	-4.0	-4.0	-3.5	-3.5	Adc
Drain Current—Pulsed (3)	I_{DM}	-24	-24	-20	-20	Adc
Gate Current—Pulsed	I_{GM}	± 1.5				Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	380				mJ
Avalanche Current	I_{AS}	-6.0				A
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	40 0.32				Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150				$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300				$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=16mH$, $V_{dd}=-25V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-Source Breakdown Voltage IRF9520 IRF9522	-100	—	—	V	V _{GS} =0V I _D =-250μA
	IRF9521 IRF9523	-60	—	—	V	
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} =V _{GS} , I _D =-250μA
I _{GSS}	Gate-Source Leakage Forward	—	—	100	nA	V _{GS} =-20V
I _{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	V _{GS} =20V
I _{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	V _{DS} =Max. Rating, V _{GS} =0V
		—	—	1000	μA	V _{DS} =Max. Rating×0.8, V _{GS} =0V, T _C =125°C
I _{D(on)}	On-State Drain-Source Current (2) IRF9520 IRF9522	-6.0	—	—	A	V _{DS} ≤-4.8V, V _{GS} =-10V
	IRF9521 IRF9523	-5.0	—	—	A	
R _{DS(on)}	Static Drain-Source On-State Resistance (2) IRF9520 IRF9522	—	—	0.6	Ω	V _{GS} =-10V, I _D =-3.0A
	IRF9521 IRF9523	—	—	0.8	Ω	
g _{fs}	Forward Transconductance (2)	0.9	—	—	Ω	V _{DS} ≤-50V, I _D =-3.0A
C _{iss}	Input Capacitance	—	427	—	pF	V _{GS} =0V, V _{DS} =-25V, f=1.0MHz
C _{oss}	Output Capacitance	—	128	—	pF	
C _{rss}	Reverse Transfer Capacitance	—	44.5	—	pF	
t _{d(on)}	Turn-On Delay Time	—	—	50	ns	V _{DD} =0.5BV _{DSS} , I _D =-3.0A, Z _O =50Ω (MOSFET switching times are essentially independent of operating temperature)
t _r	Rise Time	—	—	100	ns	
t _{d(off)}	Turn-Off Delay Time	—	—	100	ns	
t _f	Fall Time	—	—	15	ns	
Q _g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	—	12	nC	V _{GS} =-15V, I _D =-8.0A, V _{DS} =0.8 Max. Rating (Gate charge is essentially independent of operating temperature.)
Q _{gs}	Gate-Source Charge	—	—	9	nC	
Q _{gd}	Gate-Drain ("Miller") Charge	—	—	7	nC	

THERMAL RESISTANCE

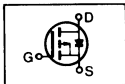
Symbol	Characteristic		IRF9520-3	Unit	
R _{thJC}	Junction-to-Case	MAX	3.12	K/W	
R _{thCS}	Case-to-Sink	TYP	1.0	K/W	Mounting surface flat, smooth, and greased
R _{thJA}	Junction-to-Ambient	MAX	80	K/W	Free Air Operation

Notes: (1) T_J=25°C to 150°C

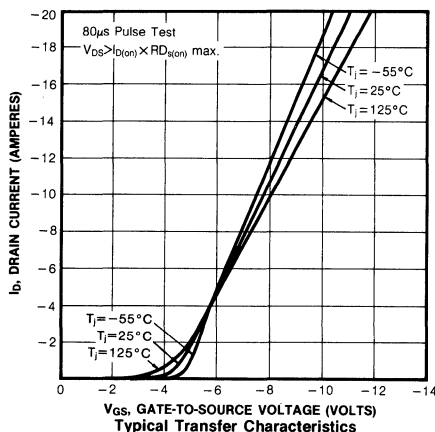
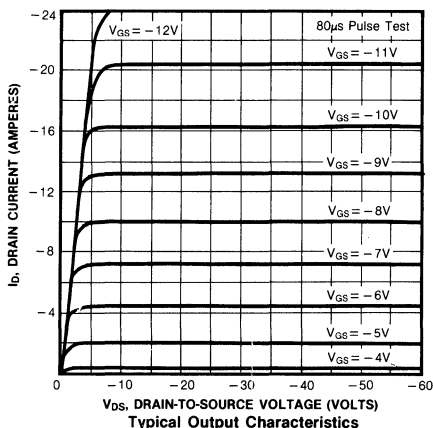
(2) Pulse test: Pulse width≤300μs, Duty Cycle≤2%

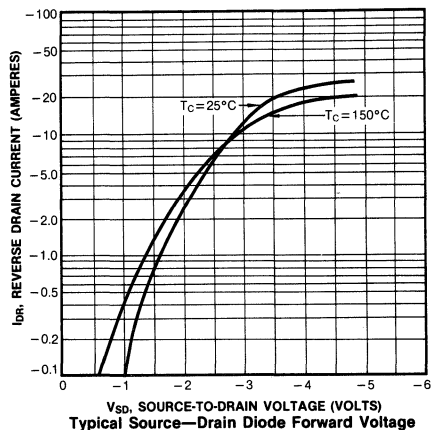
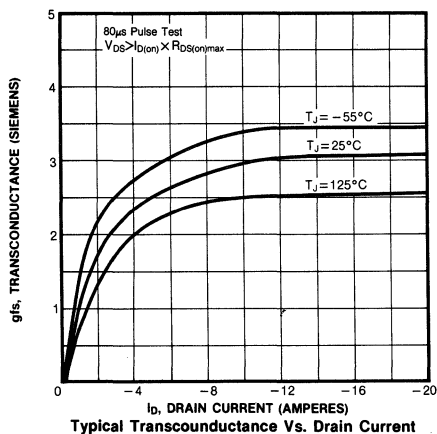
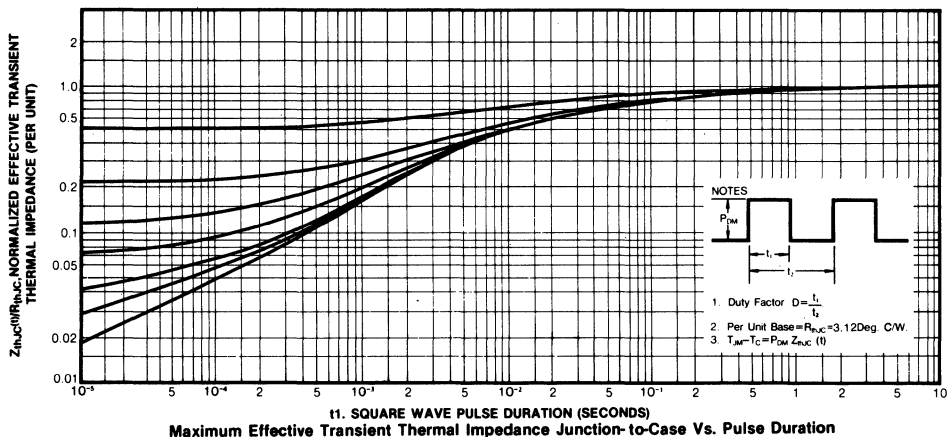
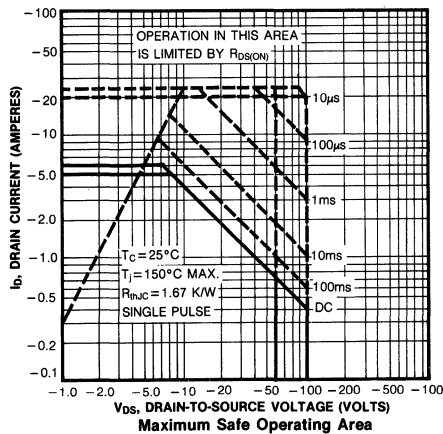
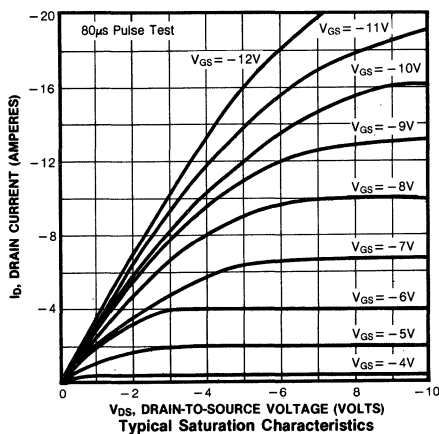
(3) Repetitive rating: Pulse width limited by max. junction temperature

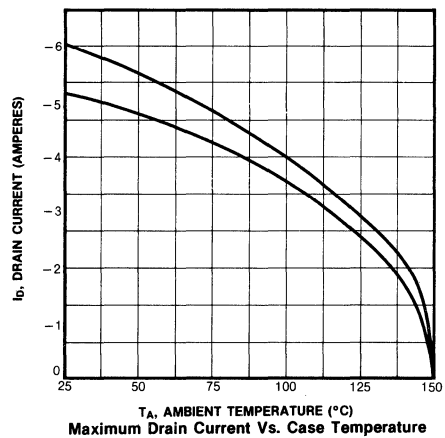
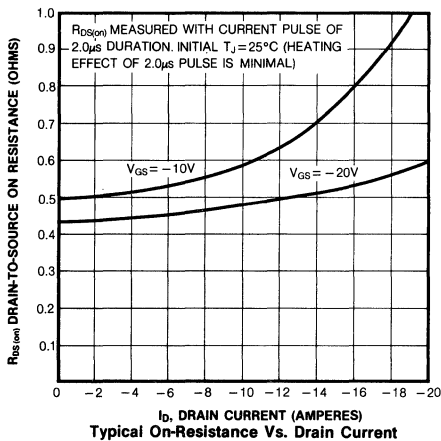
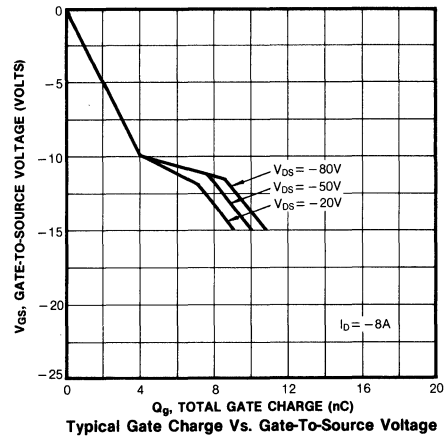
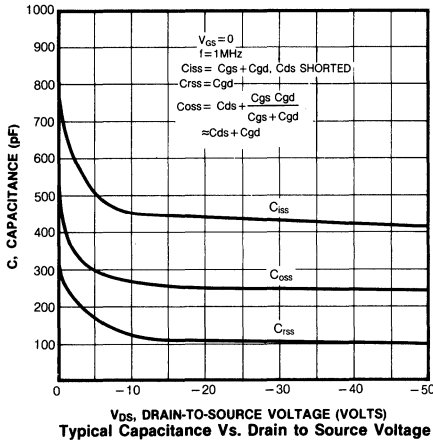
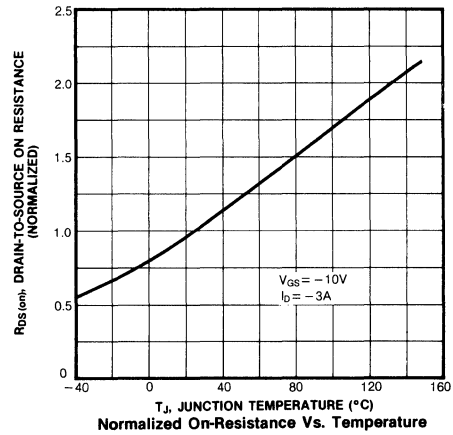
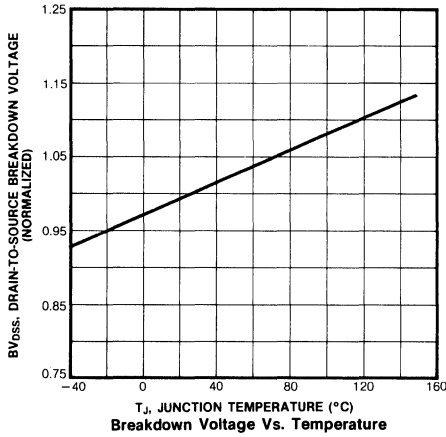
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

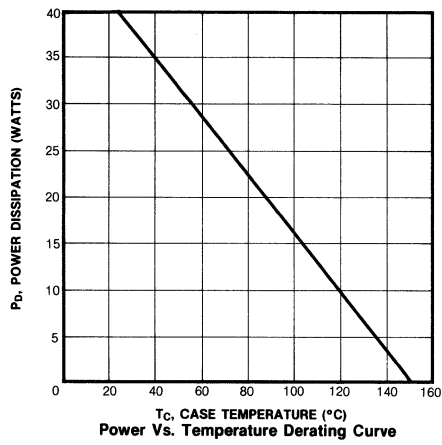
Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode) IRF9520 IRF9521	—	—	-60	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier 
	IRF9522 IRF9523	—	—	-5.0	A	
I_{SM}	Pulse Source Current (Body Diode) (3) IRF9520 IRF9521	—	—	-24	A	
	IRF9522 IRF9523	—	—	-20	A	
V_{SD}	Diode Forward Voltage (2) IRF9520 IRF9521	—	—	-6.3	A	$T_C=25^\circ\text{C}$, $I_S=-6.0\text{A}$, $V_{GS}=0\text{V}$
	IRF9522 IRF9523	—	—	-6.0	A	$T_C=25^\circ\text{C}$, $I_S=-5.0\text{A}$, $V_{GS}=0\text{V}$
t_{rr}	Reverse Recovery Time	—	230	—	ns	$T_J=150^\circ\text{C}$, $I_F=-6.0\text{A}$, $dI_F/dt=100\text{A}/\mu\text{S}$

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature









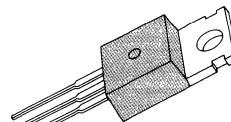
FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

PRODUCT SUMMARY

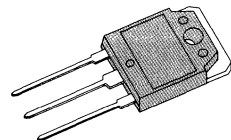
Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF9530/IRFP9130	-100V	0.30Ω	-12A
IRF9531/IRFP9131	-60V	0.30Ω	-12A
IRF9532/IRFP9132	-100V	0.40Ω	-10A
IRF9533/IRFP9133	-60V	0.40Ω	-10A

TO-220



IRF9530/9531/9532/9533

TO-3P



IRFP9130/9131/9132/9133

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MAXIMUM RATINGS

Characteristic	Symbol	IRF9530 IRFP9130	IRF9531 IRFP9131	IRF9532 IRFP9132	IRF9533 IRFP9133	Unit
Drain-Source Voltage (1)	V_{DSS}	-100	-60	-100	-60	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	-100	-60	-100	-60	Vdc
Gate-Source Voltage	V_{GS}	± 20				Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	-12	-12	-10	-10	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	-7.5	-7.5	-6.5	-6.5	Adc
Drain Current—Pulsed (3)	I_{DM}	-48	-48	-40	-40	Adc
Gate Current—Pulsed	I_{GM}	± 1.5				Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	550				mJ
Avalanche Current	I_{AS}	-12				A
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	75 0.6				Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150				$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300				$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=8.5mH$, $V_{dd}=-25V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV_{DS}	Drain-Source Breakdown Voltage IRF9530/IRFP9130 IRF9532/IRFP9132	-100	—	—	V	$V_{GS}=0V$ $I_D=-250\mu A$
	IRF9531/IRFP9131 IRF9533/IRFP9133	-60	—	—	V	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}$, $I_D=-250\mu A$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS}=-20V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	$V_{GS}=20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS}=\text{Max. Rating}$, $V_{GS}=0V$
		—	—	1000	μA	$V_{DS}=\text{Max. Rating} \times 0.8$, $V_{GS}=0V$, $T_C=125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2) IRF9530/IRFP9130 IRF9531/IRFP9131	-12	—	—	A	$V_{DS} \leq -4.8V$, $V_{GS}=-10V$
	IRF9532/IRFP9132 IRF9533/IRFP9133	-10	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance (2) IRF9530/IRFP9130 IRF9531/IRFP9131	—	—	0.3	Ω	$V_{GS}=-10V$, $I_D=-6.5A$
	IRF9532/IRFP9132 IRF9533/IRFP9133	—	—	0.4	Ω	
g_{fs}	Forward Transconductance (2)	2.0	—	—	S	$V_{DS} \leq -50V$, $I_D=-6.5A$
C_{iss}	Input Capacitance	—	835	—	pF	$V_{GS}=0V$, $V_{DS}=-25V$, $f=1.0\text{MHz}$
C_{oss}	Output Capacitance	—	357	—	pF	
C_{rss}	Reverse Transfer Capacitance	—	94	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	—	60	ns	$V_{DD}=0.5BV_{DS}$, $I_D=-6.5A$, $Z_O=50\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	—	140	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	—	140	ns	
t_f	Fall Time	—	—	140	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	—	45	nC	$V_{GS}=-15V$, $I_D=-15A$, $V_{DS}=0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	—	20	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	—	25	nC	

THERMAL RESISTANCE

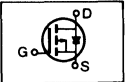
Symbol	Characteristic		IRF9530-3	IRFP9130-3	Unit	
R_{thJC}	Junction-to-Case	MAX	1.67	1.67	K/W	
R_{thCS}	Case-to-Sink	TYP	1.0	0.24	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	MAX	80	40	K/W	Free Air Operation

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C

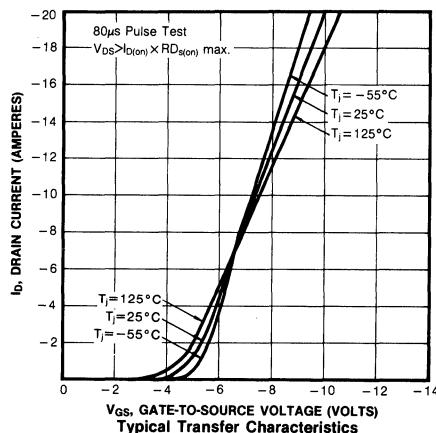
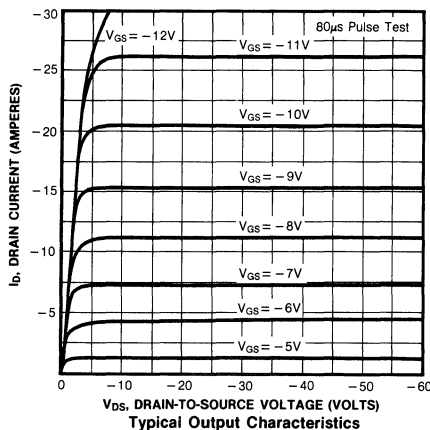
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

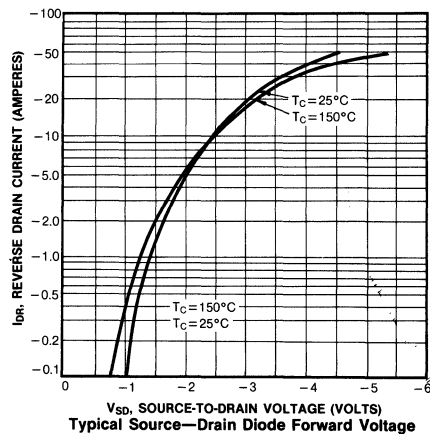
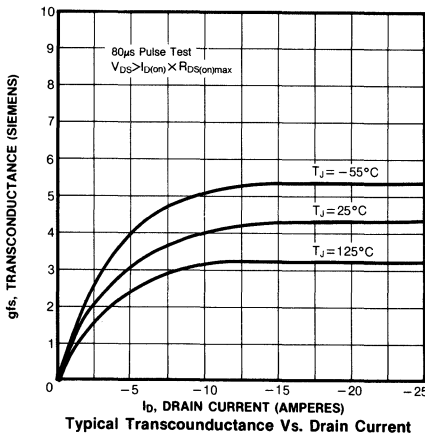
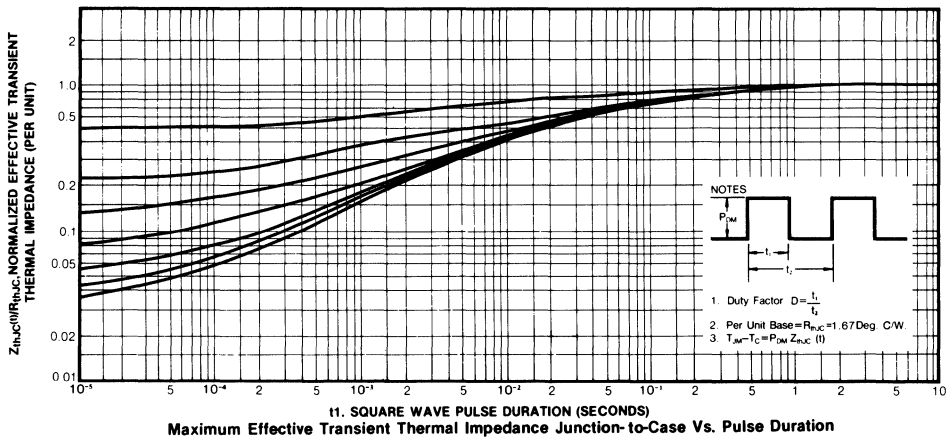
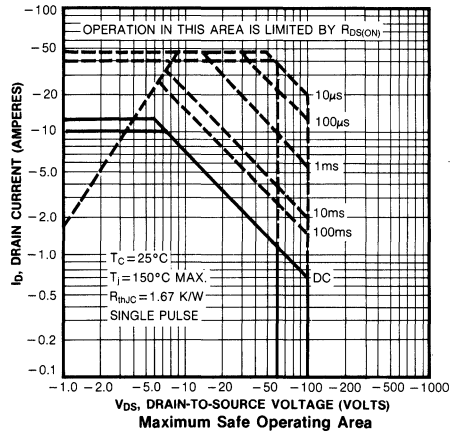
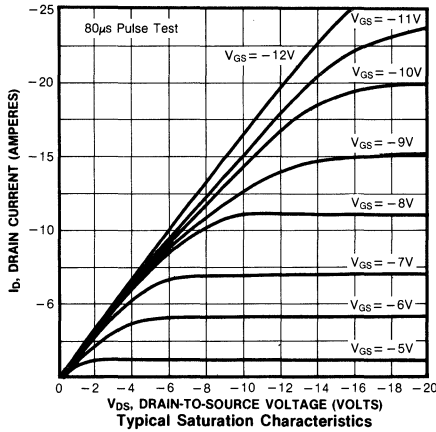
(3) Repetitive rating: Pulse width limited by max. junction temperature

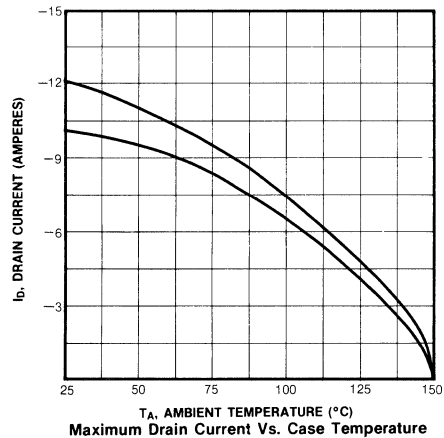
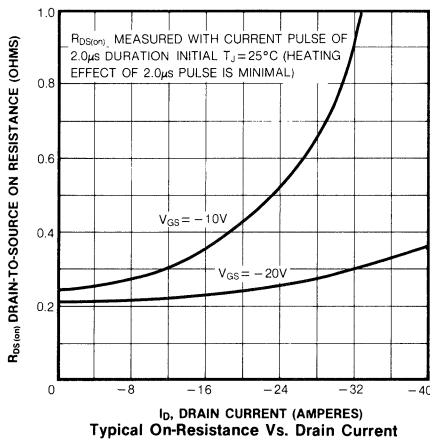
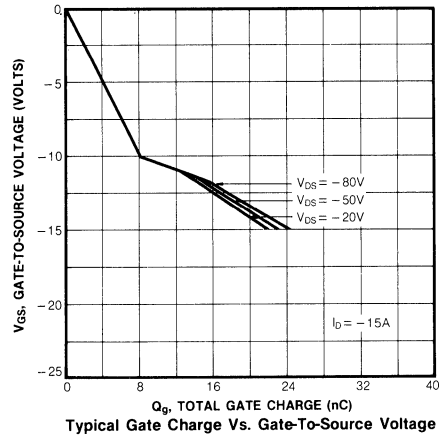
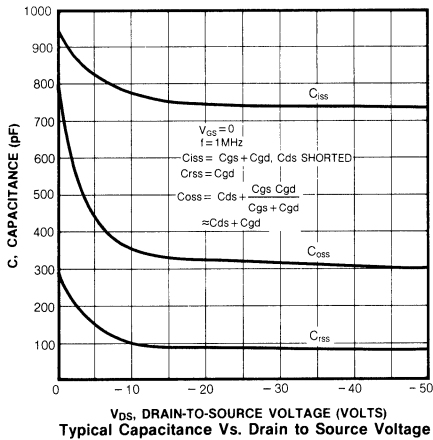
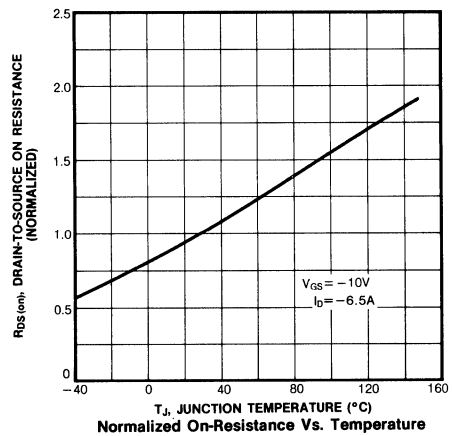
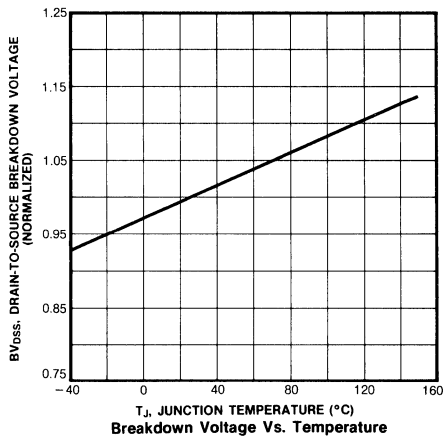
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

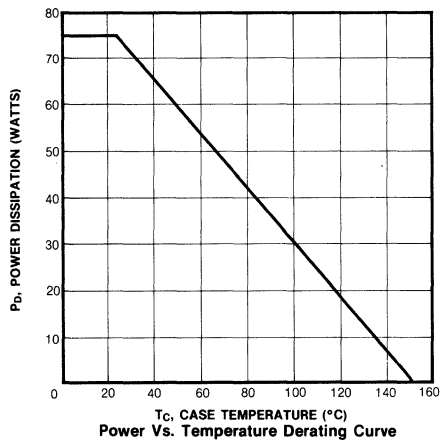
Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode) IRF9530/IRFP9130 IRF9531/IRFP9131	—	—	-12	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier 
	IRF9532/IRFP9132 IRF9533/IRFP9133	—	—	-10	A	
I_{SM}	Pulse Source Current (Body Diode) (3) IRF9530/IRFP9130 IRF9531/IRFP9131	—	—	-48	A	
	IRF9532/IRFP9132 IRF9533/IRFP9133	—	—	-40	A	
V_{SD}	Diode Forward Voltage (2) IRF9530/IRFP9130 IRF9531/IRFP9131	—	—	-6.3	A	$T_C = 25^\circ\text{C}$, $I_S = -12\text{A}$, $V_{GS} = 0\text{V}$
	IRF9532/IRFP9132 IRF9533/IRFP9133	—	—	-6.0	A	$T_C = 25^\circ\text{C}$, $I_S = -10\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	300	—	ns	$T_J = 150^\circ\text{C}$, $I_F = -6.0\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$

Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature









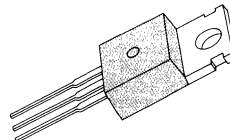
FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

PRODUCT SUMMARY

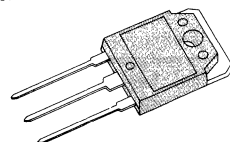
Part Number	V_{DS}	$R_{DS(on)}$	I_D
	-100V	0.2 Ω	-19A
IRF9541/IRFP9141	-60V	0.2 Ω	-19A
IRF9542/IRFP9142	-100V	0.3 Ω	-15A
IRF9543/IRFP9143	-60V	0.3 Ω	-15A

TO-220



IRF9540/9541/9542/9543

TO-3P



IRFP9140/9141/9142/9143

2

MAXIMUM RATINGS

Characteristic	Symbol		IRF9541 IRFP9141	IRF9542 IRFP9142	IRF9543 IRFP9143	Unit
Drain-Source Voltage (1)	V_{DSS}	-100	-60	-100	-60	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	-100	-60	-100	-60	Vdc
Gate-Source Voltage	V_{GS}	± 20				Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	-19	-19	-15	-15	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	-12	-12	-10	-10	Adc
Drain Current—Pulsed (3)	I_{DM}	-70	-70	-60	-60	Adc
Gate Current—Pulsed	I_{GM}	± 1.5				Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	560				mJ
Avalanche Current	I_{AS}	-19				A
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	125 1.0				Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150				$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300				$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=3.5mH$, $V_{dd}=-25V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage IRF9540/IRFP9140 IRF9542/IRFP9142	-100	—	—	V	$V_{GS} = 0V$ $I_D = -250\mu A$
	IRF9541/IRFP9141 IRF9543/IRFP9143	-60	—	—	V	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}$, $I_D = -250\mu A$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS} = -20V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	$V_{GS} = 20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0V$
		—	—	1000	μA	$V_{DS} = \text{Max. Rating} \times 0.8$, $V_{GS} = 0V$, $T_C = 125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2) IRF9540/IRFP9140 IRF9543/IRFP9143	-19	—	—	A	$V_{DS} \leq -5.7V$, $V_{GS} = -10V$
	IRF9541/IRFP9141 IRF9543/IRFP9143	-15	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance (2) IRF9540/IRFP9140 IRF9542/IRFP9142	—	—	0.2	Ω	$V_{GS} = -10V$, $I_D = -10A$
	IRF9541/IRFP9141 IRF9543/IRFP9143	—	—	0.3	Ω	
g_{fs}	Forward Transconductance (2)	5.0	—	—	S	$V_{DS} \leq -50V$, $I_D = -10A$
C_{iss}	Input Capacitance	—	1560	—	pF	$V_{GS} = 0V$, $V_{DS} = -25V$, $f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	240	—	pF	
C_{rss}	Reverse Transfer Capacitance	—	120	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	20	30	ns	$V_{DD} = 0.5BV_{DSS}$, $I_D = -10A$, $Z_o = 4.7\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	10	15	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	13	20	ns	
t_f	Fall Time	—	8.0	12	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	70	90	nC	$V_{GS} = -15V$, $I_D = -24A$, $V_{DS} = 0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	—	30	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	—	60	nC	

THERMAL RESISTANCE

Symbol	Characteristic		IRF9540-3	IRFP9140-3	Unit	
R_{thJC}	Junction-to-Case	MAX	1.0	1.0	K/W	
R_{thCS}	Case-to-Sink	TYP	0.5	0.24	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	MAX	80	40	K/W	Free Air Operation

Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C

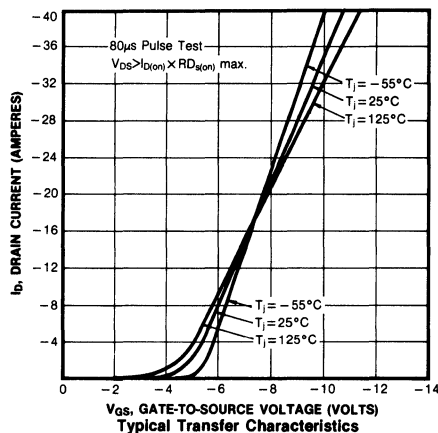
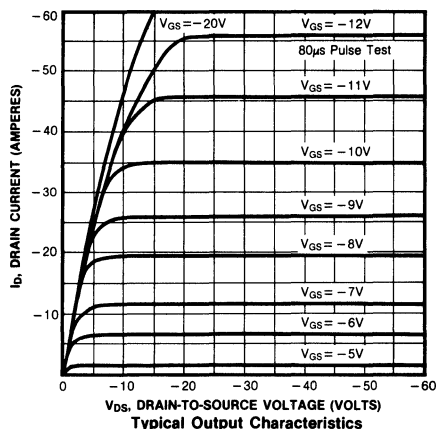
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

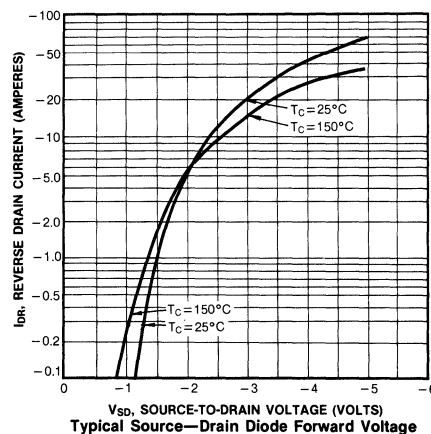
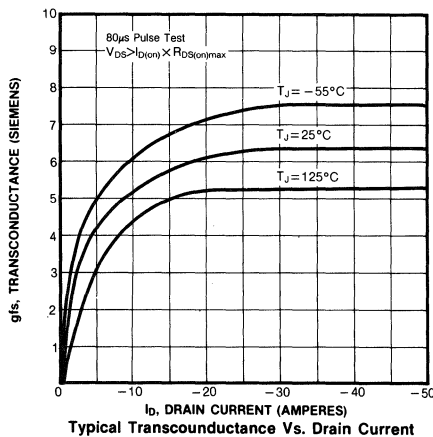
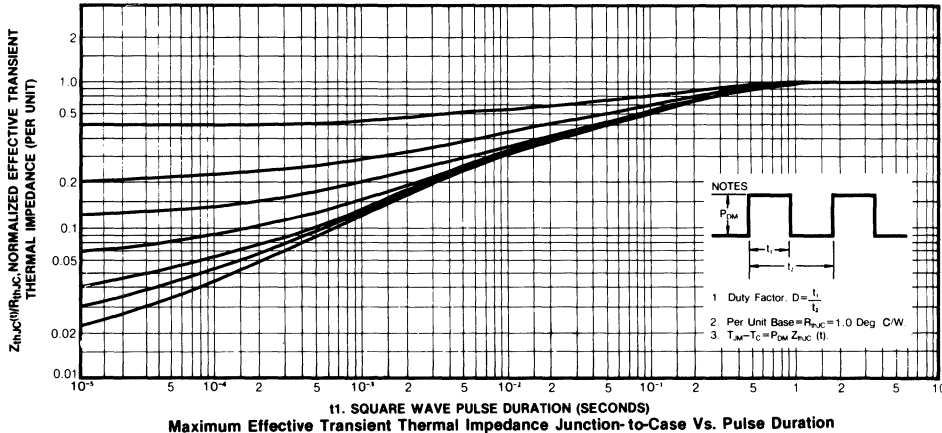
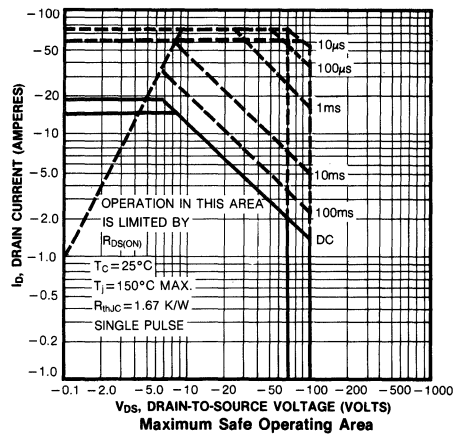
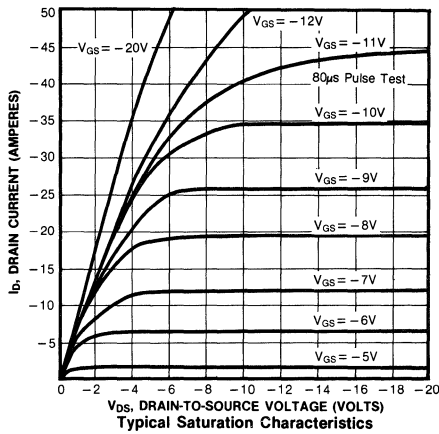
(3) Repetitive rating: Pulse width limited by max. junction temperature

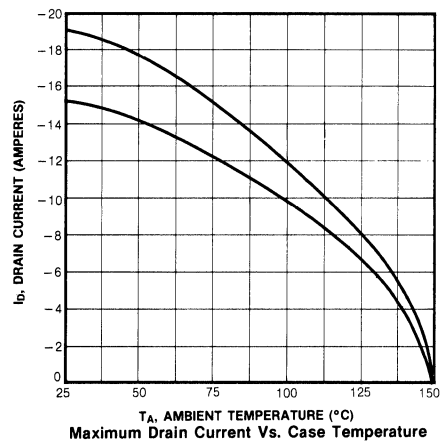
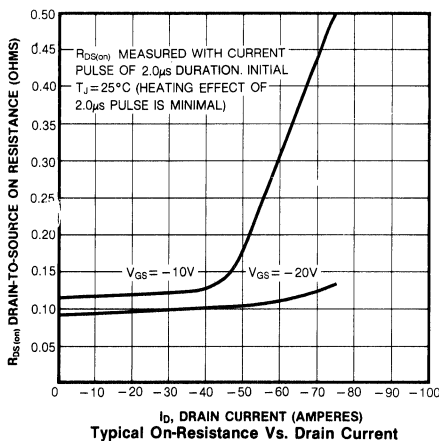
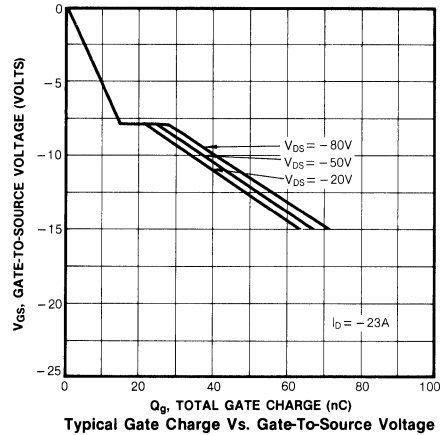
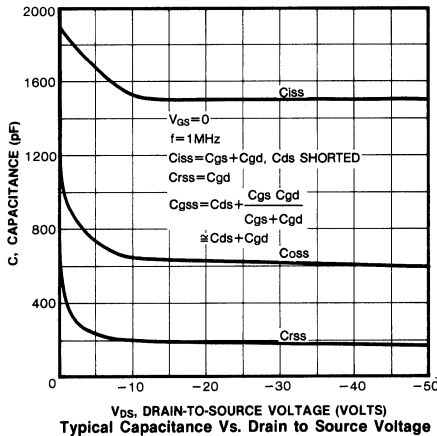
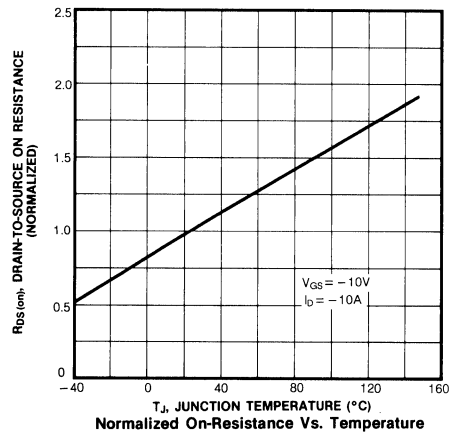
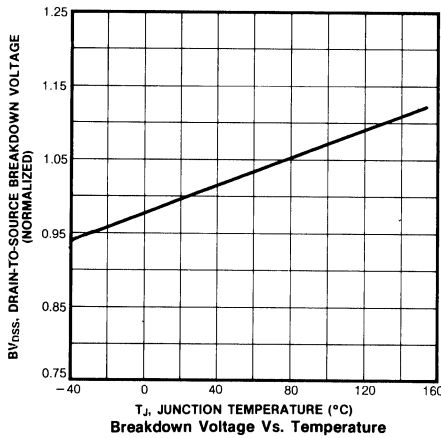
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

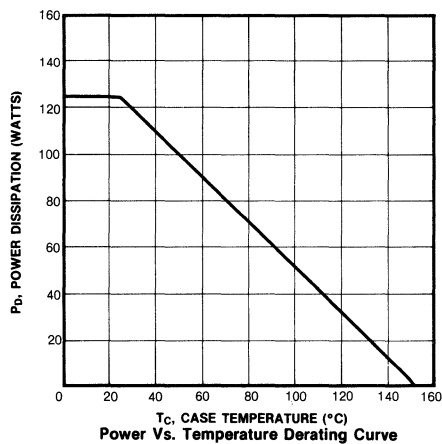
Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode) IRF9540/IRFP9140 IRF9541/IRFP9141	—	—	-19	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier
	IRF9542/IRFP9142 IRF9543/IRFP9143	—	—	-15	A	
I_{SM}	Pulse Source Current (Body Diode) (3) IRF9540/IRFP9140 IRF9541/IRFP9141	—	—	-76	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier
	IRF9542/IRFP9142 IRF9543/IRFP9143	—	—	-60	A	
V_{SD}	Diode Forward Voltage (2) IRF9540/IRFP9140 IRF9541/IRFP9141	—	—	-4.2	A	$T_C = 25^\circ\text{C}$, $I_S = -19\text{A}$, $V_{GS} = 0\text{V}$
	IRF9542/IRFP9142 IRF9543/IRFP9143	—	—	-4.0	A	$T_C = 25^\circ\text{C}$, $I_S = -15\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	170	—	ns	$T_J = 150^\circ\text{C}$, $I_F = -19\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$

Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature





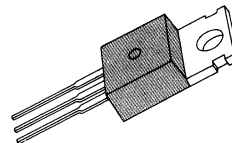




FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

TO-220



IRF9610/9611/9612/9613

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF9610	−200V	3.0Ω	−1.75A
IRF9611	−150V	3.0Ω	−1.75A
IRF9612	−200V	4.5Ω	−1.5A
IRF9613	−150V	4.5Ω	−1.5A

MAXIMUM RATINGS

Characteristic	Symbol	IRF9610	IRF9611	IRF9612	IRF9613	Unit
Drain-Source Voltage (1)	V_{DSS}	−200	−150	−200	−150	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	−200	−150	−200	−150	Vdc
Gate-Source Voltage	V_{GS}	± 20				Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	−1.75	−1.75	−1.5	−1.5	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	−1.0	−1.0	−0.9	−0.9	Adc
Drain Current—Pulsed (3)	I_{DM}	−7.0	−7.0	−6.0	−6.0	Adc
Gate Current—Pulsed	I_{GM}	± 1.5				Adc
Single Pulsed Avalanche Energy(4)	E_{AS}	110				mJ
Avalanche Current	I_{AS}	−1.75				A
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	20 0.16				Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to 150				$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300				$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=59mH$, $V_{dd}=-50V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage IRF9610/9612	-200	—	—	V	$V_{GS}=0V$ $I_D=-250\mu A$
	IRF9611/9613	-150	—	—	V	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}$, $I_D=-250\mu A$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS}=-20V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	$V_{GS}=20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS}=\text{Max. Rating}$, $V_{GS}=0V$
		—	—	1000	μA	$V_{DS}=\text{Max. Rating} \times 0.8$, $V_{GS}=0V$, $T_C=125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2) IRF9610/9611	-1.75	—	—	A	$V_{DS} \leq -7.8V$, $V_{GS}=-10V$
	IRF9612/9613	-1.5	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance (2) IRF9610/9611	—	—	3.0	Ω	$V_{GS}=-10V$, $I_D=-0.9A$
	IRF9612/9613	—	—	4.5	Ω	
g_{fs}	Forward Transconductance (2)	0.7	—	—	S	$V_{DS} \leq -50V$, $I_D=-0.9A$
C_{iss}	Input Capacitance	—	227	—	pF	$V_{GS}=0V$, $V_{DS}=-25V$, $f=1.0\text{MHz}$
C_{oss}	Output Capacitance	—	52.7	—	pF	
C_{rss}	Reverse Transfer Capacitance	—	29.6	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	—	15	ns	$V_{DD}=0.5BV_{DSS}$, $I_D=-1.5A$, $Z_O=50\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	—	25	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	—	15	ns	
t_f	Fall Time	—	—	15	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	11	—	nC	$V_{GS}=-15V$, $I_D=-4.0A$, $V_{DS}=0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	4	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	7	—	nC	

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	—	—	6.4	K/W	
R_{thCS}	Case-to-Sink	—	1.0	—	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	—	—	80	K/W	Free Air Operation

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C

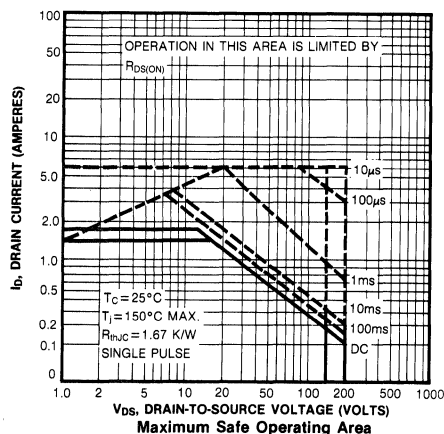
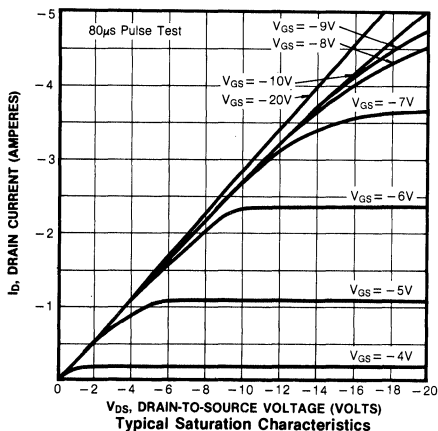
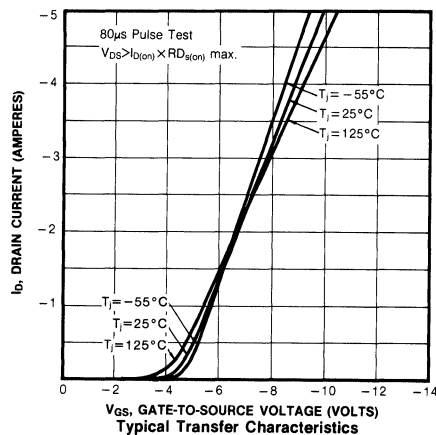
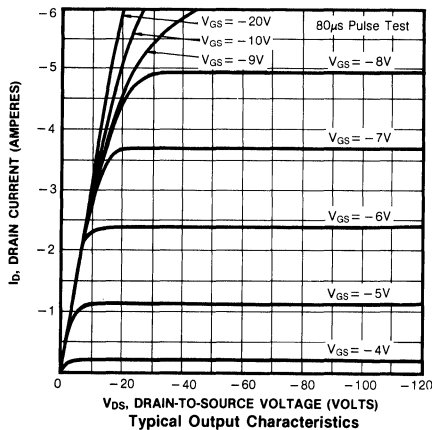
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

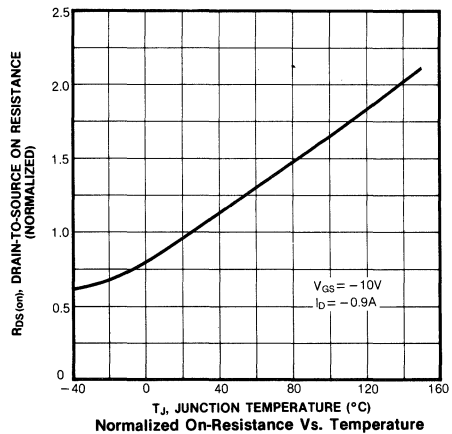
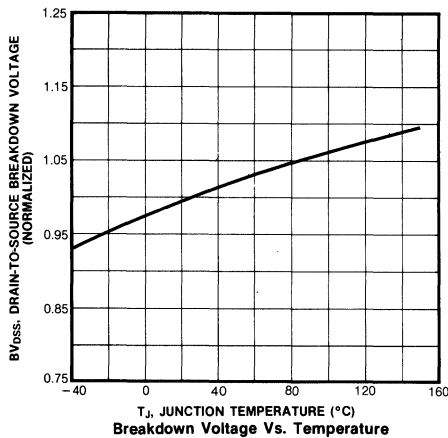
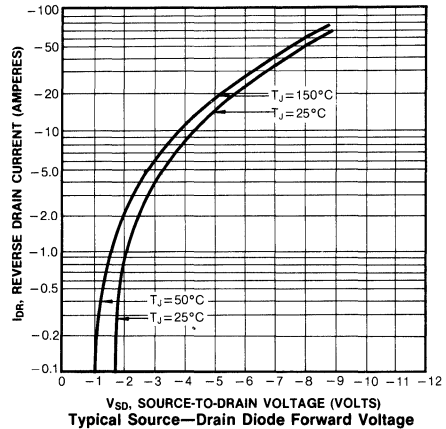
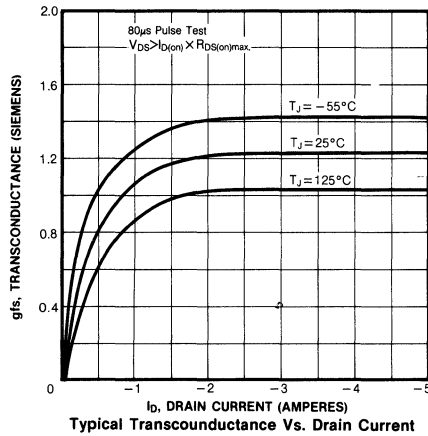
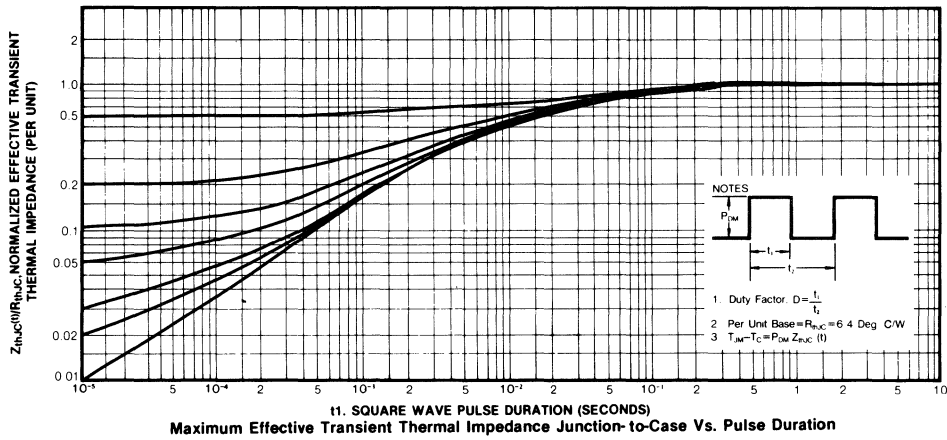
(3) Repetitive rating: Pulse width limited by max. junction temperature

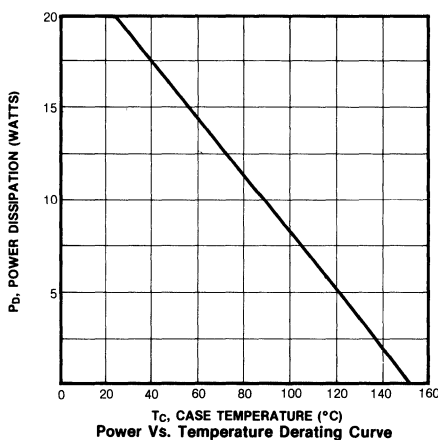
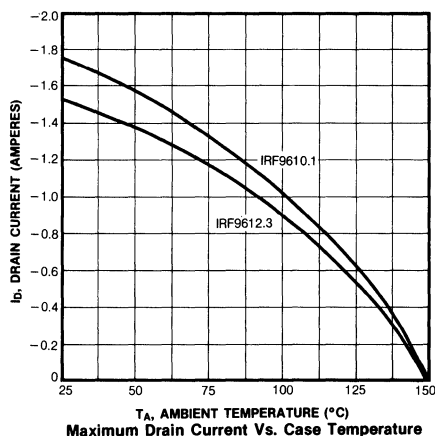
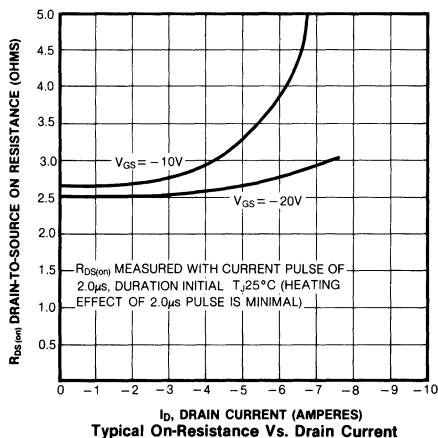
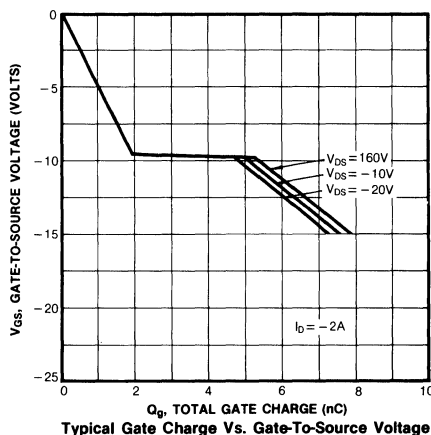
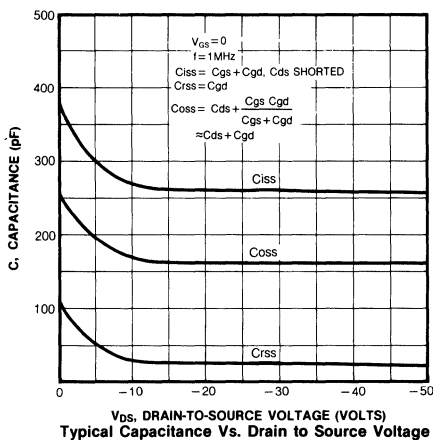
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode) IRF9610/9611	—	—	-1.75	A	Modified MOSFET showing the integral reverse P-N junction rectifier 
	IRF9612/9613	—	—	-1.5	A	
I_{SM}	Pulse Source Current (Body Diode)(3) IRF9610/9611	—	—	-7.0	A	
	IRF9612/9613	—	—	10	A	
V_{SD}	Diode Forward Voltage (2) IRF9610/9611	—	—	-5.8	V	$T_C = 25^\circ\text{C}$, $I_S = -1.75\text{A}$, $V_{GS} = 0\text{V}$
	IRF9612/9613	—	—	-5.5	V	$T_C = 25^\circ\text{C}$, $I_S = -1.5\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	240		ns	$T_J = 150^\circ\text{C}$, $I_F = -3.0\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$

Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature



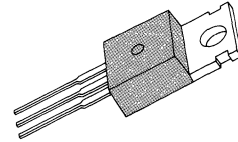




FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

TO-220



IRF9620/9621/9622/9623

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF9620	-200V	1.5Ω	-3.5A
IRF9621	-150V	1.5Ω	-3.5A
IRF9622	-200V	2.4Ω	-3.0A
IRF9623	-150V	2.4Ω	-3.0A

MAXIMUM RATINGS

Characteristic	Symbol	IRF9620	IRF9621	IRF9622	IRF9623	Unit
Drain-Source Voltage (1)	V_{DS}	-200	-150	-200	-150	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	-200	-150	-200	-150	Vdc
Gate-Source Voltage	V_{GS}	± 20				Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	-3.5	-3.5	-3.0	-3.0	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	-2.0	-2.0	-1.5	-1.5	Adc
Drain Current—Pulsed (3)	I_{DM}	-14	-14	-12	-12	Adc
Gate Current—Pulsed	I_{GM}	± 1.5				Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	270				mJ
Avalanche Current	I_{AS}	-3.5				A
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	40 0.32				Watts W/ $^\circ C$
Operating and Storage Junction to Case	T_J, T_{stg}	-55 to 150				$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300				$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=35mH$, $V_{dd}=-50V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-Source Breakdown Voltage IRF9620 IRF9622	-200	—	—	V	V _{GS} =0V I _D =-250μA
	IRF9621 IRF9623	-150	—	—	V	
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} =V _{GS} , I _D =-250μA
I _{GSS}	Gate-Source Leakage Forward	—	—	100	nA	V _{GS} =-20V
I _{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	V _{GS} =20V
I _{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	V _{DS} =Max. Rating, V _{GS} =0V
		—	—	1000	μA	V _{DS} =Max. Rating×0.8, V _{GS} =0V, T _C =125°C
I _{D(on)}	On-State Drain-Source Current (2) IRF9620 IRF9621	-3.5	—	—	A	V _{DS} ≤-8.4V, V _{GS} =-10V
	IRF9622 IRF9623	-3.0	—	—	A	
R _{DS(on)}	Static Drain-Source On-State Resistance (2) IRF9620 IRF9621	—	—	1.5	Ω	V _{GS} =-10V, I _D =-1.5A
	IRF9622 IRF9623	—	—	2.4	Ω	
g _{fs}	Forward Transconductance (2)	1.0	—	—	℧	V _{DS} ≤-50V, I _D =-1.5A
C _{iss}	Input Capacitance	—	405	—	pF	V _{GS} =0V, V _{DS} =-25V, f=1.0MHz
C _{oss}	Output Capacitance	—	85.5	—	pF	
C _{rss}	Reverse Transfer Capacitance	—	27	—	pF	
t _{d(on)}	Turn-On Delay Time	—	—	40	ns	V _{DD} =0.5BV _{DSS} , I _D =-1.5A, Z _O =50Ω (MOSFET switching times are essentially independent of operating temperature)
t _r	Rise Time	—	—	50	ns	
t _{d(off)}	Turn-Off Delay Time	—	—	50	ns	
t _f	Fall Time	—	—	40	ns	
Q _g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	—	22	nC	V _{GS} =-15V, I _D =-4.0A, V _{DS} =0.8 Max. Rating (Gate charge is essentially independent of operating temperature.)
Q _{gs}	Gate-Source Charge	—	—	9	nC	
Q _{gd}	Gate-Drain ("Miller") Charge	—	—	13	nC	

THERMAL RESISTANCE

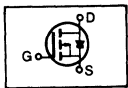
Symbol	Characteristic		IRF9620-3	Unit	
R _{thJC}	Junction-to-Case	MAX	3.12	K/W	
R _{thCS}	Case-to-Sink	TYP	1.0	K/W	Mounting surface flat, smooth, and greased
R _{thJA}	Junction-to-Ambient	MAX	80	K/W	Free Air Operation

Notes: (1) T_J=25°C to 150°C

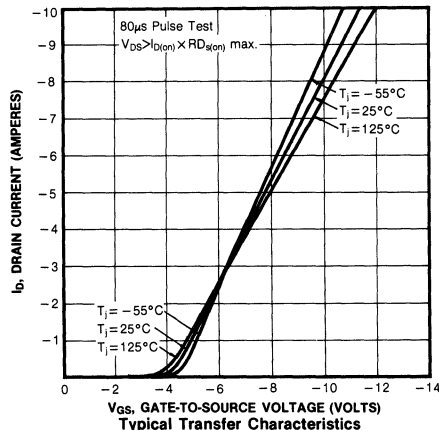
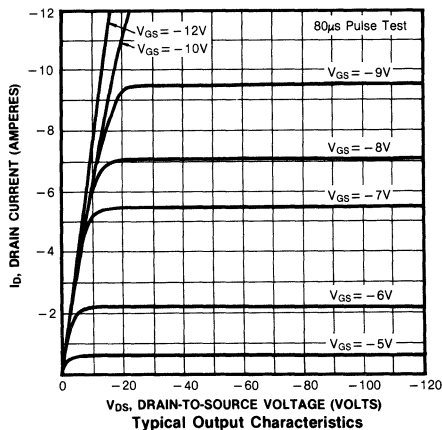
(2) Pulse test: Pulse width≤300μs, Duty Cycle≤2%

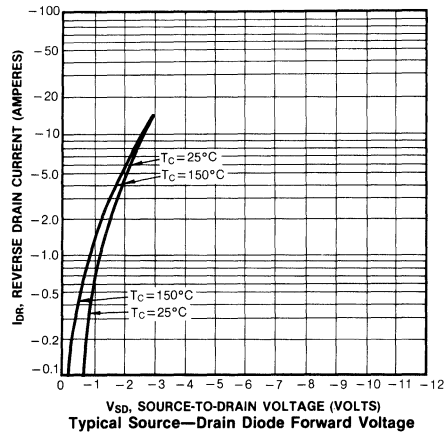
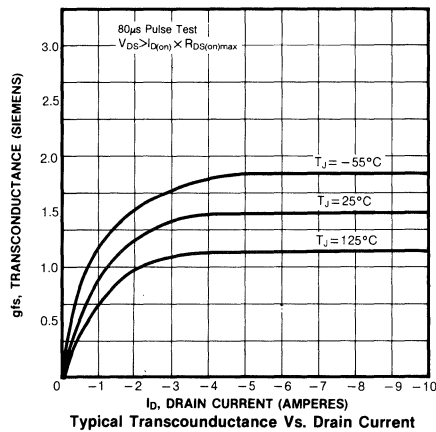
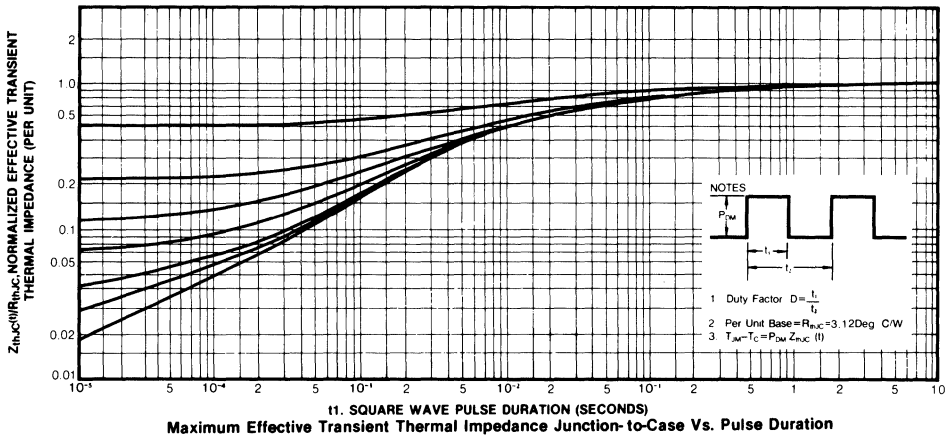
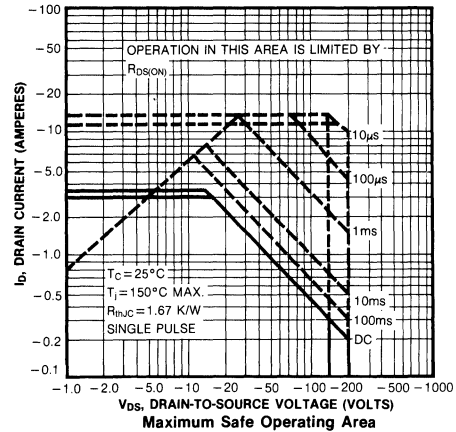
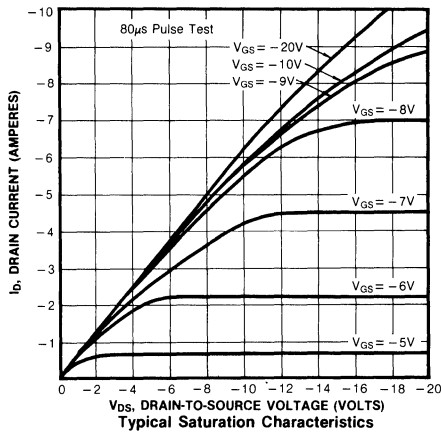
(3) Repetitive rating: Pulse width limited by max. junction temperature

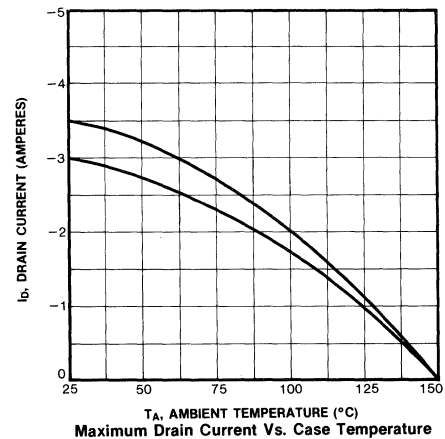
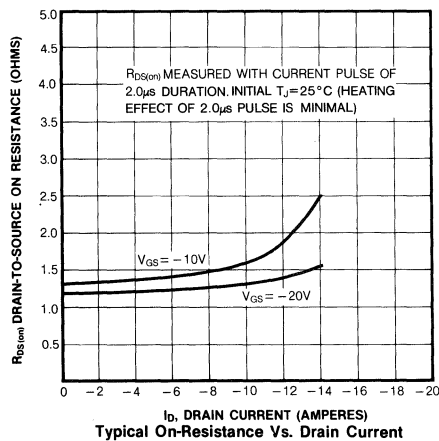
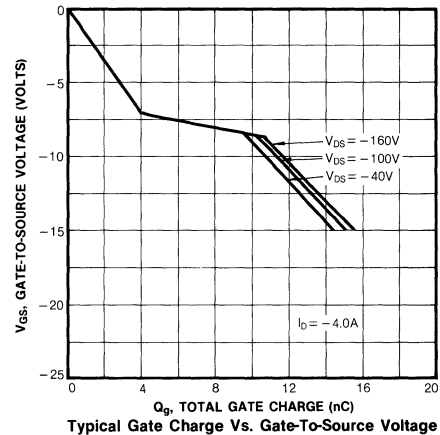
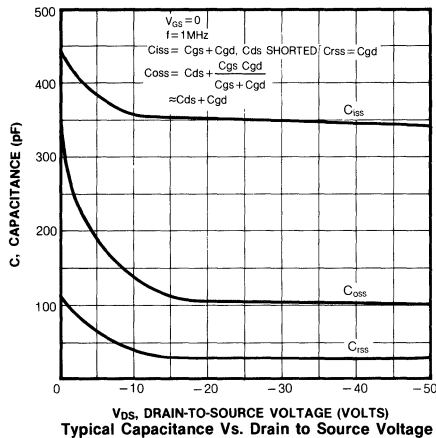
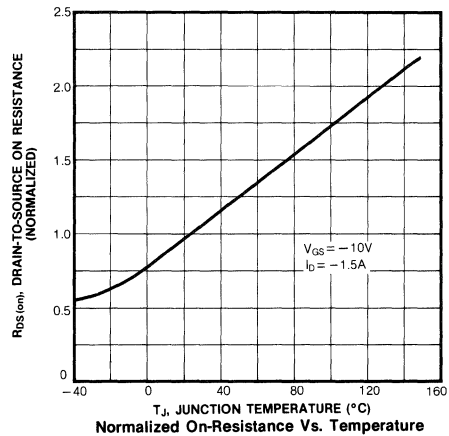
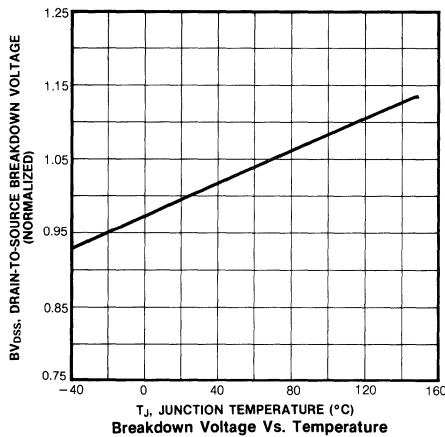
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

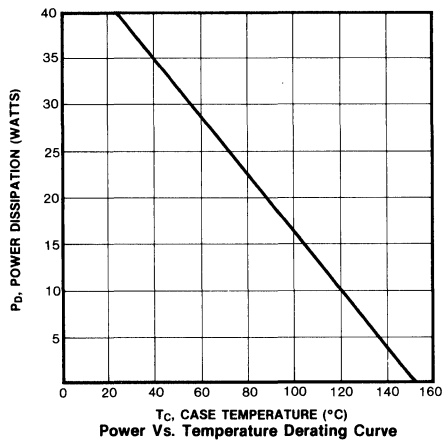
Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode) IRF9620 IRF9621	—	—	-3.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier 
	IRF9622 IRF9623	—	—	-3.0	A	
I_{SM}	Pulse Source Current(Body Diode)(3) IRF9620 IRF9621	—	—	-14	A	
	IRF9622 IRF9623	—	—	-12	A	
V_{SD}	Diode Forward Voltage (2) IRF9620 IRF9621	—	—	-7.0	V	$T_C=25^\circ\text{C}$, $I_S=-3.5\text{A}$, $V_{GS}=0\text{V}$
	IRF9622 IRF9623	—	—	-6.0	V	$T_C=25^\circ\text{C}$, $I_S=-3.0\text{A}$, $V_{GS}=0\text{V}$
t_{rr}	Reverse Recovery Time	—	300	—	ns	$T_J=150^\circ\text{C}$, $I_F=-3.5\text{A}$, $dI_F/dt=100\text{A}/\mu\text{S}$

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
 (3) Repetitive rating: Pulse with limited by max. junction temperature









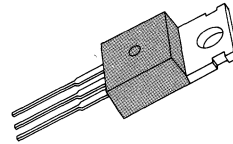
FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

PRODUCT SUMMARY

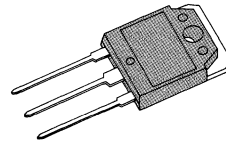
Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF9630/IRFP9230	-200V	0.8Ω	-6.5A
IRF9631/IRFP9231	-150V	0.8Ω	-6.5A
IRF9632/IRFP9232	-200V	1.2Ω	-5.5A
IRF9633/IRFP9233	-150V	1.2Ω	-5.5A

TO-220



IRF9630/9631/9632/9633

TO-3P



IRFP9230/9231/9232/9233

MAXIMUM RATINGS

Characteristic	Symbol	IRF9630 IRFP9230	IRF9631 IRFP9231	IRF9632 IRFP9232	IRF9633 IRFP9233	Unit
Drain-Source Voltage (1)	V_{DS}	-200	-150	-200	-150	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	-200	-150	-200	-150	Vdc
Gate-Source Voltage	V_{GS}	± 20				Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	-0.5	-6.5	-5.5	-5.5	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	-4.0	-4.0	-3.5	-3.5	Adc
Drain Current—Pulsed (3)	I_{DM}	-26	-26	-22	-22	Adc
Gate Current—Pulsed	I_{GM}	± 1.5				Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	260				mJ
Avalanche Current	I_{AS}	-6.5				A
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	75 0.6				Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150				$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300				$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=14mH$, $V_{dd}=-50V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

IRF9630/9631/9632/9633 IRFP9230/9231/9232/9233

P-CHANNEL POWER MOSFETS

ELECTRICAL CHARACTERISTICS (T_C=25 °C unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-Source Breakdown Voltage IRF9630/IRFP9230 IRF9632/IRFP9232	-200	—	—	V	V _{GS} =0V I _D =-250μA
	IRF9631/IRFP9231 IRF9633/IRFP9233	-150	—	—	V	
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} =V _{GS} , I _D =-250μA
I _{GSS}	Gate-Source Leakage Forward	—	—	100	nA	V _{GS} =-20V
I _{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	V _{GS} =20V
I _{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	V _{DS} =Max. Rating, V _{GS} =0V
		—	—	1000	μA	V _{DS} =Max. Rating×0.8, V _{GS} =0V, T _C =125 °C
I _{D(on)}	On-State Drain-Source Current (2) IRF9630/IRFP9230 IRF9631/IRFP9231	-6.5	—	—	A	V _{DS} ≤-7.8V, V _{GS} =-10V
	IRF9632/IRFP9232 IRF9633/IRFP9233	-5.5	—	—	A	
R _{DS(on)}	Static Drain-Source On-State Resistance (2) IRF9630/IRFP9230 IRF9631/IRFP9231	—	—	0.8	Ω	V _{GS} =-10V, I _D =-3.5A
	IRF9632/IRFP9232 IRF9633/IRFP9233	—	—	1.2	Ω	
g _{fs}	Forward Transconductance (2)	2.2	—	—	U	V _{DS} ≤-50V, I _D =-3.5A
C _{iss}	Input Capacitance	—	812	—	pF	V _{GS} =0V, V _{DS} =-25V, f=1.0MHz
C _{oss}	Output Capacitance	—	318	—	pF	
C _{rss}	Reverse Transfer Capacitance	—	72.6	—	pF	
t _{d(on)}	Turn-On Delay Time	—	—	50	ns	V _{DD} =0.5BV _{DSS} , I _D =-3.5A, Z _O =50Ω (MOSFET switching times are essentially independent of operating temperature)
t _r	Rise Time	—	—	100	ns	
t _{d(off)}	Turn-Off Delay Time	—	—	100	ns	
t _f	Fall Time	—	—	80	ns	
Q _g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	—	45	nC	V _{GS} =-15V, I _D =-8.0A, V _{DS} =0.8 Max. Rating (Gate charge is essentially independent of operating temperature.)
Q _{gs}	Gate-Source Charge	—	—	20	nC	
Q _{gd}	Gate-Drain ("Miller") Charge	—	—	25	nC	

THERMAL RESISTANCE

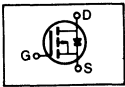
Symbol	Characteristic		IRF9630-3	IRFP9230-3	Unit	
R _{thJC}	Junction-to-Case	MAX	1.67	1.67	K/W	
R _{thCS}	Case-to-Sink	TYP	1.0	0.24	K/W	Mounting surface flat, smooth, and greased
R _{thJA}	Junction-to-Ambient	MAX	80	40	K/W	Free Air Operation

Notes: (1) T_J=25 °C to 150 °C

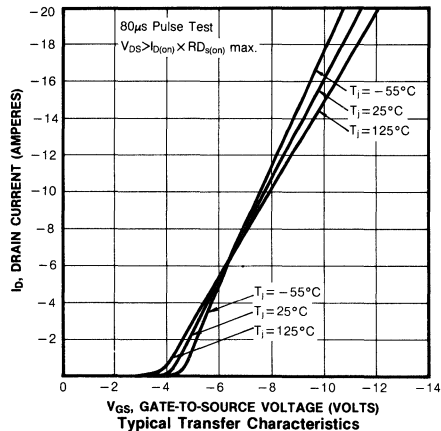
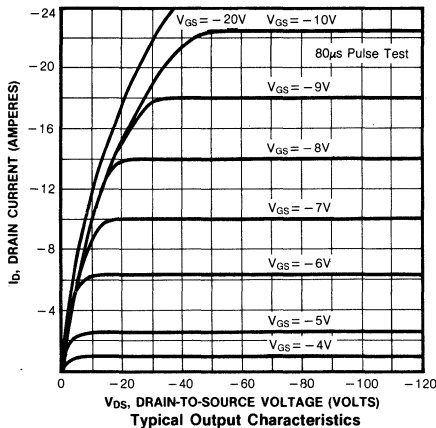
(2) Pulse test: Pulse width≤300μs, Duty Cycle≤2%

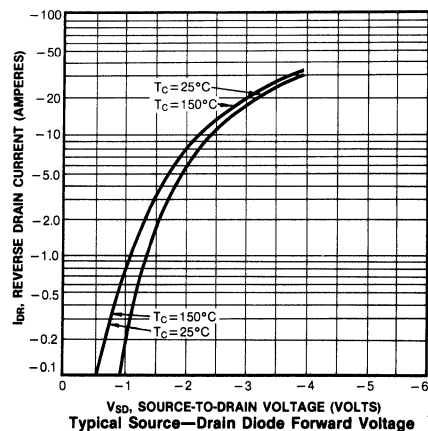
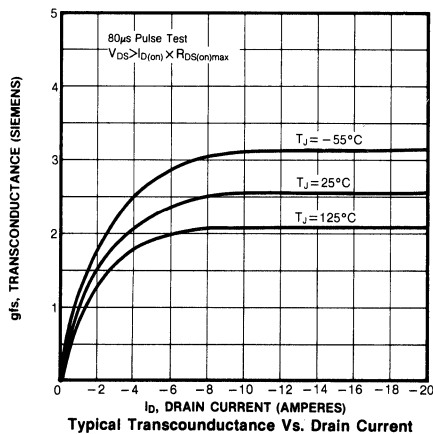
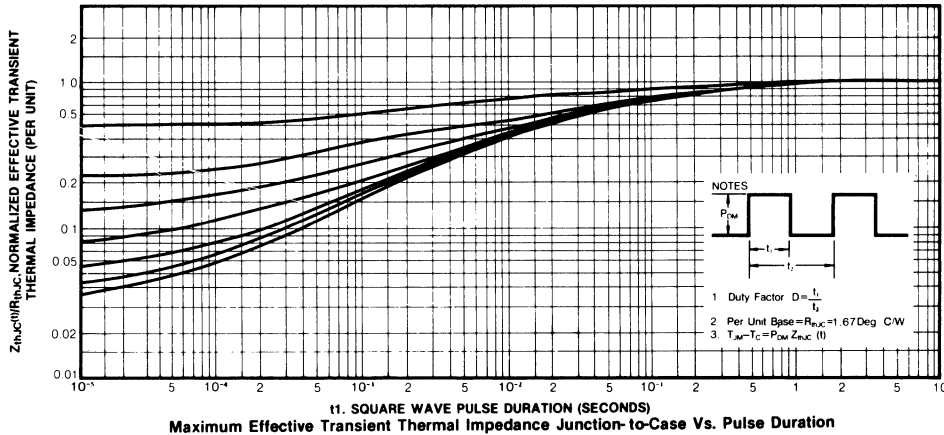
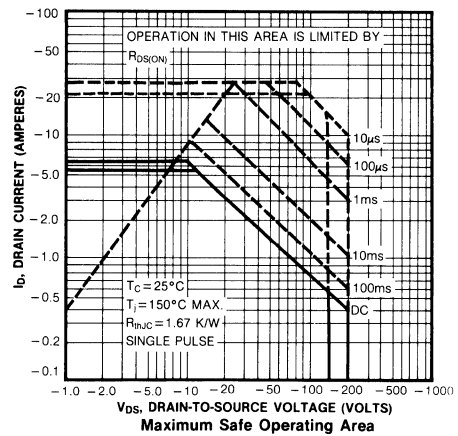
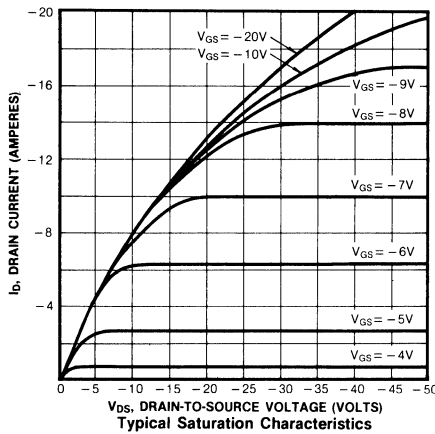
(3) Repetitive rating: Pulse width limited by max. junction temperature

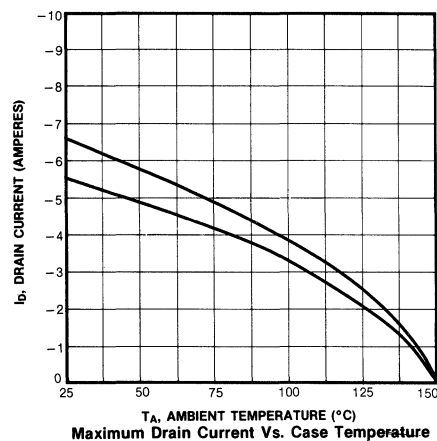
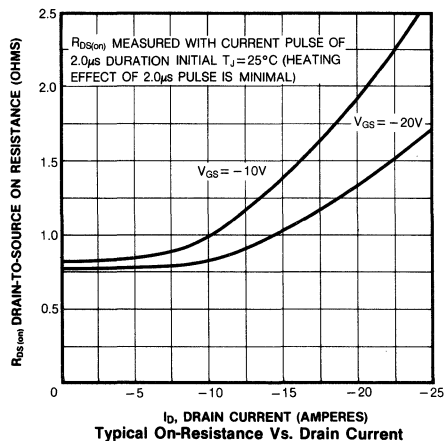
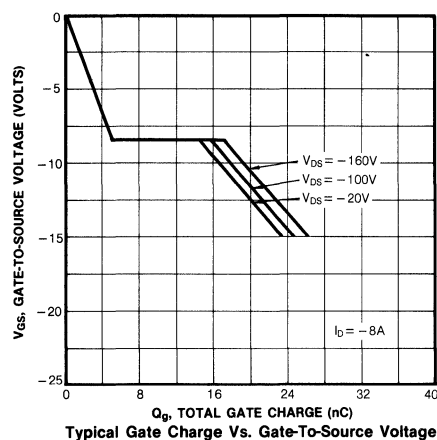
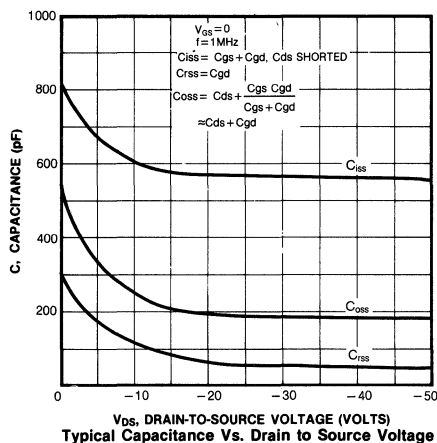
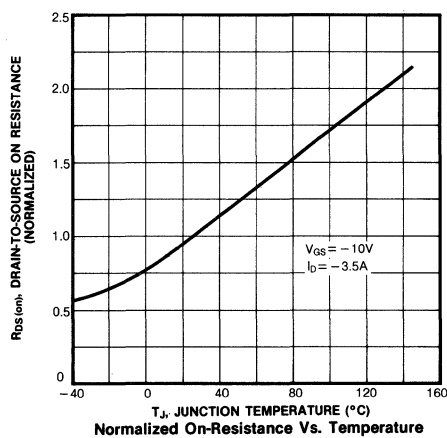
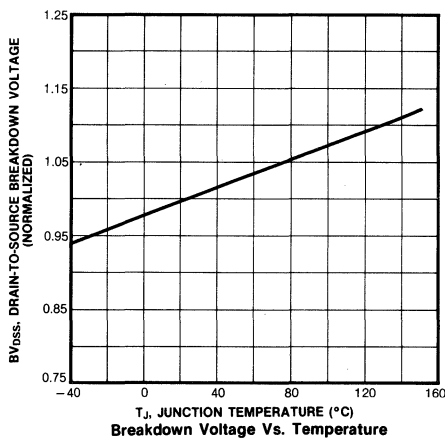
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

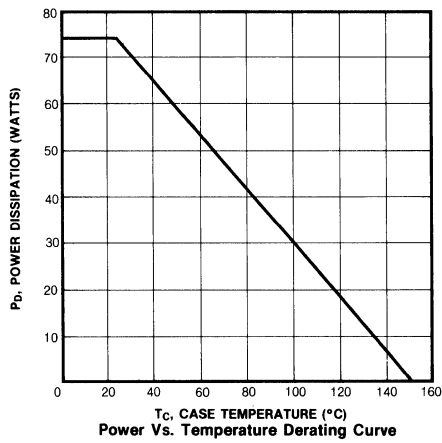
Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode) IRF9630/IRFP9230 IRF9631/IRFP9231	—	—	-6.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier 
	IRF9632/IRFP9232 IRF9633/IRFP9233	—	—	-5.5	A	
I_{SM}	Pulse Source Current (Body Diode) (3) IRF9630/IRFP9230 IRF9631/IRFP9231	—	—	-26	A	
	IRF9632/IRFP9232 IRF9633/IRFP9233	—	—	-22	A	
V_{SD}	Diode Forward Voltage (2) IRF9630/IRFP9230 IRF9631/IRFP9231	—	—	-6.5	A	$T_C = 25^\circ\text{C}$, $I_S = -6.5\text{A}$, $V_{GS} = 0\text{V}$
	IRF9632/IRFP9232 IRF9633/IRFP9233	—	—	-6.3	A	$T_C = 25^\circ\text{C}$, $I_S = -5.5\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	300	—	ns	$T_J = 150^\circ\text{C}$, $I_F = -6.5\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$

Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature









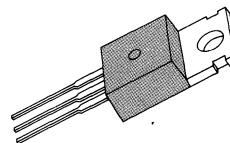
FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

PRODUCT SUMMARY

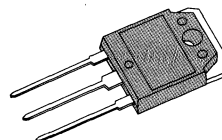
Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF9640/IRFP9240	-200V	0.5Ω	-11A
IRF9641/IRFP9241	-150V	0.5Ω	-11A
IRF9642/IRFP9242	-200V	0.7Ω	-9.0A
IRF9643/IRFP9243	-150V	0.7Ω	-9.0A

TO-220



IRF9640/9641/9642/9643

TO-3P



IRFP9240/9241/9242/9243

MAXIMUM RATINGS

Characteristic	Symbol	IRF9640 IRFP9240	IRF9641 IRFP9241	IRF9642 IRFP9242	IRF9643 IRFP9243	Unit
Drain-Source Voltage (1)	V_{DSS}	-200	-150	-200	-150	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	-200	-150	-200	-150	Vdc
Gate-Source Voltage	V_{GS}	± 20				Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	-11	-11	-9.0	-9.0	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	-7.0	-7.0	-6.0	-6.0	Adc
Drain Current—Pulsed (3)	I_{DM}	-44	-44	-36	-37	Adc
Gate Current—Pulsed	I_{GM}	± 1.5				Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	380				mJ
Avalanche Current	I_{AS}	-11				A
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	125 1.0				Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150				$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300				$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=7mH$, $V_{dd}=-50V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage IRF9640/IRFP9240 IRF9642/IRFP9242	-200	—	—	V	$V_{GS}=0V$ $I_D = -250\mu A$
	IRF9641/IRFP9241 IRF9643/IRFP9243	-150	—	—	V	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}$, $I_D = -250\mu A$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS} = -20V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	$V_{GS} = 20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0V$
		—	—	1000	μA	$V_{DS} = \text{Max. Rating} \times 0.8$, $V_{GS} = 0V$, $T_C = 125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2) IRF9640/IRFP9240 IRF9641/IRFP9241	-11	—	—	A	$V_{DS} \leq -7.7V$, $V_{GS} = -10V$
	IRF9642/IRFP9242 IRF9643/IRFP9243	-9.0	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance (2) IRF9640/IRFP9240 IRF9642/IRFP9241	—	0.44	0.5	Ω	$V_{GS} = -10V$, $I_D = -6.0A$
	IRF9642/IRFP9242 IRF9643/IRFP9243	—	0.5	0.7	Ω	
g_{fs}	Forward Transconductance (2)	4.0	4.7	—	Ω	$V_{DS} \leq -50V$, $I_D = -6.0A$
C_{iss}	Input Capacitance	—	1542	—	pF	$V_{GS} = 0V$, $V_{DS} = -25V$, $f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	230	—	pF	
C_{rss}	Reverse Transfer Capacitance	—	115	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	—	30	ns	$V_{DD} = 0.5BV_{DSS}$, $I_D = -6.0A$, $Z_O = 4.7\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	—	15	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	—	18	ns	
t_f	Fall Time	—	—	12	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	—	90	nC	$V_{GS} = -15V$, $I_D = -22A$, $V_{DS} = 0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	—	30	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	—	60	nC	

THERMAL RESISTANCE

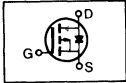
Symbol	Characteristic		IRF9640-3	IRFP9240-3	Unit	
R_{thJC}	Junction-to-Case	MAX	1.0	1.0	K/W	
R_{thCS}	Case-to-Sink	TYP	0.5	0.24	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	MAX	80	40	K/W	Free Air Operation

Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C

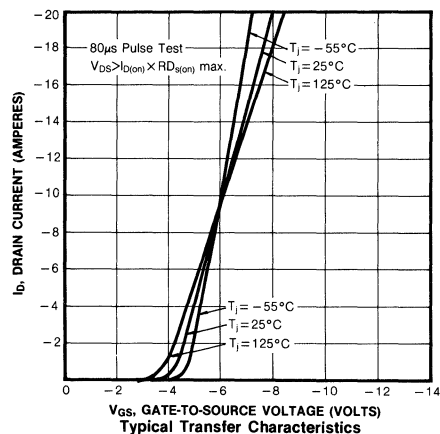
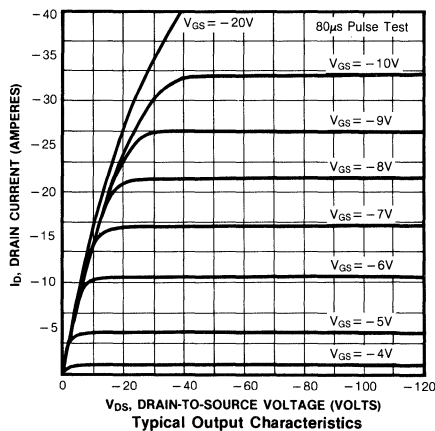
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

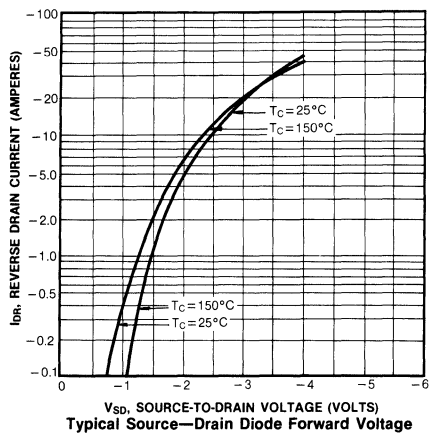
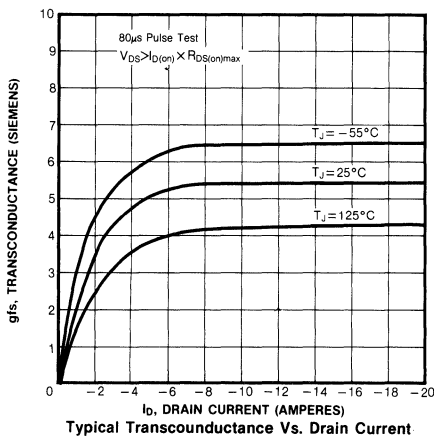
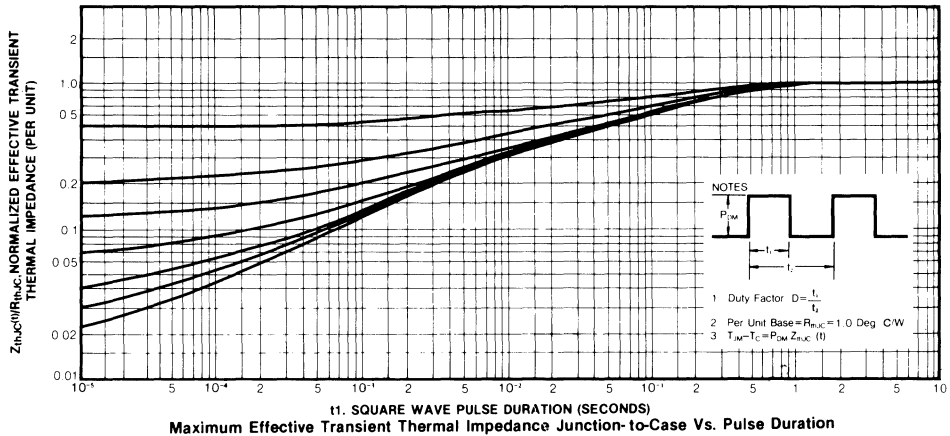
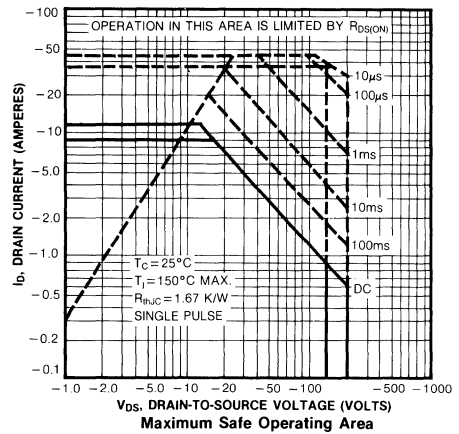
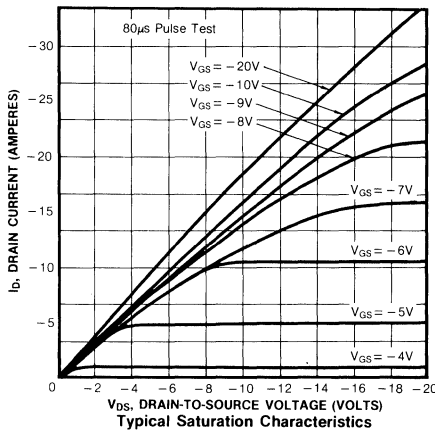
(3) Repetitive rating: Pulse width limited by max. junction temperature

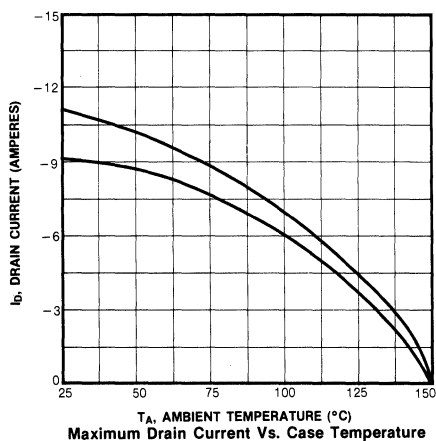
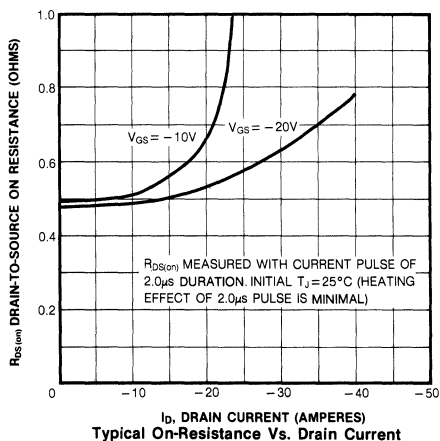
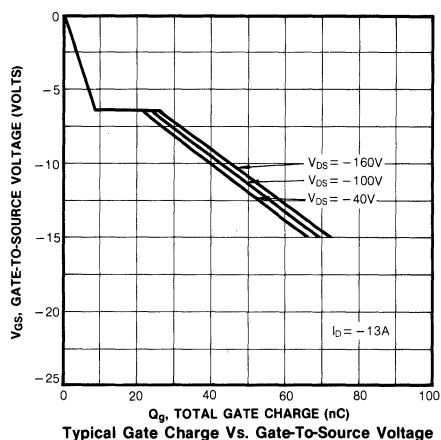
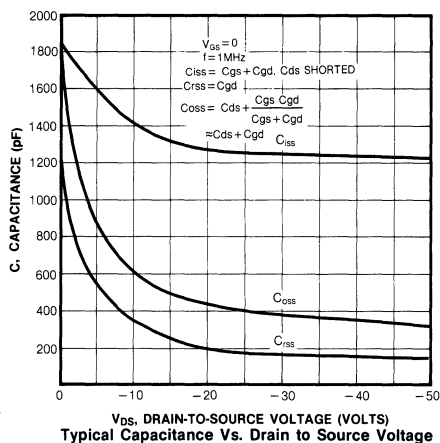
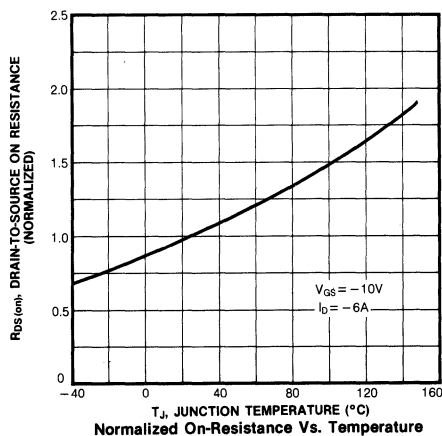
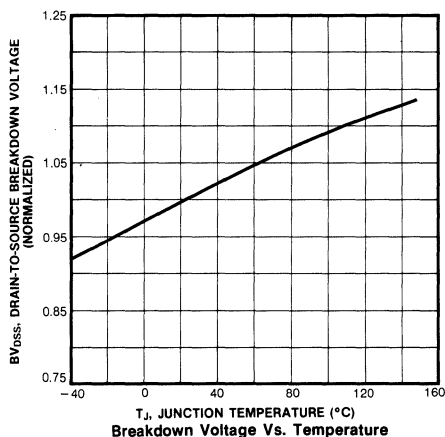
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

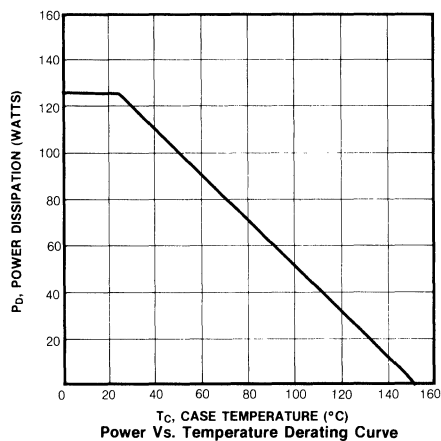
Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode) IRF9640/IRFP9240 IRF9641/IRFP9241	—	—	-11	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier 
	IRF9642/IRFP9242 IRF9643/IRFP9243	—	—	-9	A	
I_{SM}	Pulse Source Current (Body Diode) (3) IRF9640/IRFP9240 IRF9641/IRFP9241	—	—	-44	A	
	IRF9642/IRFP9242 IRF9643/IRFP9243	—	—	-36	A	
V_{SD}	Diode Forward Voltage (2) IRF9640/IRFP9240 IRF9641/IRFP9241	—	—	-4.6	A	$T_C=25^\circ\text{C}$, $I_S=-11\text{A}$, $V_{GS}=0\text{V}$
	IRF9642/IRFP9242 IRF9643/IRFP9243	—	—	-4.4	A	$T_C=25^\circ\text{C}$, $I_S=-9.0\text{A}$, $V_{GS}=0\text{V}$
t_{rr}	Reverse Recovery Time	—	270	—	ns	$T_J=150^\circ\text{C}$, $I_F=-11\text{A}$, $dI_F/dt=100\text{A}/\mu\text{S}$

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature





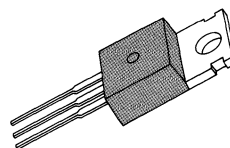




FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

TO-220



IRF9Z14/Z15
IRF9Z10/Z12

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF9Z10	-50V	0.50 Ω	-4.7A
IRF9Z14	-60V	0.50 Ω	-4.7A
IRF9Z12	-50V	0.70 Ω	-4.0A
IRF9Z15	-60V	0.70 Ω	-4.0A

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	IRF9Z10	IRF9Z12	IRF9Z14	IRF9Z15	Unit
Drain-Source Voltage (1)	V _{DSS}	−50		−60V		V _{dc}
Drain-Gate Voltage (R _{GS} =1.0MΩ)(1)	V _{DGR}	−50		−60V		V _{dc}
Gate-Source Voltage	V _{GS}	±20				V _{dc}
Continuous Drain Current T _C =25°C	I _D	−4.7	−4.0	−4.7	−4.0	A _{dc}
Continuous Drain Current T _C =100°C	I _D	−3.0	−2.5	−3.0	−2.5	A _{dc}
Drain Current—Pulsed (3)	I _{DM}	−19	−16	−19	−16	A _{dc}
Gate Current—Pulsed	I _{GM}	±1.5				A _{dc}
Single Avalanche Energy (4)	E _{AS}	1.0				mj
Avalanche Current	I _{AS}	−4.7				A
Total Power Dissipation at T _C =25°C Derate above 25°C	P _D	20 0.16				Watts W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	−55 to 150				°C
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T _L	300				°C

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=100\mu H$, $V_{dd}=-25V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-Source IRF9Z14/Z15	-60	—	—	V	V _{GS} =0V, I _D =-250μA
	Breakdown Voltage IRF9Z10/Z12	-50	—	—	V	
V _{GS(th)}	Gate Threshold Voltage	-2.0	—	-4.0	V	V _{DS} =V _{GS} , I _D =-250μA
I _{GSS}	Gate-Source Leakage Forward	—	—	-100	nA	V _{GS} =-20V
I _{GSS}	Gate-Source Leakage Reverse	—	—	+100	nA	V _{GS} =+20V
I _{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	V _{DS} =Max. Rating, V _{GS} =0V
		—	—	1000		V _{DS} =0.8Max, Rating, V _{GS} =20V, T _J =125°C
I _{D(on)}	On-State Drain- IRF9Z10/Z14	-4.7	—	—	A	V _{DS} ≤-3.29V V _{GS} =-10V
	Source Current (2) IRF9Z12/Z15	-4.0	—	—		
R _{DS(on)}	Static Drain-Source IRF9Z10/Z14	—	—	0.50	Ω	V _{GS} =-10V, I _D =-2.5A
	On-State Resistance IRF9Z12/Z15	—	—	0.70		
g _{fs}	Forward Transconductance (2)	1.7	—	—	U	V _{DS} =2×V _{GS} , I _D =-2.4A
C _{iss}	Input Capacitance	—	308	—	pF	V _{GS} =0V
C _{oss}	Output Capacitance	—	123	—	pF	V _{DS} =-25V f=1.0MHz
C _{rss}	Reverse Transfer Capacitance	—	55	—	pF	
t _{d(on)}	Turn-On Delay Time	—	—	9.2	ns	V _{DD} =-25 V, I _D =-4.7A Z _O =24 Ω (MOSFET switching times are essentially independent of operating temperature)
t _r	Rise Time	—	—	71	ns	
t _{d(off)}	Turn-Off Delay Time	—	—	20	ns	
t _f	Fall Time	—	—	59	ns	
Q _g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	—	11	nC	V _{GS} =-10V, I _D =-4.7A, V _{DS} =0.8, Max. Rating (Gate charge is essentially independent of operating temperature.)
Q _{gs}	Gate-Source Charge	—	—	3.8	nC	
Q _{gd}	Gate-Drain ("Miller") Charge	—	—	4.1	nC	

THERMAL RESISTANCE

R _{thJC}	Junction-to-Case	MAX	6.4	K/W	
R _{thCS}	Case-to-Sink	TYP	1.0	K/W	Mounting surface flat Smooth, and greased
R _{thJA}	Junction-to-Ambient	MAX	80	K/W	Free Air Operation

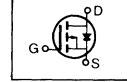
Notes: (1) T_J=25°C to 150°C

(2) Pulse test: Pulse width≤300μs, Duty Cycle≤2%

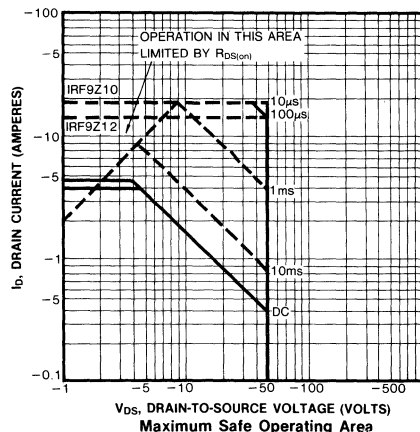
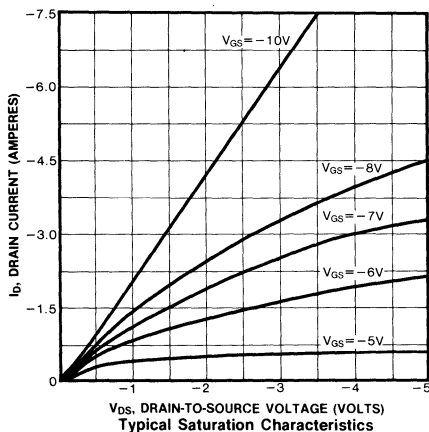
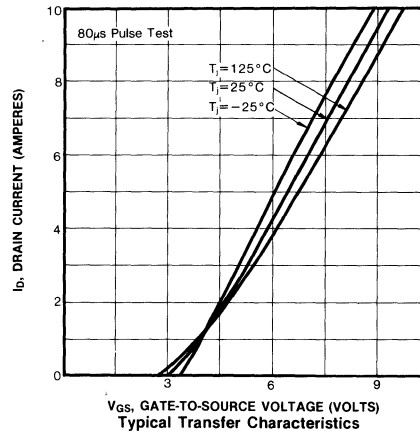
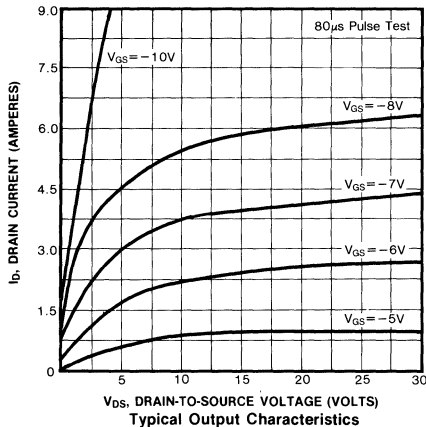
(3) Repetitive rating: Pulse width limited by max. junction temperature

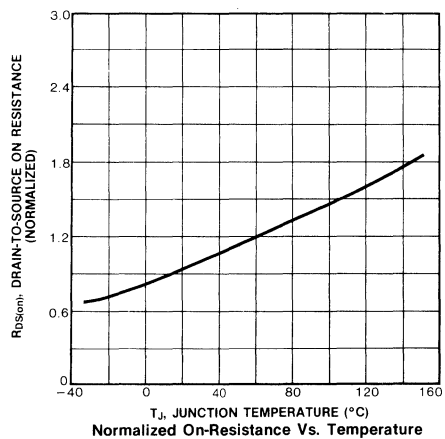
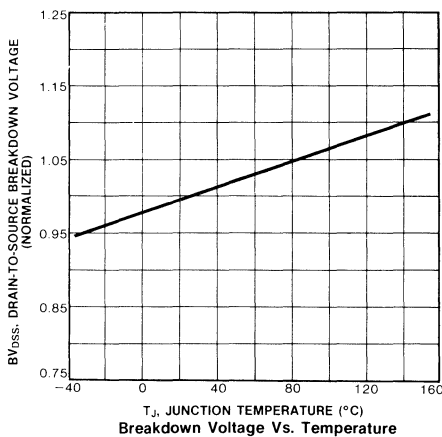
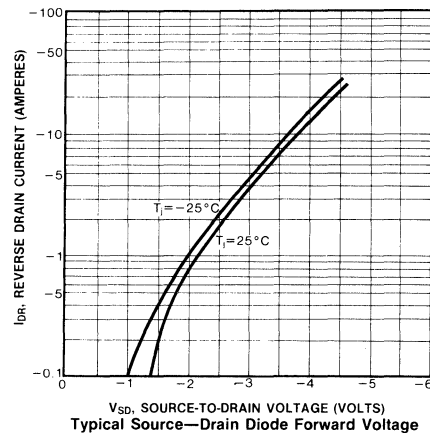
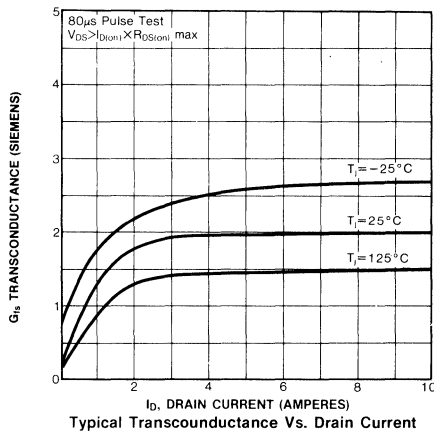
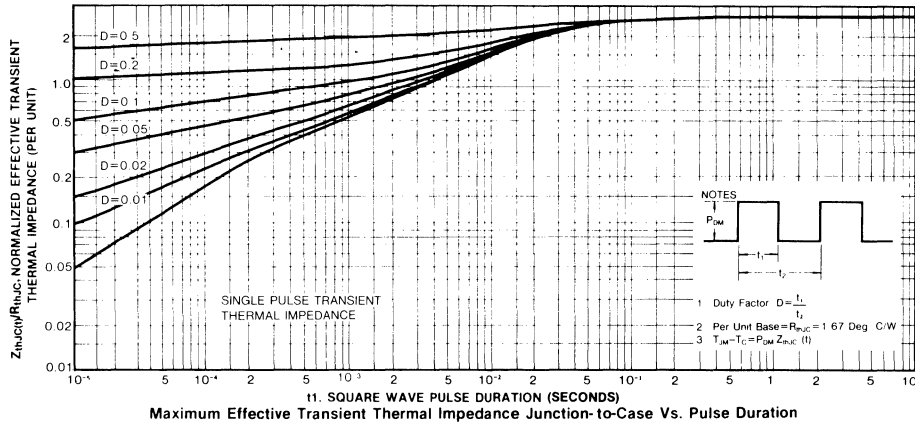
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

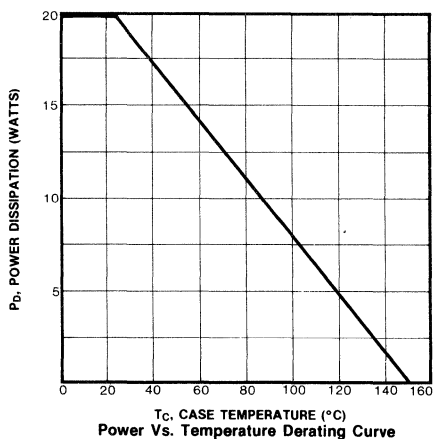
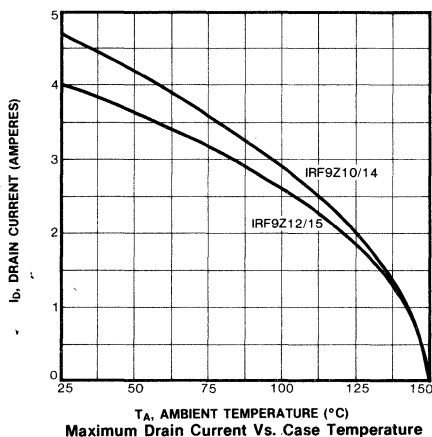
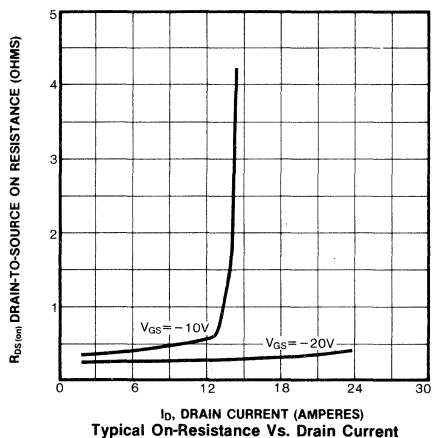
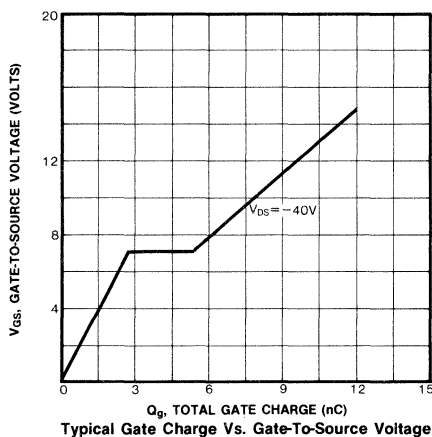
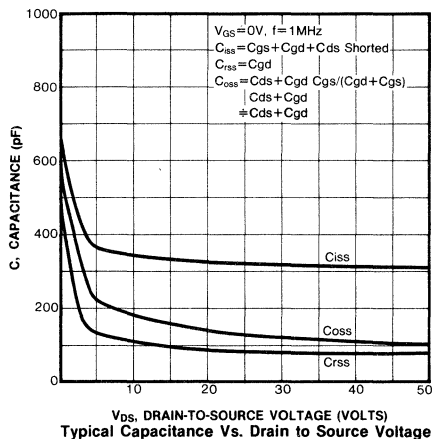
Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-4.7	A	Modified MOSFET integral reverse P-N junction rectifier
	IRF9Z14/10	—	—	-4.0		
I_{SM}	Pulse Source Current (3)	—	—	-19	A	
	IRF9Z15/12	—	—	-16		
V_{SD}	Diode Forward Voltage	—	—	-5.5	V	$T_J = 25^\circ\text{C}$, $I_S = -4.7\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	—	160	ns	$T_J = 25^\circ\text{C}$, $I_F = -4.7\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$



- Notes:** (1) $T_J = 25^\circ\text{C}$ to 150°C
(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature



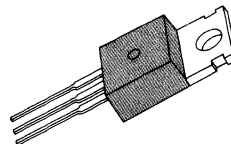




FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

TO-220



IRF9Z24/Z25
IRF9Z20/Z22

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF9Z20	-50V	0.28Ω	-9.7A
IRF9Z24	-60V	0.28Ω	-9.7A
IRF9Z22	-50V	0.33Ω	-8.9A
IRF9Z25	-60V	0.33Ω	-8.9A

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	IRF9Z20	IRF9Z22	IRF9Z24	IRF9Z25	Unit
Drain-Source Voltage (1)	V_{DSS}	-50		-60V		Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	-50		-60V		Vdc
Gate-Source Voltage	V_{GS}	± 20				Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	-9.7	-8.9	-9.7	-8.9	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	-6.1	-5.6	-6.1	-5.6	Adc
Drain Current—Pulsed (3)	I_{DM}	-39	-36	-39	-36	Adc
Gate Current—Pulsed	I_{GM}	± 1.5				Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	4.2				mJ
Avalanche Current	I_{AS}	-9.7				A
Total Power Dissipation at $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	40 0.32				Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150				$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300				$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=100\mu H$, $V_{dd}=-25V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV_{DS}	Drain-Source IRF9Z24/Z25	-60	—	—	V	$V_{GS}=0V$, $I_D=-250\mu A$
	Breakdown Voltage IRF9Z20/Z22	-50	—	—	V	
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	$V_{DS}=V_{GS}$, $I_D=-250\mu A$
I_{GSS}	Gate-Source Leakage Forward	—	—	-100	nA	$V_{GS}=-20V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	100	nA	$V_{GS}=20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS}=\text{Max. Rating}$, $V_{GS}=0V$
		—	—	1000		$V_{DS}=0.8\text{Max. Rating}$, $T_C=125^\circ\text{C}$, $V_{GS}=0V$
$I_{D(on)}$	On-State Drain- IRF9Z20/Z24	-9.7	—	—	A	$V_{DS}\leq -3.2V$ $V_{GS}=-10V$
	Source Current (2) IRF9Z22/Z25	-8.9	—	—		
$R_{DS(on)}$	Static Drain-Source IRF9Z20/Z24	—	0.18	0.28	Ω	$V_{GS}=-10V$, $I_D=-5.6A$
	On-State Resistance IRF9Z22/Z25	—	—	0.33		
g_{fs}	Forward Transconductance (2)	2.3	4.1	—	U	$V_{DS}=2\times V_{GS}$, $I_D=-5.6A$
C_{iss}	Input Capacitance	—	635	—	pF	$V_{GS}=0V$
C_{oss}	Output Capacitance	—	218	—	pF	$V_{DS}=-25V$ $f=1.0\text{MHz}$
C_{rss}	Reverse Transfer Capacitance	—	105	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	8.2	12	ns	$V_{DD}=-25V$, $I_D=-9.7A$, $R_G=18\Omega$ $R_D=2.4\Omega$
t_r	Rise Time	—	57	86	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	12	18	ns	(MOSFET switching times are essentially independent of operating temperature)
t_f	Fall Time	—	25	38	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	17	26	nC	$V_{GS}=-10V$, $I_D=-9.7A$, $V_{DS}=0.8\text{Max. Rating}$ (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	4.1	6.2	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	5.7	8.6	nC	

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	MAX	3.1	K/W	
R_{thCS}	Case-to-Sink	TYP	1.0	K/W	Mounting surface flat smooth, and greased
R_{thJA}	Junction-to-Ambient	MAX	80	K/W	Free Air Operation

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse width limited by max. junction temperature

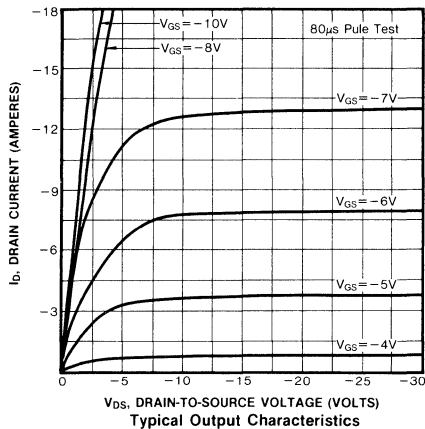
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-9.7	A	Modified MOSFET integral reverse P-N junction rectifier
I_{SM}	Pulse Source Current	—	—	-39	A	
V_{SD}	Diode Forward Voltage	—	—	-6.3	V	$T_C = 25^\circ\text{C}$, $I_S = -9.7\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	—	280	ns	$T_J = 25^\circ\text{C}$, $I_F = -9.7\text{A}$, $dI_F/dt = 10\text{S}$

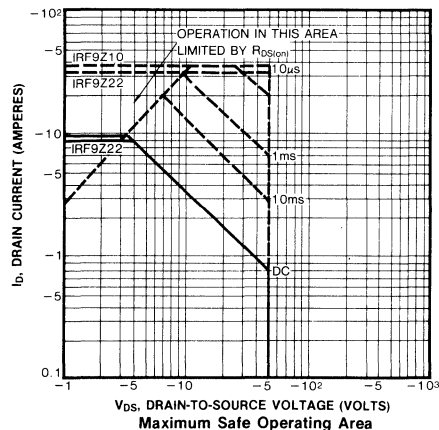
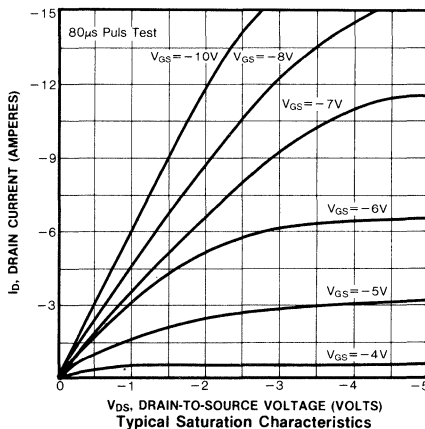
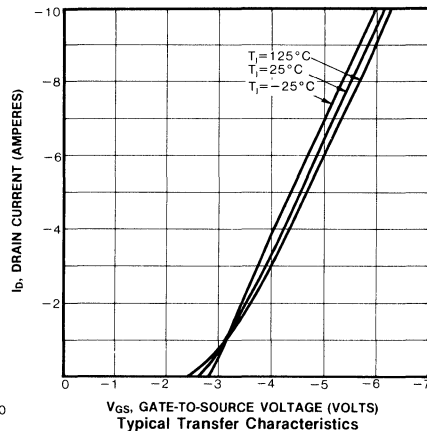
Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C

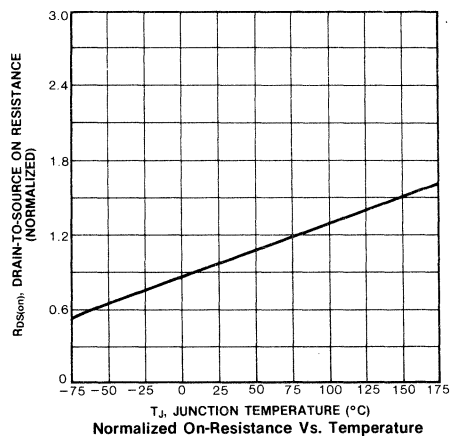
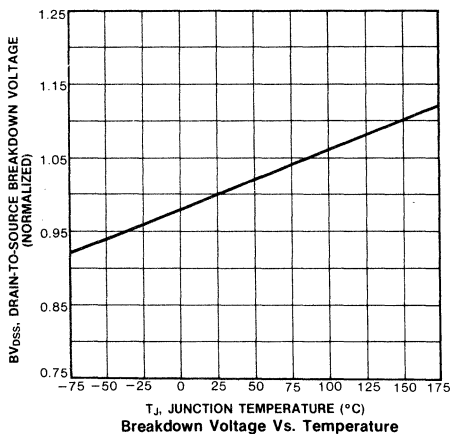
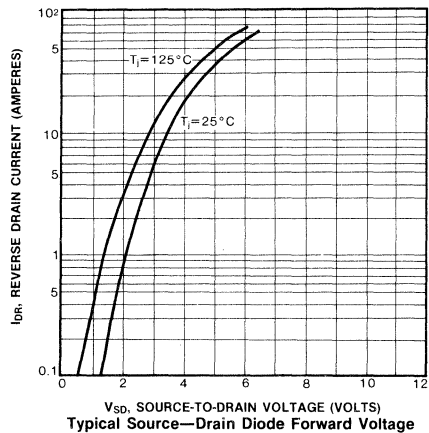
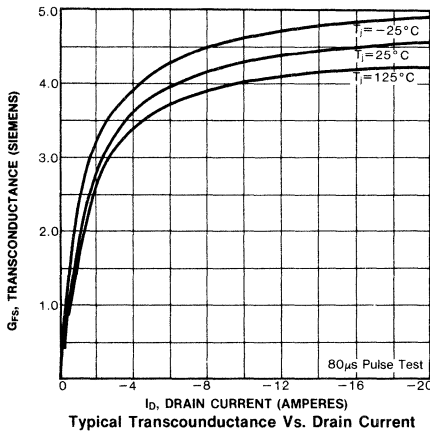
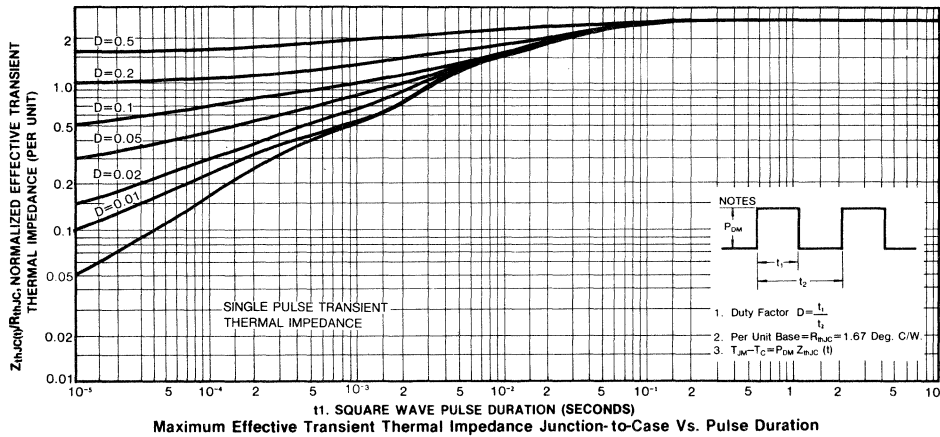
(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$

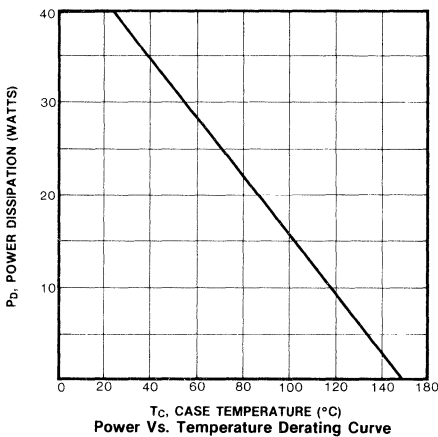
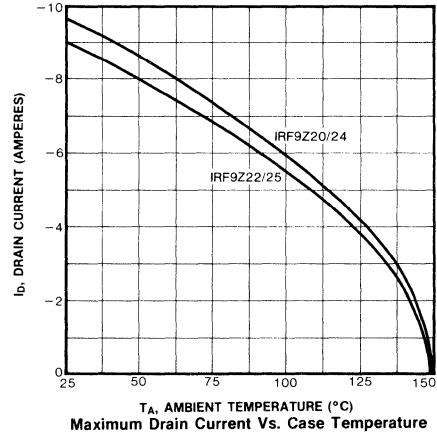
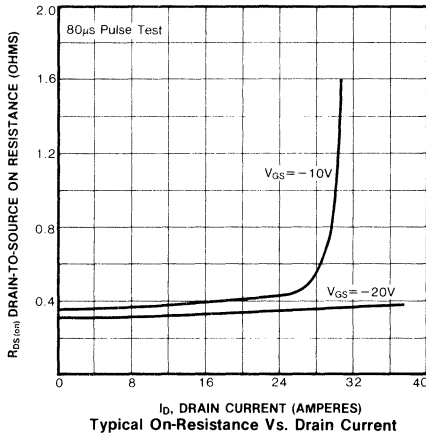
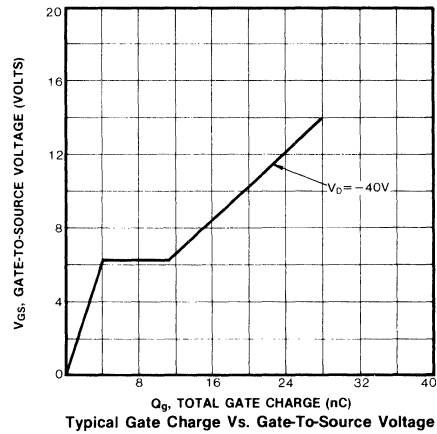
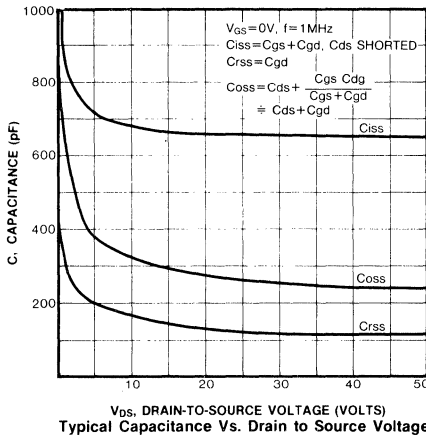
(3) Repetitive rating: Pulse with limited by max. junction temperature



IRF9Z20



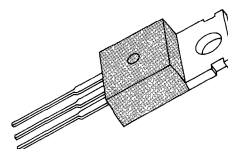




FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

TO-220



IRF9Z34/Z35
IRF9Z30/Z32

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF9Z30	-50V	0.14 Ω	-18A
IRF9Z34	-60V	0.14 Ω	-18A
IRF9Z32	-50V	0.21 Ω	-15A
IRF9Z35	-60V	0.21 Ω	-15A

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	IRF9Z30	IRF9Z32	IRF9Z34	IRF9Z35	Unit
Drain-Source Voltage (1)	V_{DS}	-50		-60V		Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	-50		-60V		Vdc
Gate-Source Voltage	V_{GS}	± 20				Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	-18	-15	-18	-15	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	-11	-9.3	-60	-50	Adc
Drain Current—Pulsed (3)	I_{DM}	-60	-50	-60	-50	Adc
Gate Current—Pulsed	I_{GM}	± 1.5				Adc
Single Avalanche Energy (4)	E_{AS}	13				mj
Avalanche Current	I_{AS}	-18				A
Total Power Dissipation at $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	74 0.59				Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150				$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300				$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=100\mu H$, $V_{dd}=-25V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV_{DS}	Drain-Source Breakdown Voltage	-60	—	—	V	$V_{GS}=0V$, $I_D = -250\mu A$
		-50	—	—	V	
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	$V_{DS}=V_{GS}$, $I_D = -250\mu A$
I_{GSS}	Gate-Source Leakage Forward	—	—	-100	nA	$V_{GS} = -20V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	100	nA	$V_{GS} = 20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0V$
		—	—	1000		$V_{DS} = 0.8 \text{Max. Rating}$, $T_C = 125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2)	-18	—	—	A	$V_{DS} \leq -3.7V$
		-15	—	—		$V_{GS} = -10V$
$R_{DS(on)}$	Static Drain-Source On-State Resistance	—	0.10	0.14	Ω	$V_{GS} = -10V$, $I_D = -9.3A$
		—	—	0.21		
g_{fs}	Forward Transconductance (2)	3.1	7.3	—	Ω	$V_{DS} = 2 \times V_{GS}$, $I_D = -9.3A$
C_{ISS}	Input Capacitance	—	1196	—	pF	$V_{GS} = 0V$
C_{OSS}	Output Capacitance	—	444	—	pF	$V_{DS} = -25V$
C_{RSS}	Reverse Transfer Capacitance	—	232	—	pF	$f = 1.0\text{MHz}$
$t_{d(on)}$	Turn-On Delay Time	—	12	18	ns	$V_{DD} = -25V$, $I_D = -18A$, $R_G = 13\Omega$ $R_D = 1.3\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	110	170	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	21	32	ns	
t_f	Fall Time	—	64	96	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	26	39	nC	$V_{GS} = -10V$, $I_D = -18A$, $V_{DS} = 0.8 \text{Max. Rating}$ (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	6.9	10	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	9.7	15	nC	

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	MAX	6.4	K/W	
R_{thCS}	Case-to-Sink	TYP	1.0	K/W	Mounting surface flat Smooth, and greased
R_{thJA}	Junction-to-Ambient	MAX	80	K/W	Free Air Operation

Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

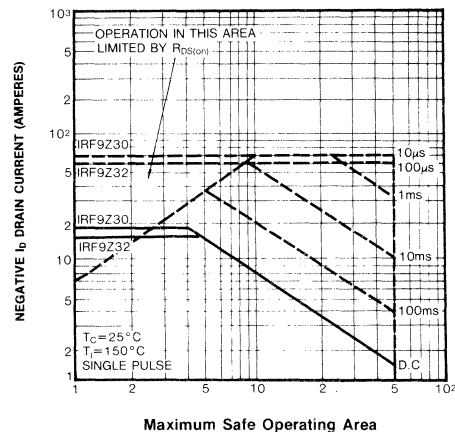
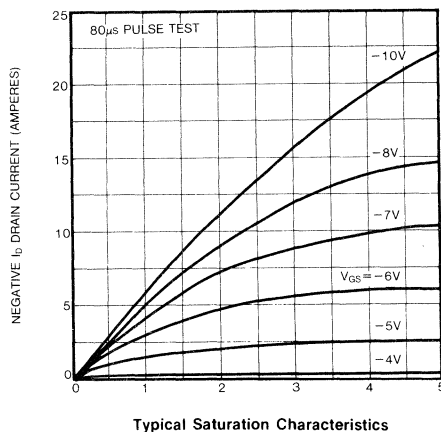
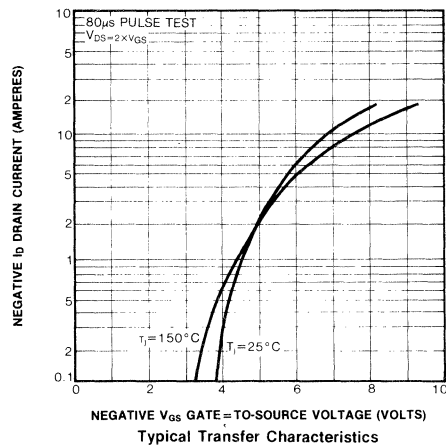
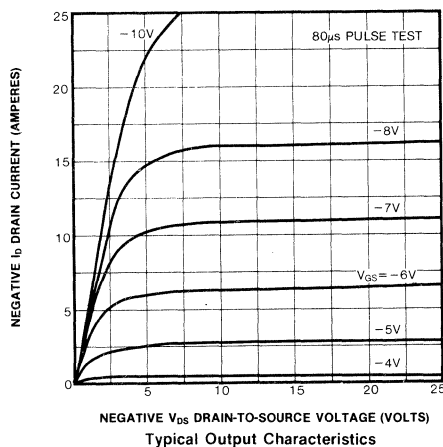
(3) Repetitive rating: Pulse width limited by max. junction temperature

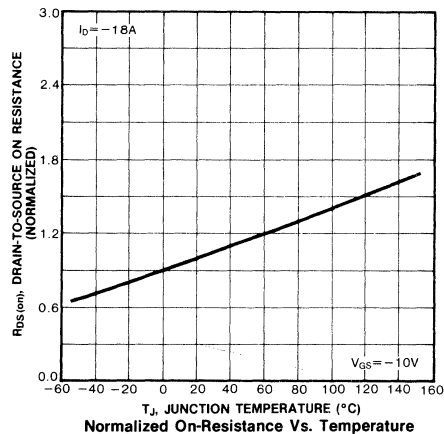
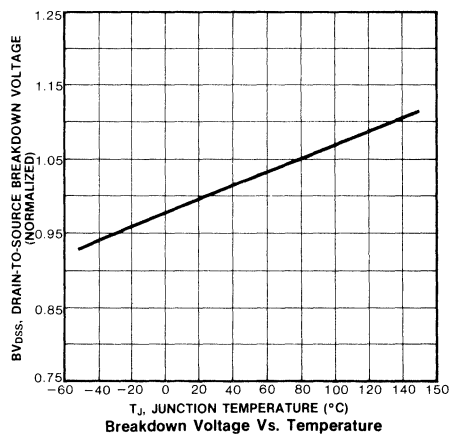
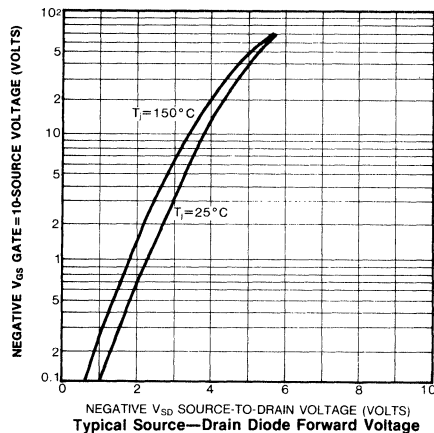
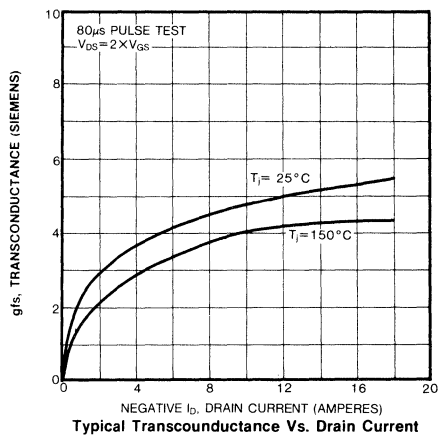
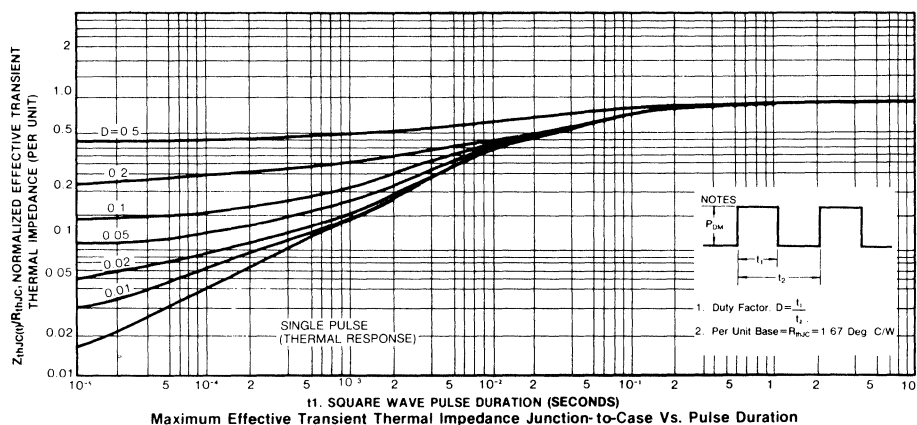
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

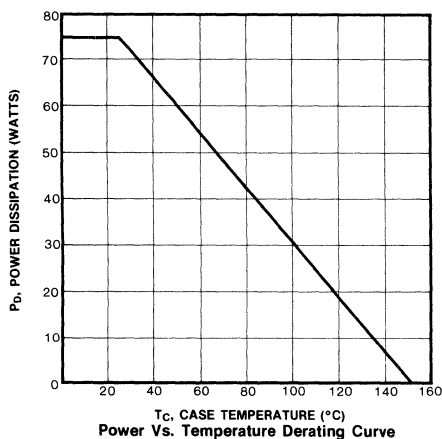
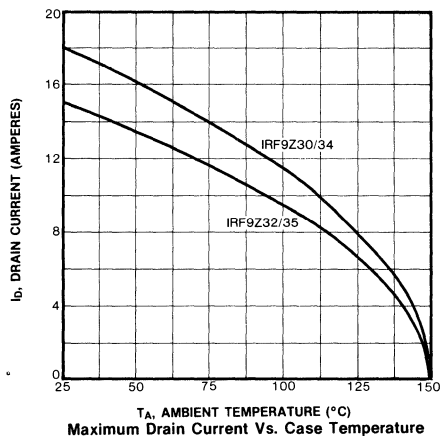
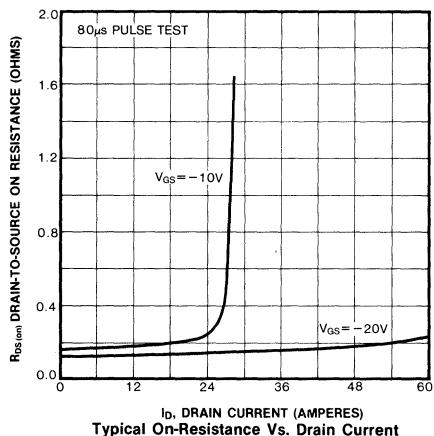
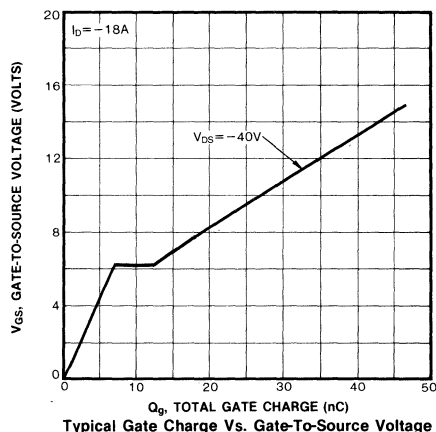
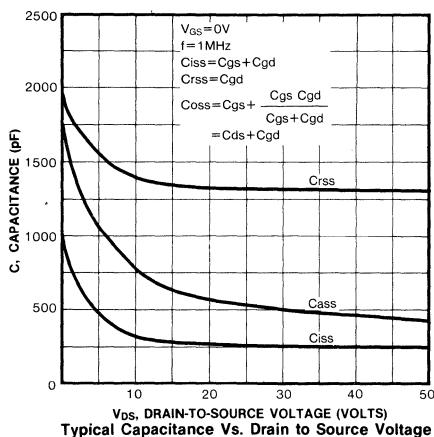
Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-18 -15	A	Modified MOSFET integral reverse P-N junction rectifier
I_{SM}	Pulse Source Current (3)	—	—	-60 -50	A	
V_{SD}	Diode Forward Voltage	—	—	-6.3	V	$T_C = 25^\circ\text{C}$, $I_S = -18\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	—	250	ns	$T_J = 25^\circ\text{C}$, $I_F = -18\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$



- Notes:** (1) $T_J = 25^\circ\text{C}$ to 150°C
(2) Pulse test: Pulse width $< 300\mu\text{s}$, Duty Cycle $< 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature



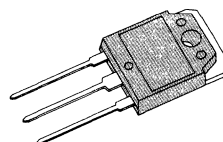




FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

TO-3P



IRFP150/151/152/153

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFP150	100V	0.055 Ω	40A
IRFP150	60V	0.055 Ω	40A
IRFP150	100V	0.08 Ω	34A
IRFP150	60V	0.08 Ω	34A

MAXIMUM RATINGS

Characteristic	Symbol	IRFP150	IRFP151	IRFP152	IRFP153	Unit
Drain-Source Voltage (1)	V_{DS}	100	60	100	60	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	100	60	100	60	Vdc
Gate-Source Voltage	V_{GS}	± 20				Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	40	40	34	34	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	26	26	22	22	Adc
Drain Current—Pulsed (3)	I_{DM}	100	100	140	140	Adc
Gate Current—Pulsed	I_{GM}	± 1.5				Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	374				mJ
Avalanche Current	I_{AS}	40				A
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$ (4)	P_D	150 1.2				Watts W/ $^\circ C$
Operating and Storage Junction to Case	T_J, T_{stg}	-55 to 150				$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300				$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=0.36 mH$, $V_{dd}=25V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-Source Breakdown Voltage IRFP150/152	100	—	—	V	V _{GS} =0V
	IRFP151/153	60	—	—	V	I _D =250μA
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} =V _{GS} , I _D =250μA
I _{GSS}	Gate-Source Leakage Forward	—	—	100	nA	V _{GS} =20V
I _{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	V _{GS} =-20V
I _{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	V _{DS} =Max. Rating, V _{GS} =0V
		—	—	1000	μA	V _{DS} =Max. Rating×0.8, V _{GS} =0V, T _C =125°C
I _{D(on)}	On-State Drain-Source Current (2) IRFP150/151	40	—	—	A	V _{DS} ≥3.2V, V _{GS} =10V
	IRFP150/151	34	—	—	A	
R _{DS(on)}	Static Drain-Source On-State Resistance (2) IRFP150/151	—	0.045	0.055	Ω	V _{GS} =10V, I _D =22A
	IRFP152/153	—	0.06	0.08	Ω	
g _{fs}	Forward Transconductance (2)	13.0	20	—	Ω	V _{DS} ≥50V, I _D =20A
C _{iss}	Input Capacitance	—	2400	—	pF	V _{GS} =0V, V _{DS} =25V, f=1.0MHz
C _{oss}	Output Capacitance	—	1000	—	pF	
C _{rss}	Reverse Transfer Capacitance	—	200	—	pF	
t _{d(on)}	Turn-On Delay Time	—	—	24	ns	V _{DD} =0.5BV _{DSS} , I _D =20A, Z _O =4.7Ω (MOSFET switching times are essentially independent of operating temperature)
t _r	Rise Time	—	—	210	ns	
t _{d(off)}	Turn-Off Delay Time	—	—	84	ns	
t _f	Fall Time	—	—	140	ns	
Q _g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	72	110	nC	V _{GS} =10V, I _D =38A, V _{DS} =0.8 Max. Rating (Gate charge is essentially independent of operating temperature.)
Q _{gs}	Gate-Source Charge	—	18	—	nC	
Q _{gd}	Gate-Drain ("Miller") Charge	—	27	—	nC	

THERMAL RESISTANCE

Symbol	Characteristic		IRFP150-3	Unit	
R _{thJC}	Junction-to-Case	MAX	0.7	K/W	
R _{thCS}	Case-to-Sink	TYP	0.1	K/W	Mounting surface flat, smooth, and greased
R _{thJA}	Junction-to-Ambient	MAX	40	K/W	Free Air Operation

Notes: (1) T_J=25°C to 150°C

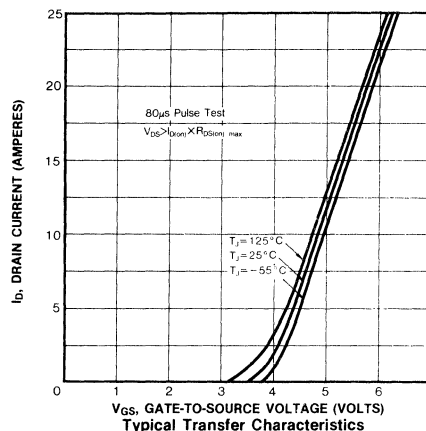
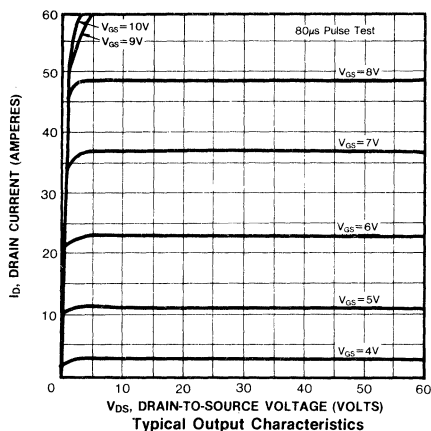
(2) Pulse test: Pulse width≤300μs, Duty Cycle≤2%

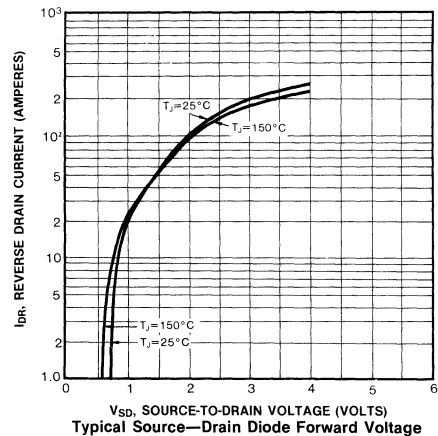
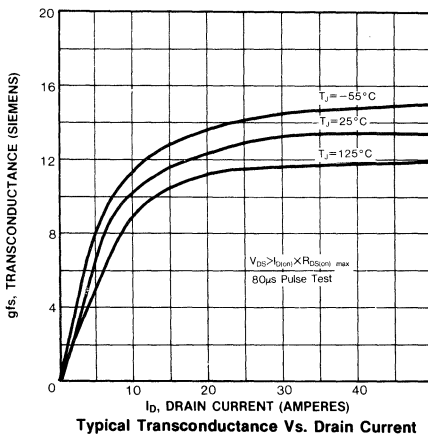
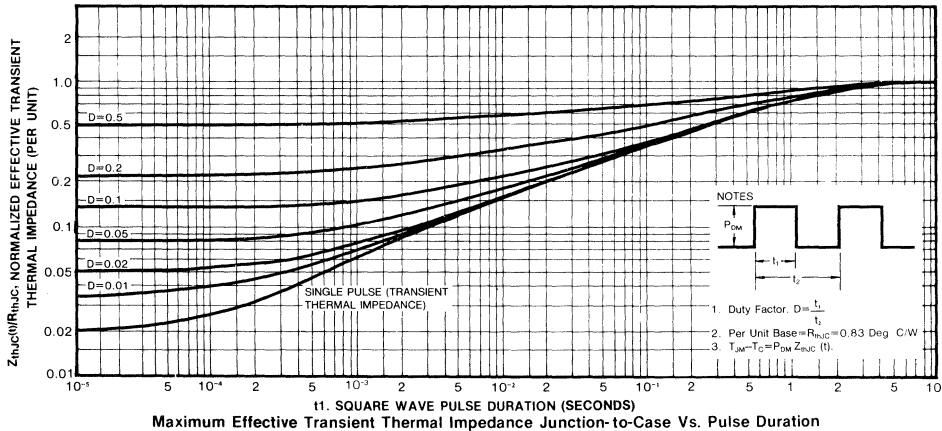
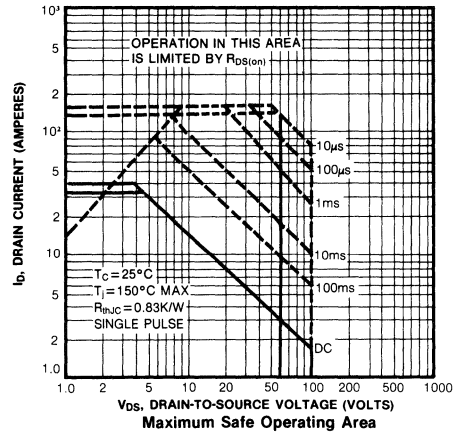
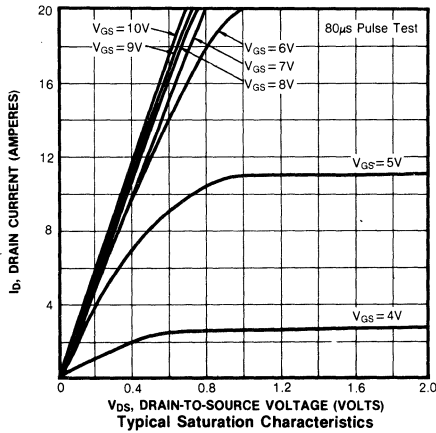
(3) Repetitive rating: Pulse width limited by max. junction temperature

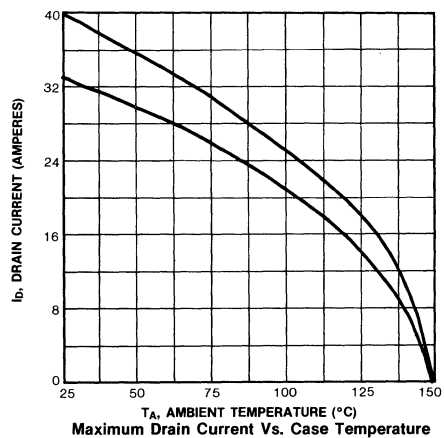
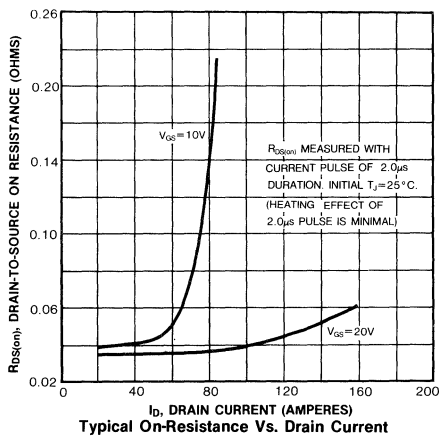
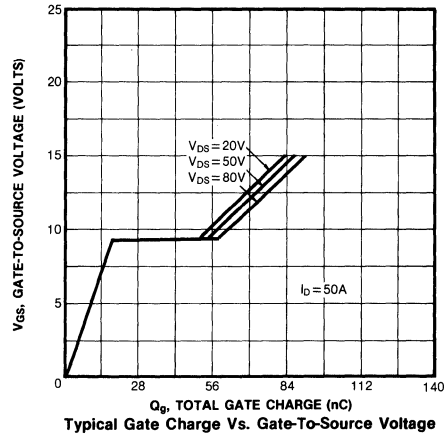
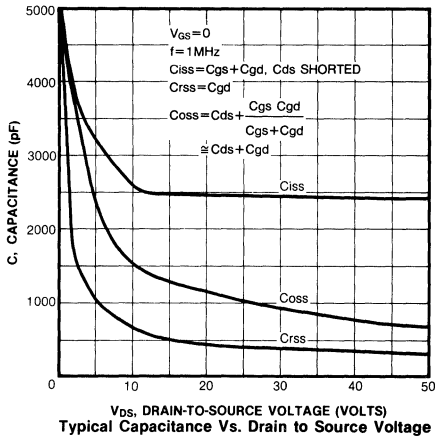
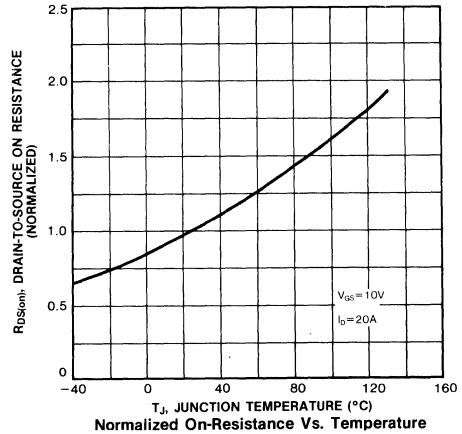
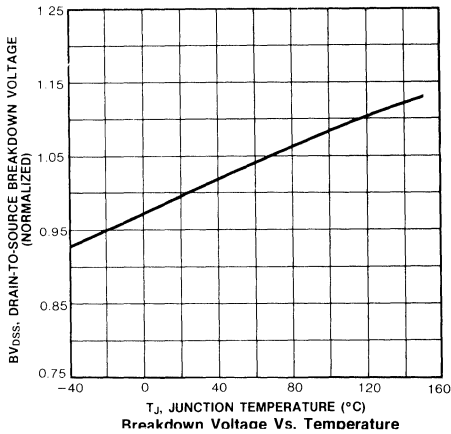
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

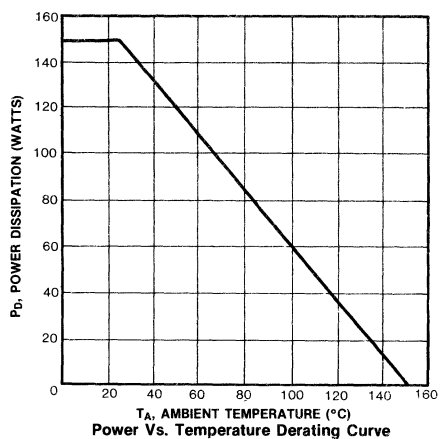
Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode) IRFP150/151	—	—	40	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier 
	IRFP150/151	—	—	34	A	
I_{SM}	Pulse Source Current(Body Diode)(3) IRFP150/151	—	—	160	A	
	IRFP152, 153	—	—	132	A	
V_{SD}	Diode Forward Voltage (2) IRFP150/151	—	—	2.5	V	$T_C=25^\circ\text{C}$, $I_S=40\text{A}$, $V_{GS}=0\text{V}$
	IRFP152/151	—	—	2.3	V	$T_C=25^\circ\text{C}$, $I_S=34\text{A}$, $V_{GS}=0\text{V}$
t_{rr}	Reverse Recovery Time	—	220	530	ns	$T_J=25^\circ\text{C}$, $I_F=40\text{A}$, $dI_F/dt=100\text{A}/\mu\text{S}$

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature



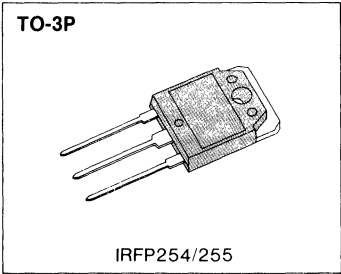






FEATURES

- Lower $R_{DS(ON)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability



PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFP254	250V	0.14 Ω	23A
IRFP255	250V	0.17	21A

MAXIMUM RATINGS

Characteristic	Symbol	IRFP254	IRFP255	Unit
Drain-Source Voltage (1)	V_{DSS}	250	250	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	250	250	Vdc
Gate-Source Voltage	V_{GS}	± 20		Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	23	21	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	15	13	Adc
Drain Current—Pulsed (3)	I_{DM}	92	84	Adc
Gate Current—Pulsed	I_{GM}	± 1.5		Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	800		mJ
Avalanche Current	I_{AS}	23		A
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	150 1.2		Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300		$^\circ C$

- Notes: (1) $T_J=25^\circ C$ to $150^\circ C$
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature
(4) $L=3\text{ mH}$, $V_{dd}=50V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage	250	—	—	V	$V_{GS}=0V$ $I_D=250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}$, $I_D=250\mu A$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS}=20V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	$V_{GS}=-20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS}=\text{Max. Rating}$, $V_{GS}=0V$
		—	—	1000	μA	$V_{DS}=\text{Max. Rating} \times 0.8$, $V_{GS}=0V$, $T_C=125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2) IRFP254	23	—	—	A	$V_{DS} \geq 3.9V$, $V_{GS}=10V$
	IRFP255	21	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance (2) IRFP254	—	0.098	0.14	Ω	$V_{GS}=10V$, $I_D=13A$
	IRFP255	—	0.14	0.17	Ω	
g_{fs}	Forward Transconductance (2)	11	18.5	—	Ω	$V_{DS} \geq 50V$, $I_D=13A$
C_{iss}	Input Capacitance	—	2890	—	pF	$V_{GS}=0V$, $V_{DS}=25V$, $f=1.0\text{MHz}$
C_{oss}	Output Capacitance	—	376	—	pF	
C_{rss}	Reverse Transfer Capacitance	—	140	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	19	29	ns	$V_{DD}=0.5BV_{DSS}$, $I_D=22A$, $Z_O=6.2\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	84	130	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	75	110	ns	
t_f	Fall Time	—	65	98	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	87	130	nC	$V_{GS}=10V$, $I_D=22A$, $V_{DS}=0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	14	20	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	73	110	nC	

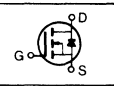
THERMAL RESISTANCE

Symbol	Characteristic		IRFP254-5	Unit	Test Conditions
R_{thJC}	Junction-to-Case	MAX	0.83	K/W	
R_{thCS}	Case-to-Sink	TYP	0.24	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	MAX	40	K/W	Free Air Operation

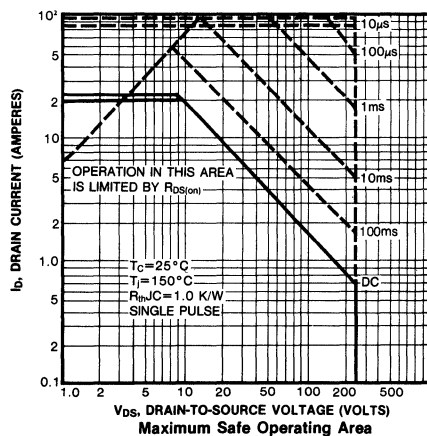
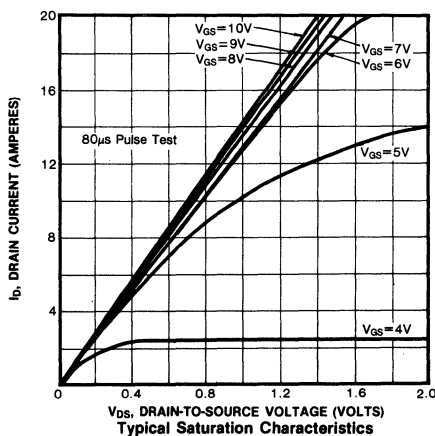
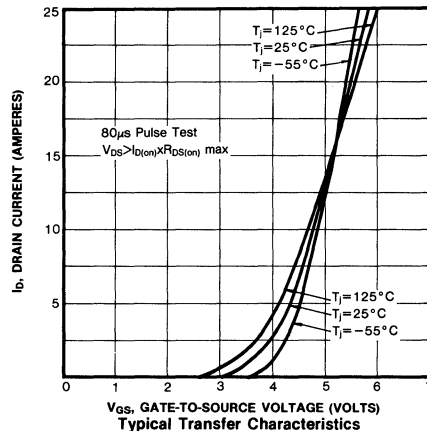
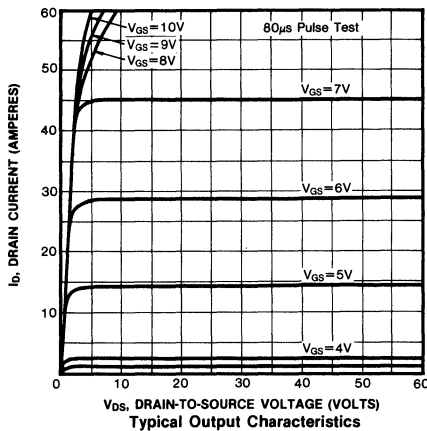
Notes: (1) $T_J=25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

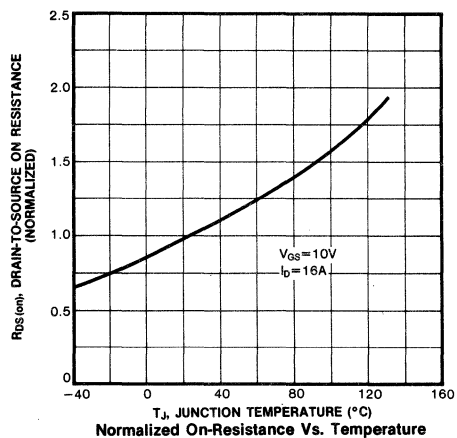
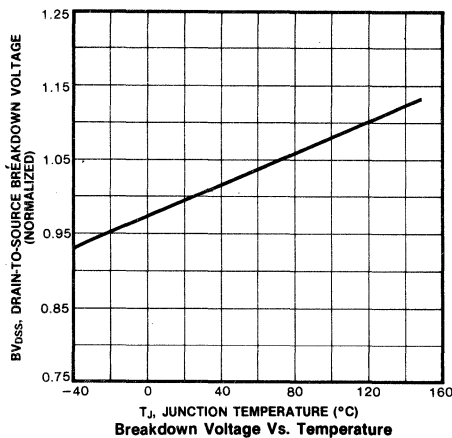
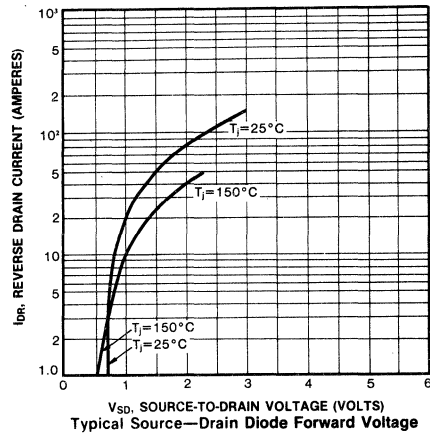
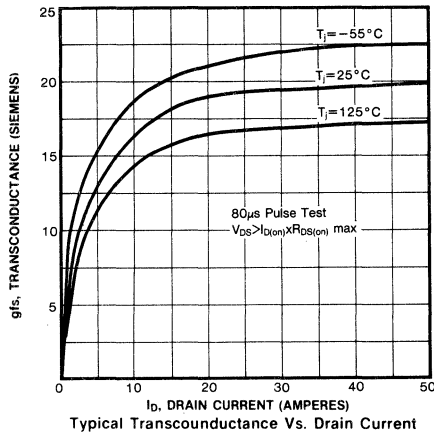
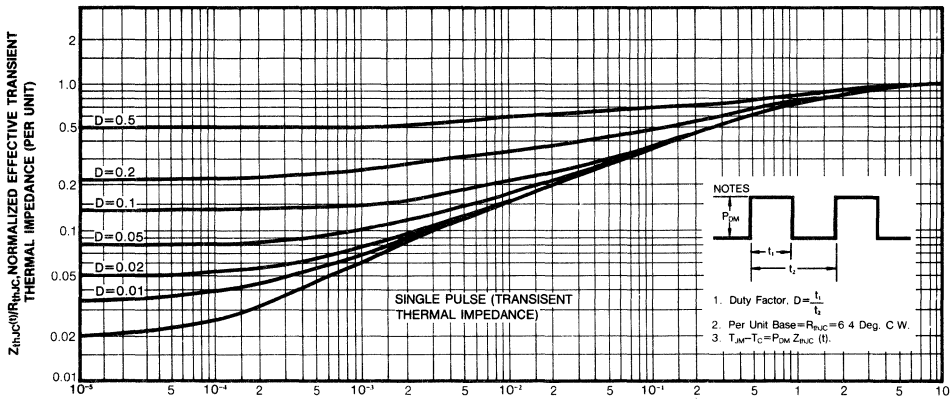
(3) Repetitive rating: Pulse width limited by max. junction temperature

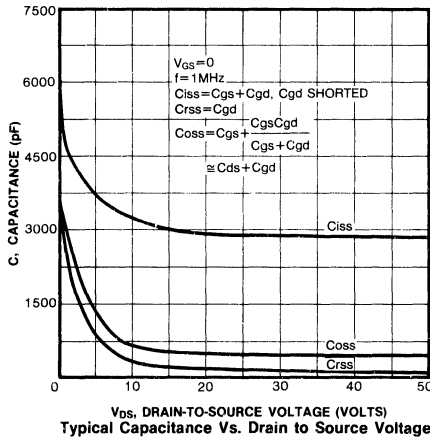
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode) IRFP254	—	—	23	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier 
	IRFP255	—	—	21	V	
I_{SM}	Pulse Source Current (Body Diode) (3) IRFP254	—	—	92	A	
	IRFP255	—	—	84	V	
V_{SD}	Diode Forward Voltage (2)	—	—	1.8	V	$T_C = 25^\circ\text{C}$, $I_S = 23\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	310	—	ns	$T_J = 25^\circ\text{C}$, $I_F = 22\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{s}$

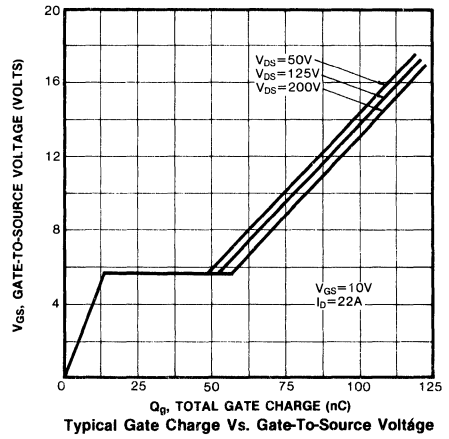
Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
 (3) Repetitive rating: Pulse with limited by max. junction temperature



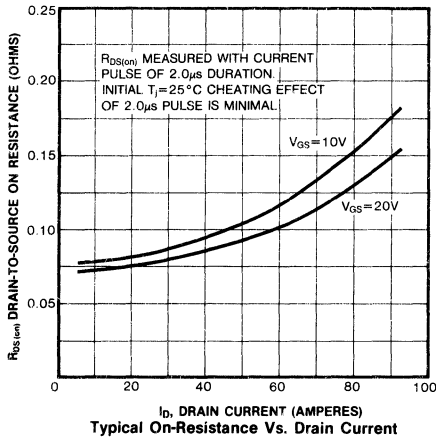




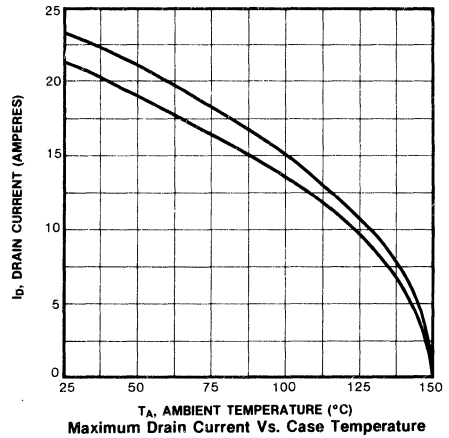
Typical Capacitance Vs. Drain to Source Voltage



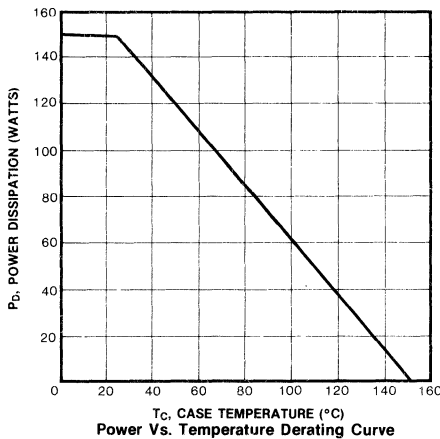
Typical Gate Charge Vs. Gate-To-Source Voltage



Typical On-Resistance Vs. Drain Current



Maximum Drain Current Vs. Case Temperature



Power Vs. Temperature Derating Curve

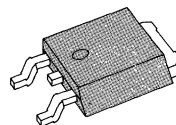
FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

PRODUCT SUMMARY

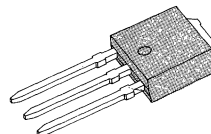
Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFR010/U010	50V	$0.20\ \Omega$	8.2A
IRFR012/U012	50V	$0.30\ \Omega$	6.7A
IRFR014/U014	60V	$0.20\ \Omega$	8.2A
IRFR015/U015	60V	$0.32\ \Omega$	6.7A

D-PACK



IRFR010/012
 IRFR014/015

I-PACK



IRFU010/012
 IRFU014/015

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	IRFR010 IRFU010	IRFR012 IRFU012	IRFR014 IRFU014	IRFR015 IRFU015	Unit
Drain-Source Voltage (1)	V _{DSS}	50		60		V _{dc}
Drain-Gate Voltage (R _{GS} =1.0MΩ)(1)	V _{DGR}	50		60		V _{dc}
Gate-Source Voltage	V _{GS}	±20				V _{dc}
Continuous Drain Current T _C =25°C	I _D	8.2	6.7	8.2	6.7	A _{dc}
Continuous Drain Current T _C =100°C	I _D	5.2	4.2	5.2	4.2	A _{dc}
Drain Current—Pulsed (3)	I _{DM}	33	27	33	27	A _{dc}
Gate Current—Pulsed	I _{GM}	±1.5				A _{dc}
Single Pulsed Avalanche Energy (4)	E _{AS}	1.4				mJ
Avalanche Current	I _{AS}	8.2				A
Total Power Dissipation at T _C =25°C Derate above 25°C	P _D	25 0.20				Watts W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	−55 to 150				°C
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T _L	300				°C

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=50\mu H$, $V_{dd}=25V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage					
	IRFR014/015, IRFU014/015	60	—	—	V	$V_{GS}=0V, I_D=250\mu A$
	IRFR010/012, IRFU010/012	50	—	—	V	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}, I_D=250\mu A$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS}=20V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	$V_{GS}=-20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS}=\text{Max. Rating}, V_{GS}=0V$
		—	—	1000		$V_{DS}=0.8 \text{ Max Rating}, V_{GS}=0V, T_J=125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2)					$V_{DS}\geq 2.4V, V_{GS}=10V$
	IRFR010/014, IRFU010/014	8.2	—	—	A	
	IRFR012/015, IRFU012/015	6.7	—	—		
$R_{DS(on)}$	Static Drain-Source					
	IRFR010/014, IRFU010/014	—	0.15	0.20	Ω	$V_{GS}=10V, I_D=4.2A$
	IRFR012/015, IRFU012/015	—	—	0.30		
g_{fs}	Forward Transconductance (2)	2.1	—	—	U	$V_{DS}\geq 50V, I_D=3.6A$
C_{iss}	Input Capacitance	—	358	—	pF	$V_{GS}=0V$
C_{oss}	Output Capacitance	—	134	—	pF	$V_{DS}=25V$
C_{rss}	Reverse Transfer Capacitance	—	55	—	pF	$f=1.0\text{MHz}$
$t_{d(on)}$	Turn-On Delay Time	—	—	17	ns	$V_{DD}=0.5 BV_{DSS}, I_D=7.3A, Z_O=24\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	—	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	—	18	ns	
t_f	Fall Time	—	—	35	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	—	10	nC	$V_{GS}=10V, I_D=7.3A, V_{DS}=0.8\text{Max. Rating}$ (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	—	2.6	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	—	4.8	nC	

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	MAX	5.0	K/W	
R_{thCS}	Case-to-Sink	TYP	1.7	K/W	Mounting surface flat smooth, and greased
R_{thJA}	Junction-to-Ambient	MAX	110	K/W	Free Air Operation

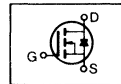
Notes: (1) $T_J=25^\circ\text{C}$ to 150°C

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse width limited by max. junction temperature

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

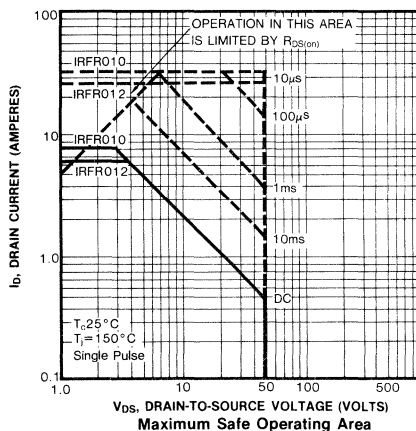
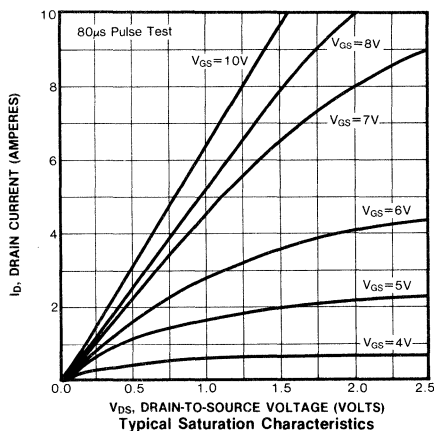
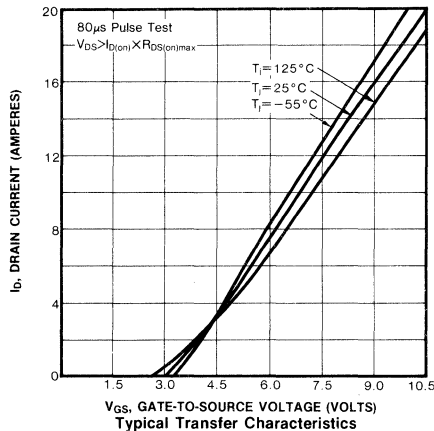
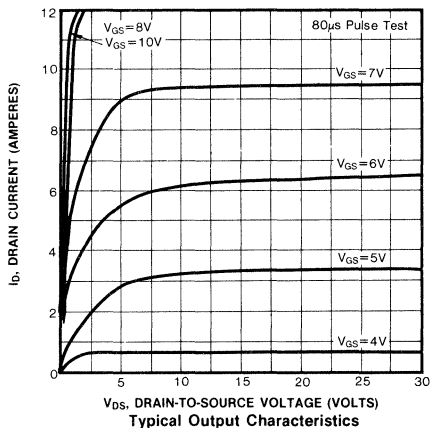
Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode) IRFR010/014, IRFU010/014 IRFR010/015, IRFU012/015	—	—	8.2 6.7	A A	Modified MOSFET integral reverse P-N junction rectifier
I_{SM}	Pulse Source Current (3) IRFR010/014, IRFU010/014 IRFR012/015, IRFU012/015	—	—	33 27	A A	
V_{SD}	Diode Forward Voltage	—	—	1.6	V	$T_C = 25^\circ\text{C}$, $I_S = 8.2\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	—	190	ns	$T_J = 25^\circ\text{C}$, $I_F = 7.3\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{s}$

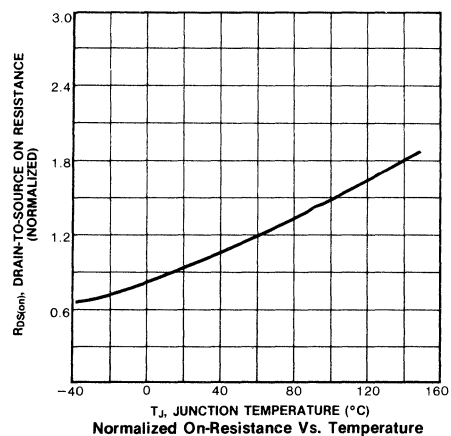
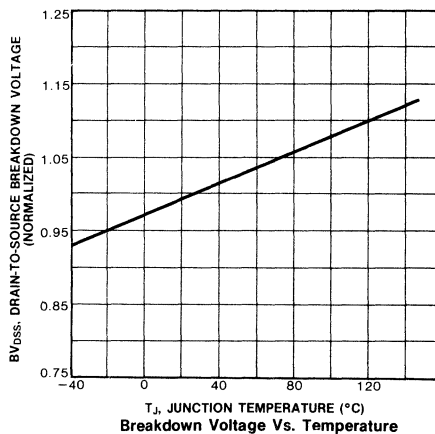
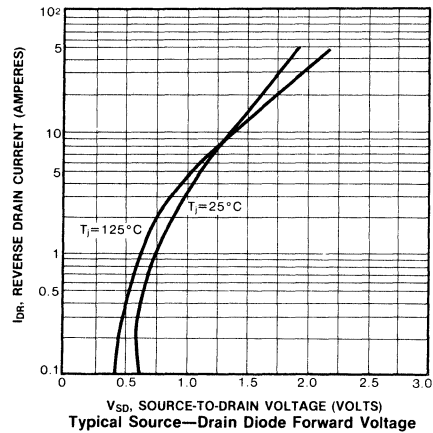
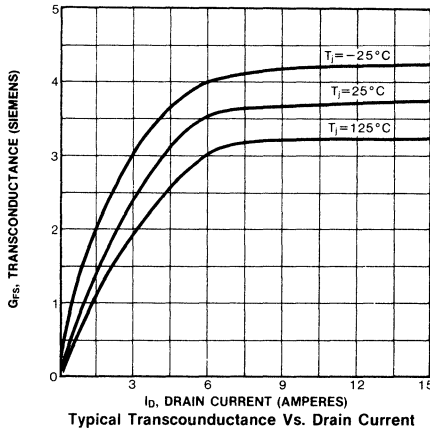
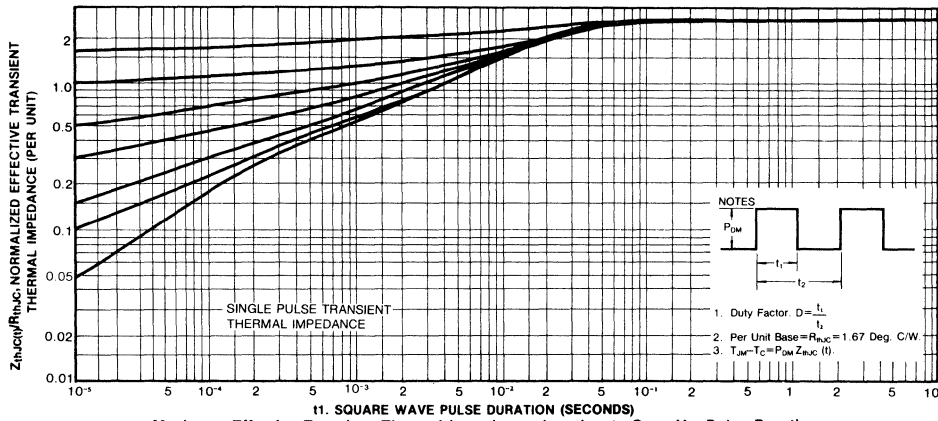


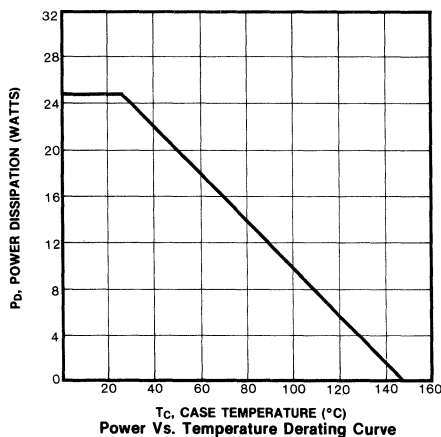
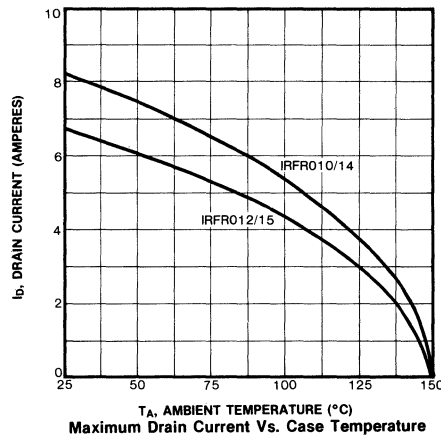
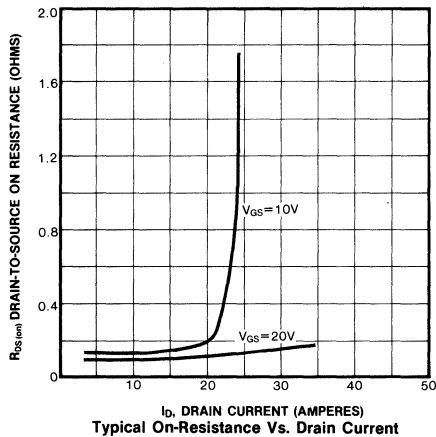
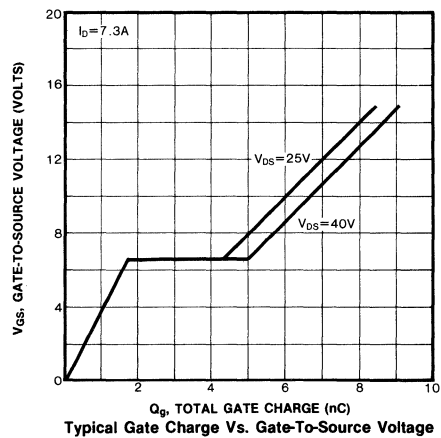
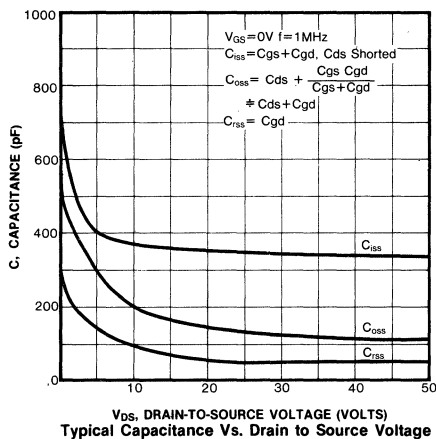
Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C

(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature







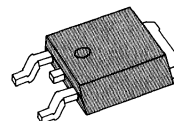
FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

PRODUCT SUMMARY

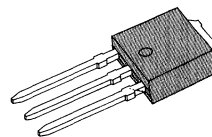
Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFR020/U020	50V	0.10 Ω	15A
IRFR022/U022	50V	0.12 Ω	14A
IRFR024/U024	60V	0.10 Ω	15A
IRFR025/U025	60V	0.12 Ω	14A

D-PACK



IRFR020/012
IRFR024/025

I-PACK



IRFU020/012
IRFU024/025

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	IRFR020 IRFU020	IRFR022 IRFU022	IRFR024 IRFU024	IRFR025 IRFU025	Unit
Drain-Source Voltage (1)	V _{DSS}	50		60		Vdc
Drain-Gate Voltage (R _{GS} =1.0MΩ)(1)	V _{DGR}	50		60		Vdc
Gate-Source Voltage	V _{GS}	±20				Vdc
Continuous Drain Current T _C =25°C	I _D	15	14	15	14	Adc
Continuous Drain Current T _C =100°C	I _D	9.6	8.7	9.6	8.7	Adc
Drain Current—Pulsed (3)	I _{DM}	60	56	60	56	Adc
Gate Current—Pulsed	I _{GM}	±1.5				Adc
Single Pulsed Avalanche Energy (4)	E _{AS}	9.5				mJ
Avalanche Current	I _{AS}	15				A
Total Power Dissipation at T _C =25°C Derate above 25°C	P _D	42 0.33				Watts W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	−55 to 150				°C
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T _L	300				°C

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=100\mu H$, $V_{dd}=25V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage IRFR024/025, IRFU024/025 IRFR020/022, IRFU020/022	60	—	—	V	$V_{GS}=0V$, $I_D=250\mu A$
		50	—	—	V	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}$, $I_D=250\mu A$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS}=20V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	$V_{GS}=-20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS}=\text{Max. Rating}$, $V_{GS}=0V$ $V_{DS}=0.8 \text{ Max Rating}$, $V_{GS}=0V$, $T_J=125^\circ\text{C}$
		—	—	1000		
$I_{D(on)}$	On-State Drain-Source Current (2) IRFR020/024, IRFU020/024 IRFR022/025, IRFU022/025	15	—	—	A	$V_{DS}\geq 1.8V$, $V_{GS}=10V$
		14	—	—		
$R_{DS(on)}$	Static Drain-Source IRFR020/024, IRFU020/024 IRFR022/025, IRFU022/025	—	0.08	0.10	Ω	$V_{GS}=10V$, $I_D=8.7A$
		—	—	0.12	Ω	
g_{fs}	Forward Transconductance (2)	3.6	—	—	Ω	$V_{DS}\geq 50V$, $I_D=8.7A$
C_{iss}	Input Capacitance	—	635	—	pF	$V_{GS}=0V$
C_{oss}	Output Capacitance	—	218	—	pF	$V_{DS}=25V$
C_{rss}	Reverse Transfer Capacitance	—	105	—	pF	$f=1.0\text{MHz}$
$t_{d(on)}$	Turn-On Delay Time	—	7.3	—	ns	$V_{DD}=0.5 BV_{DSS}$, $I_D=15A$, $Z_O=18\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	17.8	—	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	20.4	—	ns	
t_f	Fall Time	—	14.5	—	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	38.5	—	nC	$V_{GS}=10V$, $I_D=15A$, $V_{DS}=0.8\text{Max. Rating}$ (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	8.75	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	17.8	—	nC	

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	MAX	3.0	K/W	
R_{thCS}	Case-to-Sink	TYP	1.7	K/W	Mounting surface flat smooth, and greased
R_{thJA}	Junction-to-Ambient	MAX	110	K/W	Free Air Operation

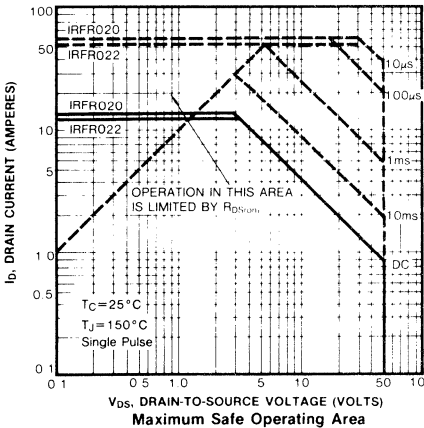
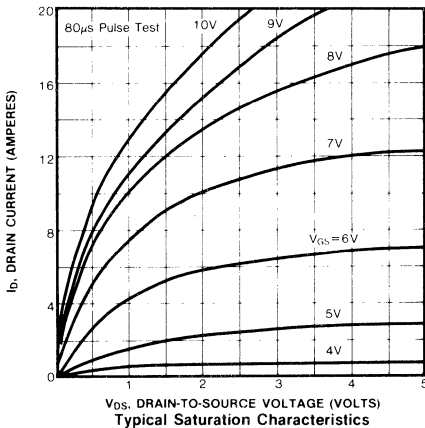
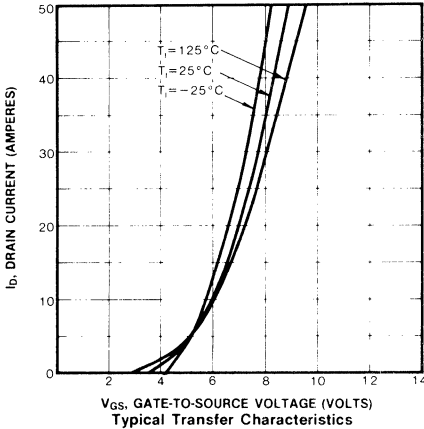
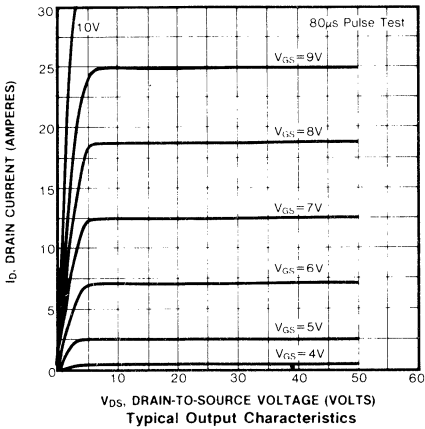
- Notes:** (1) $T_J=25^\circ\text{C}$ to 150°C
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse width limited by max. junction temperature

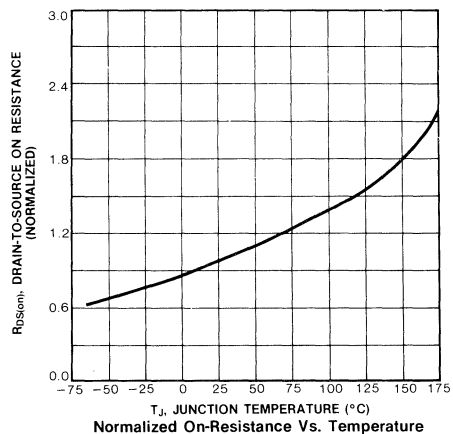
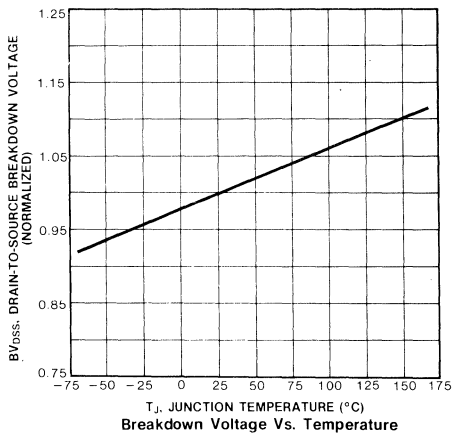
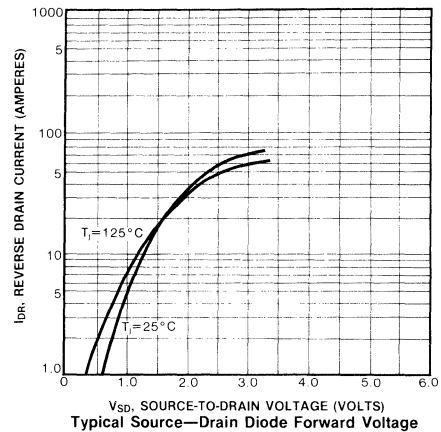
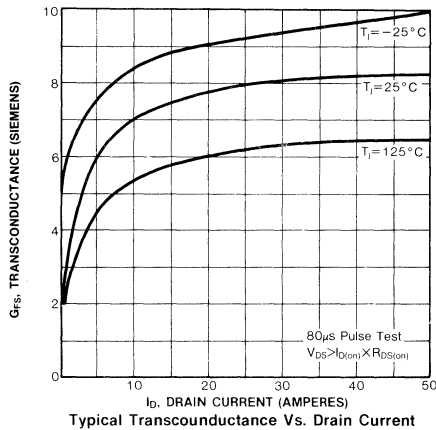
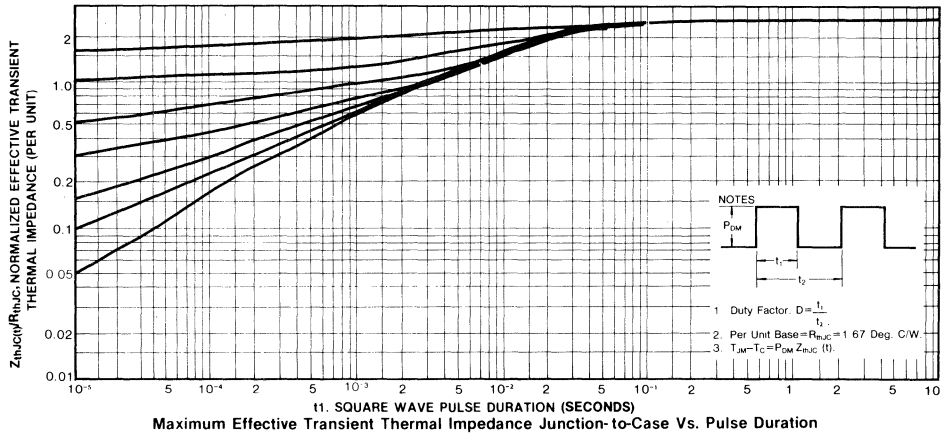
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

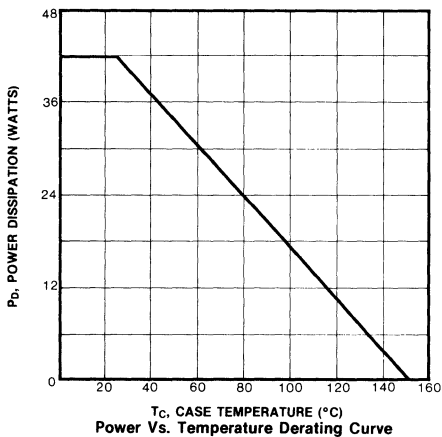
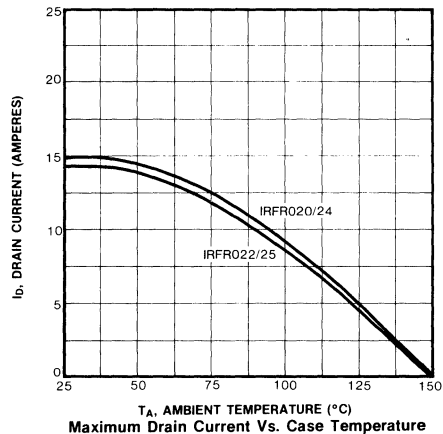
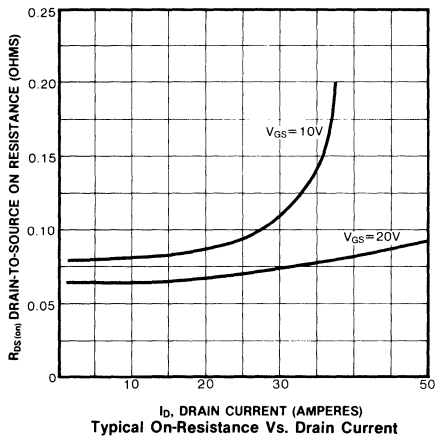
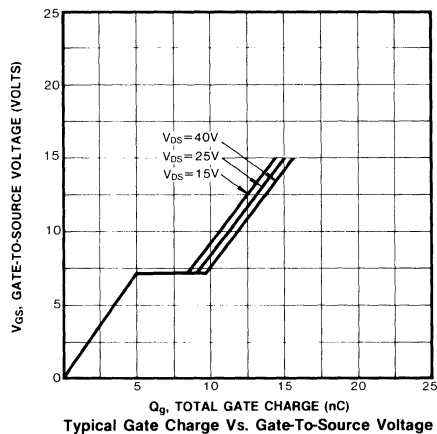
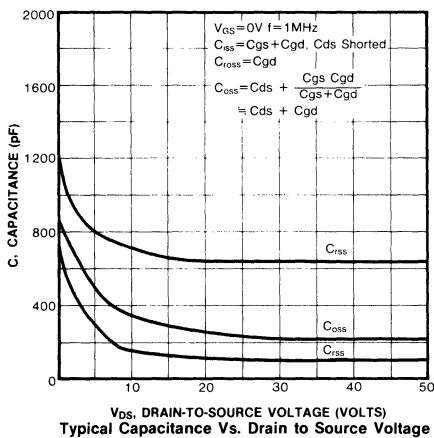
Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	15	A	Modified MOSFET integral reverse P-N junction rectifier
I_{SM}	Pulse Source Current (3)	—	—	60	A	
V_{SD}	Diode Forward Voltage	—	—	1.4	V	$T_C=25^{\circ}\text{C}$, $I_S=15\text{A}$, $V_{GS}=0\text{V}$
t_{rr}	Reverse Recovery Time	—	—	310	ns	$T_J=25^{\circ}\text{C}$, $I_F=15\text{A}$, $dI_F/dt=100\text{A}/\mu\text{S}$

- Notes: (1) $T_J=25^{\circ}\text{C}$ to 150°C
(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature

2







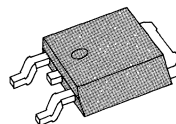
FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

PRODUCT SUMMARY

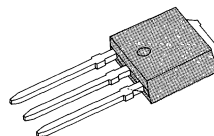
Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFR110/U110	100V	0.54Ω	4.7A
IRFR111/U111	80V	0.54Ω	4.7A

D-PACK



IRFR110/111

I-PACK



IRFU110/111

MAXIMUM RATINGS

Characteristic	Symbol	IRFR110/U110	IRFR111/U111	Unit
Drain-Source Voltage (1)	V_{DSS}	100	80	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	100	80	Vdc
Gate-Source Voltage	V_{GS}	± 20		Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	4.7		Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	3.3		Adc
Drain Current—Pulsed (3)	I_{DM}	17		Adc
Gate Current—Pulsed	I_{GM}	± 1.5		Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	13		mJ
Avalanche Current	I_{AS}	4.7		A
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	25 0.20		Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300		$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=0.91mH$, $V_{dd}=25V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage IRFR110/U110	100	—	—	V	$V_{GS}=0V$
	IRFR111/U111	80	—	—	V	$I_D=250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}$, $I_D=250\mu A$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS}=20V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	$V_{GS}=-20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS}=\text{Max. Rating}$, $V_{GS}=0V$
		—	—	1000	μA	$V_{DS}=\text{Max. Rating} \times 0.8$, $V_{GS}=0V$, $T_C=125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2)	4.7	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$, $V_{GS}=10V$
$R_{DS(on)}$	Static Drain-Source On-State Resistance (2)	—	0.37	0.54	Ω	$V_{GS}=10V$, $I_D=3.3A$
g_{fs}	Forward Transconductance (2)	1.3	1.8	—	S	$V_{DS} \geq 50V$, $I_D=3.3A$
C_{iss}	Input Capacitance	—	180	—	pF	$V_{GS}=0V$, $V_{DS}=25V$, $f=1.0\text{MHz}$
C_{oss}	Output Capacitance	—	67	—	pF	
C_{rss}	Reverse Transfer Capacitance	—	29	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	7.6	11	ns	$V_{DD}=0.5BV_{DSS}$, $I_D=5.6A$, $Z_O=4.7\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	24	36	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	14	21	ns	
t_f	Fall Time	—	14	21	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	5.2	7.7	nC	$V_{GS}=10V$, $I_D=10A$, $V_{DS}=0.8$ Max. Rating (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	1.5	2.3	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	2.2	3.2	nC	

THERMAL RESISTANCE

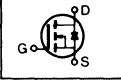
R_{thJC}	Junction-to-Case	MAX	5.0	K/W	
R_{thCS}	Case-to-Sink	TYP	1.7	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	MAX	110	K/W	Free Air Operation

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C

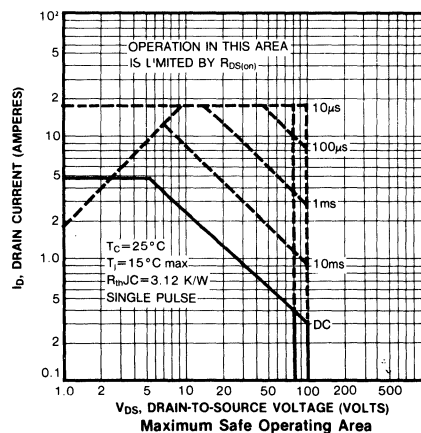
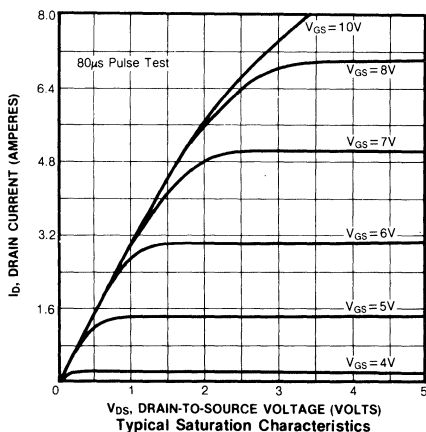
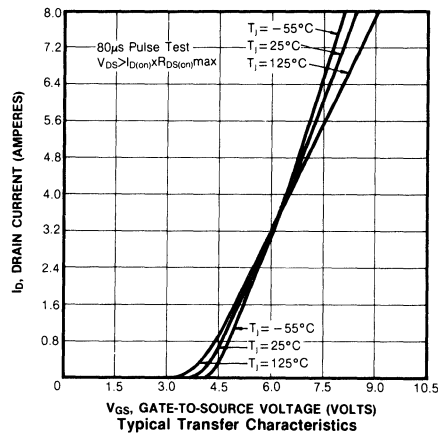
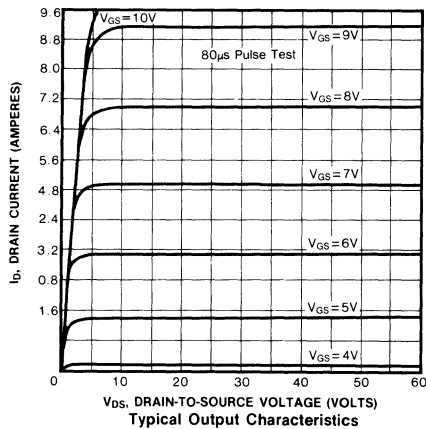
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

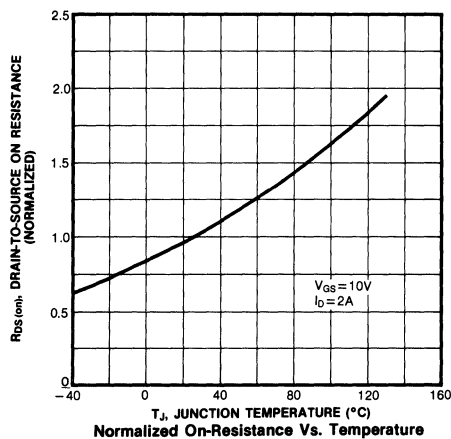
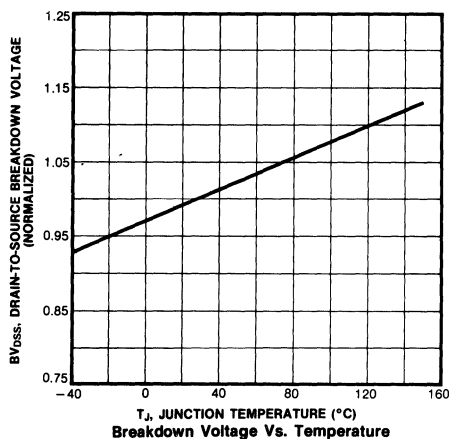
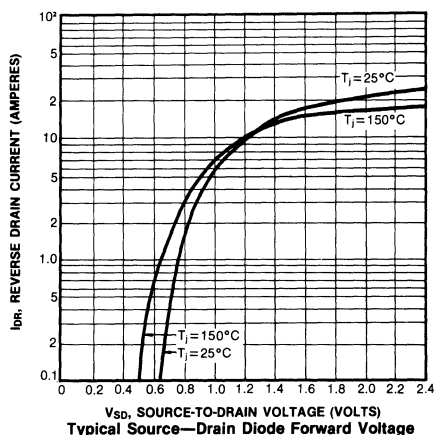
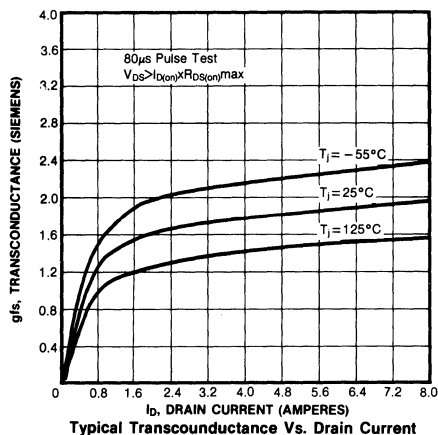
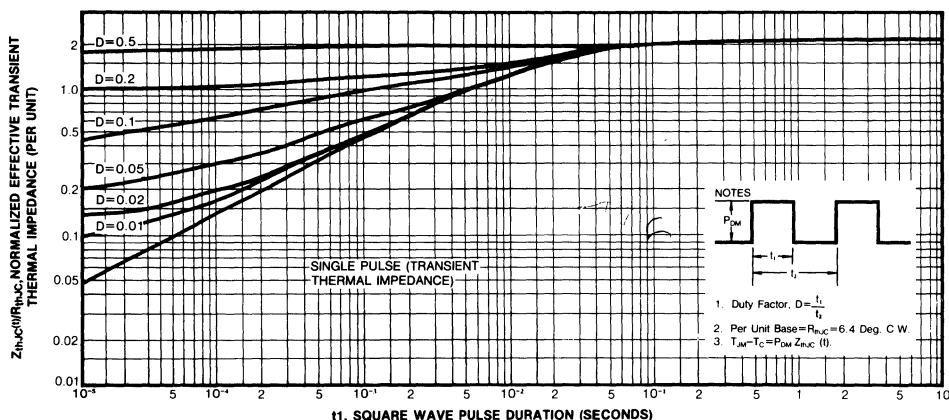
(3) Repetitive rating: Pulse width limited by max. junction temperature

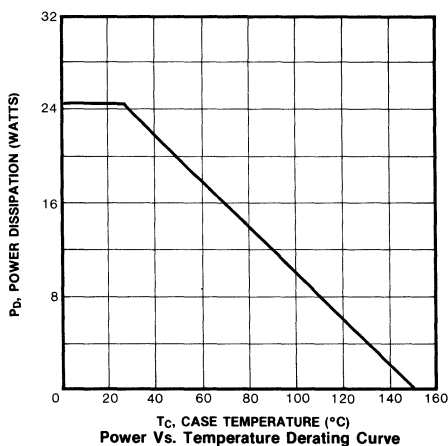
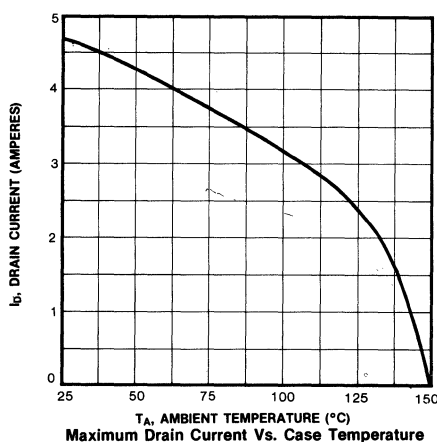
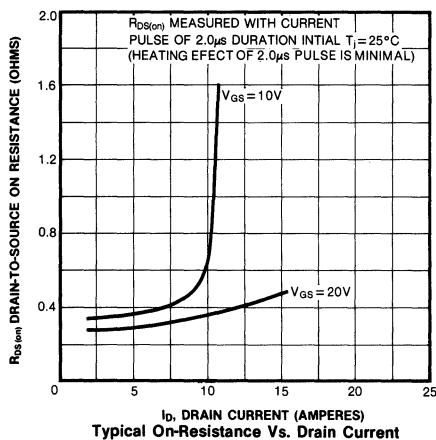
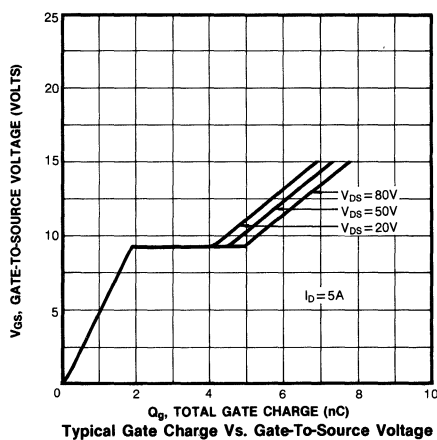
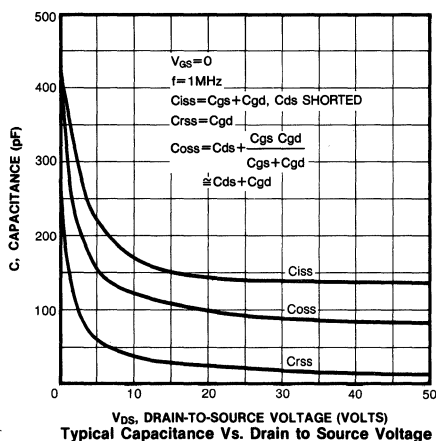
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	4.7	A	Modified MOSFET showing the integral reverse P-N junction rectifier 
I_{SM}	Pulse Source Current(Body Diode)(3)	—	—	17	A	
V_{SD}	Diode Forward Voltage (2)	—	—	2.5	V	$T_C=25^\circ\text{C}$, $I_S=4.7\text{A}$, $V_{GS}=0\text{V}$
t_{rr}	Reverse Recovery Time	—	96	200	ns	$T_J=150^\circ\text{C}$, $I_F=5.6\text{A}$, $dI_F/dt=100\text{A}/\mu\text{S}$

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature





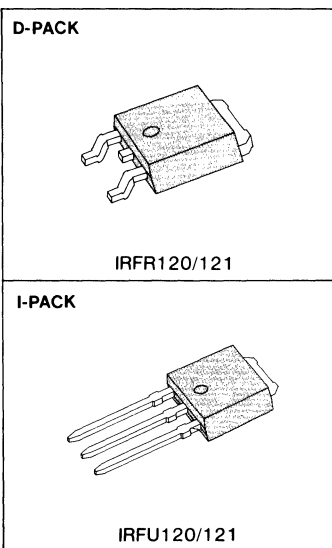


FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFR120/U120	100V	0.27Ω	8.4A
IRFR121/U121	80V	0.27Ω	8.4A



MAXIMUM RATINGS

Characteristic	Symbol	IRFR120/U120	IRFR121/U121	Unit
Drain-Source Voltage (1)	V_{DS}	100	80	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	100	80	Vdc
Gate-Source Voltage	V_{GS}	± 20		Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	8.4		Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	5.9		Adc
Drain Current—Pulsed (3)	I_{DM}	34		Adc
Gate Current—Pulsed	I_{GM}	± 1.5		Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	30		mJ
Avalanche Current	I_{AS}	8.4		A
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	42 0.33		Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300		$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=0.64mH$, $V_{dd}=25V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage IRFR120/U120	100	—	—	V	$V_{GS}=0V$
	IRFR121/U121	80	—	—	V	$I_D=250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}$, $I_D=250\mu A$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS}=20V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	$V_{GS}=-20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS}=\text{Max. Rating}$, $V_{GS}=0V$
		—	—	1000	μA	$V_{DS}=\text{Max. Rating} \times 0.8$, $V_{GS}=0V$, $T_C=125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2)	8.4	—	—	A	$V_{DS}>I_{D(on)} \times R_{DS(on)max}$, $V_{GS}=10V$
$R_{DS(on)}$	Static Drain-Source On-State Resistance (2)	—	0.214	0.27	Ω	$V_{GS}=10V$, $I_D=5.7A$
g_{fs}	Forward Transconductance (2)	2.8	3.3	—	Ω	$V_{DS} \geq 50V$, $I_D=5.9A$
C_{iss}	Input Capacitance	—	416	—	pF	$V_{GS}=0V$, $V_{DS}=25V$, $f=1.0\text{MHz}$
C_{oss}	Output Capacitance	—	111	—	pF	
C_{rss}	Reverse Transfer Capacitance	—	43	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	8.8	13	ns	$V_{DD}=0.5BV_{DSS}$, $I_D=9.2A$, $Z_O=18\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	30	45	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	19	29	ns	
t_f	Fall Time	—	20	30	ns	$V_{GS}=10V$, $I_D=9.2A$, $V_{DS}=0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature.)
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	9.7	15	nC	
Q_{gs}	Gate-Source Charge	—	2.2	3.3	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	2.3	3.4	nC	

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	MAX	3.0	K/W	
R_{thCS}	Case-to-Sink	TYP	1.7	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	MAX	110	K/W	Free Air Operation

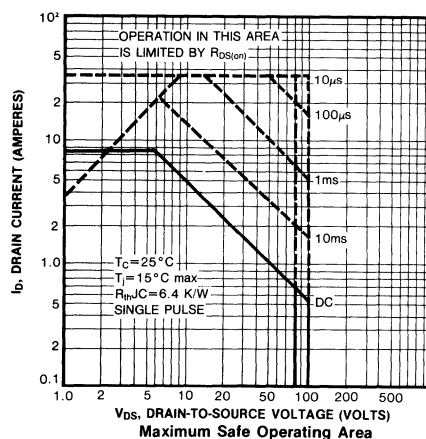
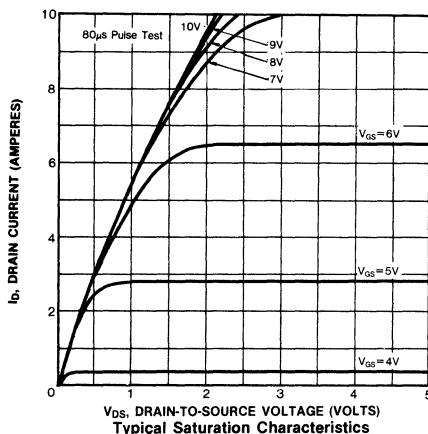
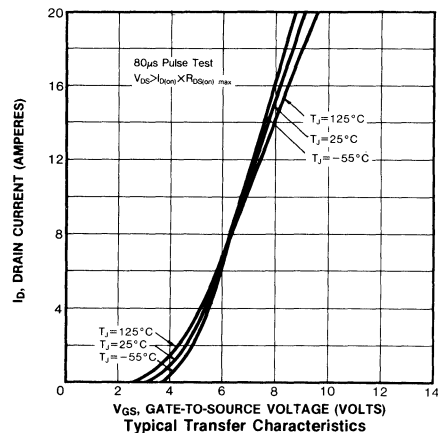
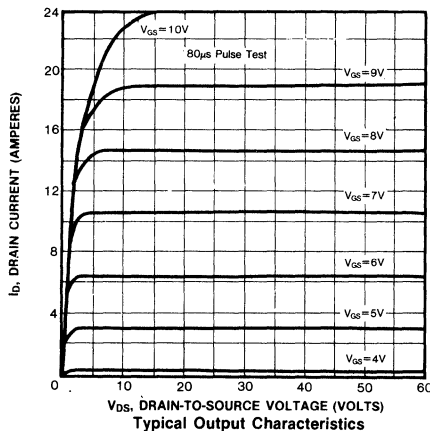
- Notes:** (1) $T_J=25^\circ\text{C}$ to 150°C
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse width limited by max. junction temperature

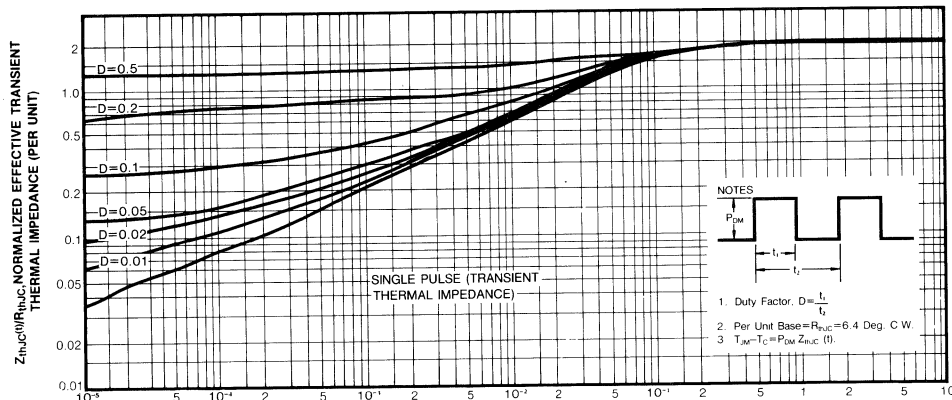
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	8.4	A	Modified MOSFET showing the integral reverse P-N junction rectifier 
I_{SM}	Pulse Source Current(Body Diode)(3)	—	—	34	A	
V_{SD}	Diode Forward Voltage (2)	—	—	2.5	V	$T_C=25^\circ\text{C}$, $I_S=8.4\text{A}$, $V_{GS}=0\text{V}$
t_{rr}	Reverse Recovery Time	—	110	240	ns	$T_J=150^\circ\text{C}$, $I_F=9.2\text{A}$, $dI_F/dt=100\text{A}/\mu\text{S}$

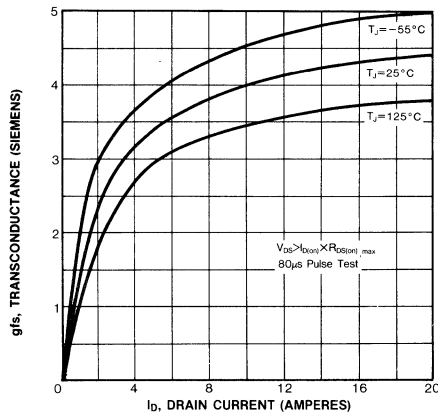
Notes: (1) $T_J=25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature

2

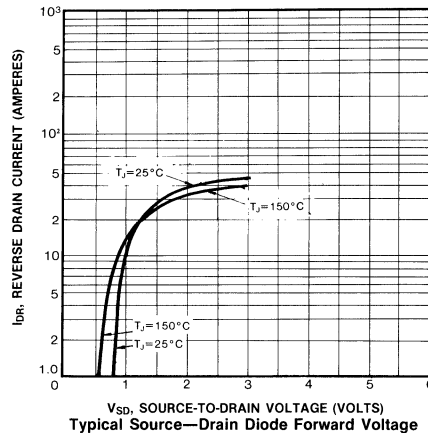




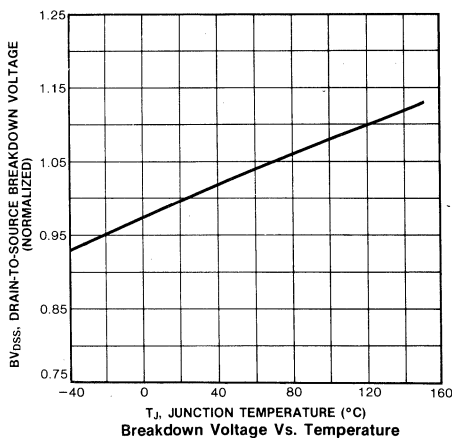
t₁. SQUARE WAVE PULSE DURATION (SECONDS)
Maximum Effective Transient Thermal Impedance Junction-to-Case Vs. Pulse Duration



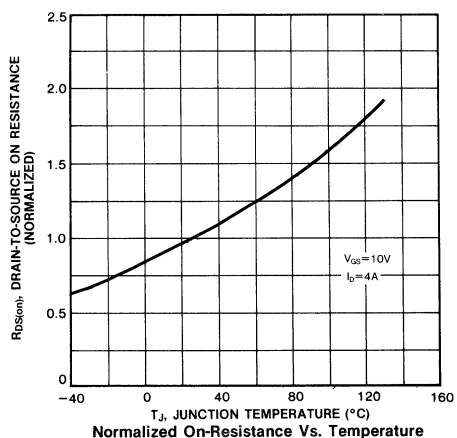
Typical Transconductance Vs. Drain Current



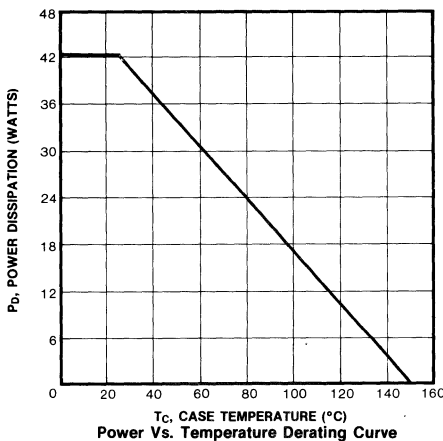
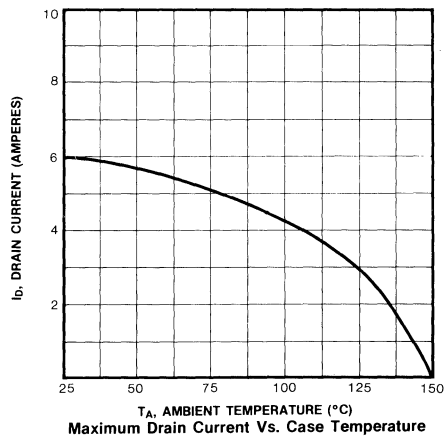
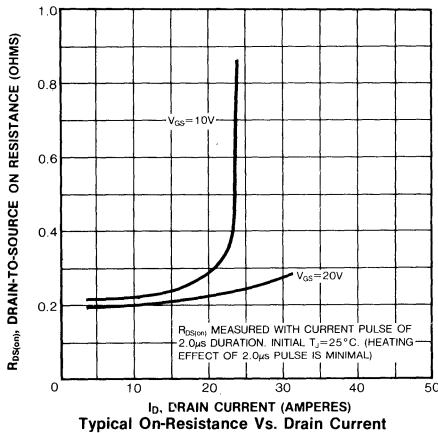
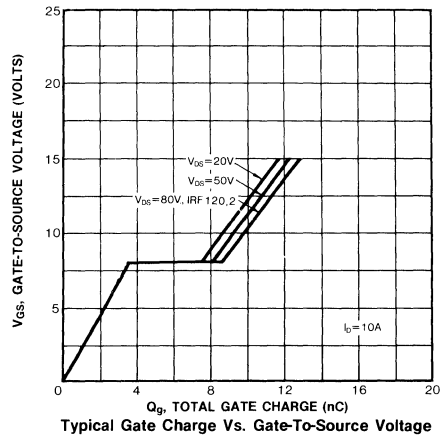
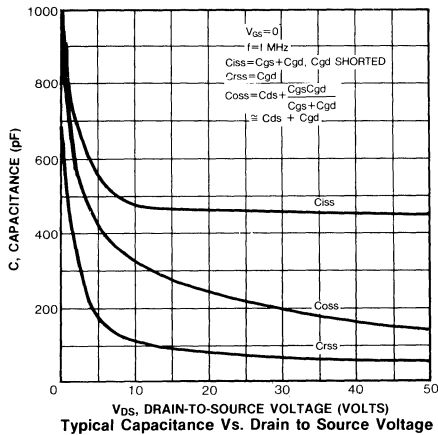
Typical Source-Drain Diode Forward Voltage



Breakdown Voltage Vs. Temperature



Normalized On-Resistance Vs. Temperature



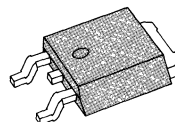
FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

PRODUCT SUMMARY

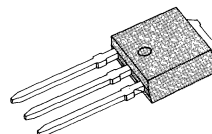
Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFR210/U210	200V	1.5Ω	2.7A
IRFR122/U212	200V	2.4Ω	2.1A

D-PACK



IRFR210/212

I-PACK



IRFU210/212

MAXIMUM RATINGS

Characteristic	Symbol	IRFR210/U210	IRFR212/U212	Unit
Drain-Source Voltage (1)	V_{DSS}	200	200	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	200	200	Vdc
Gate-Source Voltage	V_{GS}	± 20		Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	2.7	2.1	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	1.7	1.3	Adc
Drain Current—Pulsed (3)	I_{DM}	11	8.4	Adc
Gate Current—Pulsed	I_{GM}	± 1.5		Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	31		mJ
Avalanche Current	I_{AS}	2.7		A
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	25 0.20		Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300		$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=0.64mH$, $V_{dd}=50V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage	200	—	—		$V_{GS} = 0V$ $I_D = 250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu A$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS} = 20V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	$V_{GS} = -20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0V$
		—	—	1000	μA	$V_{DS} = \text{Max. Rating} \times 0.8$, $V_{GS} = 0V$, $T_C = 125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2) IRFR210/U210	2.7	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$, $V_{GS} = 10V$
	IRFR212/U212	2.1	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance (2) IRFR210/U210	—	0.91	1.5	Ω	$V_{GS} = 10V$, $I_D = 1.3A$
	IRFR212/U212	—	1.5	2.4	Ω	
g_{fs}	Forward Transconductance (2)	0.83	1.3	—	Ω	$V_{DS} \geq 50V$, $I_D = 1.3A$
C_{iss}	Input Capacitance	—	180	—	pF	$V_{GS} = 0V$, $V_{DS} = 25V$, $f = 1.0MHz$
C_{oss}	Output Capacitance	—	40	—	pF	
C_{rss}	Reverse Transfer Capacitance	—	18	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	8.0	12	ns	$V_{DD} = 0.5BV_{DSS}$, $I_D = 3.2A$, $Z_O = 24\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	20	30	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	17	26	ns	
t_f	Fall Time	—	20	30	ns	$V_{GS} = 10V$, $I_D = 3.2A$, $V_{DS} = 0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature.)
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	11	17	nC	
Q_{gs}	Gate-Source Charge	—	1.3	2.0	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	4.1	6.1	nC	

THERMAL RESISTANCE

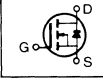
R_{thJC}	Junction-to-Case	MAX	5.0	K/W	
R_{thCS}	Case-to-Sink	TYP	1.7	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	MAX	110	K/W	Free Air Operation

Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C

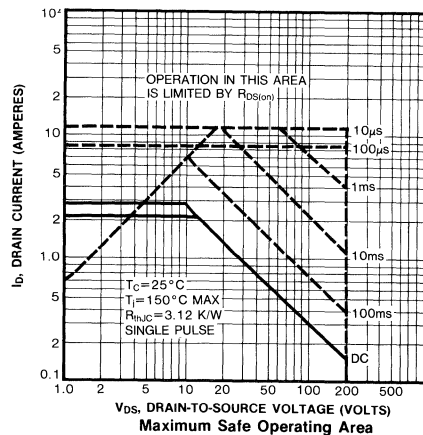
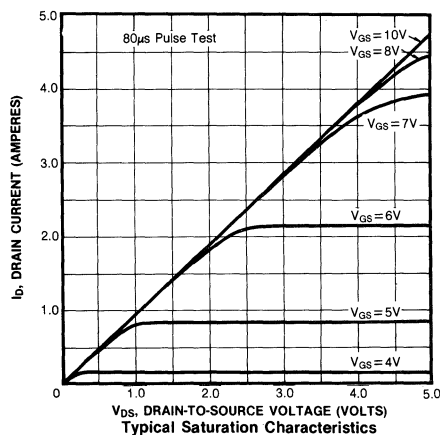
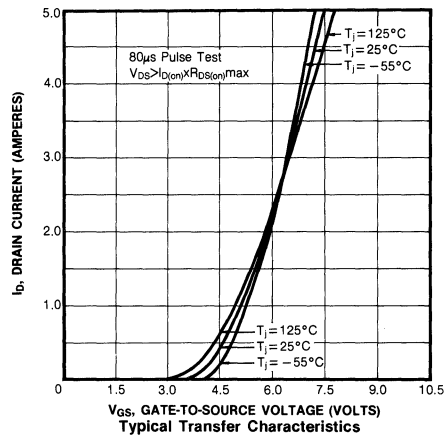
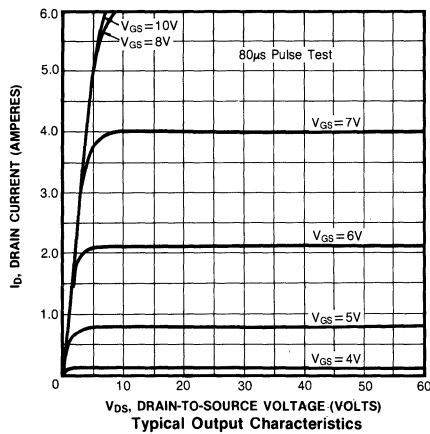
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

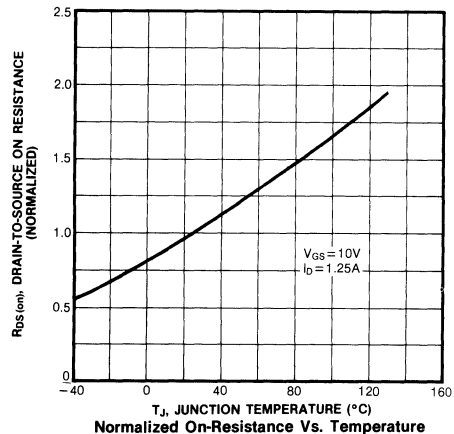
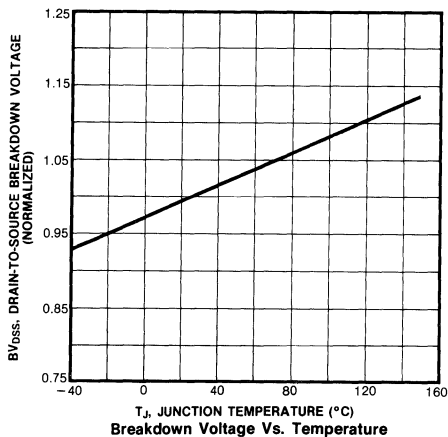
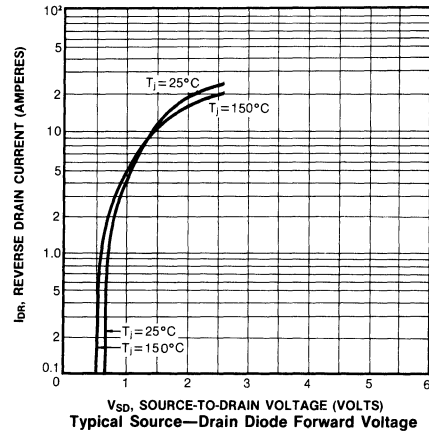
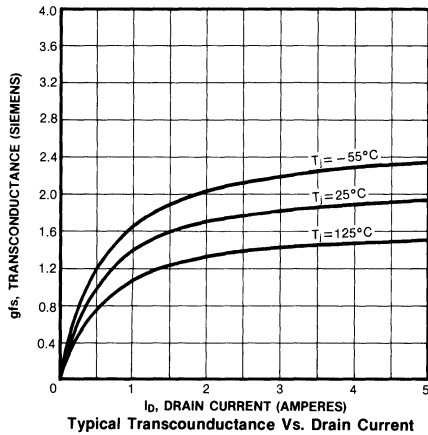
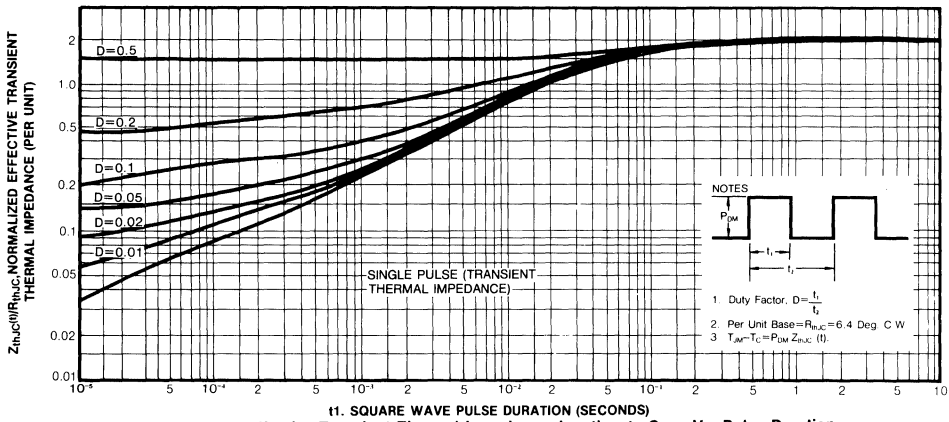
(3) Repetitive rating: Pulse width limited by max. junction temperature

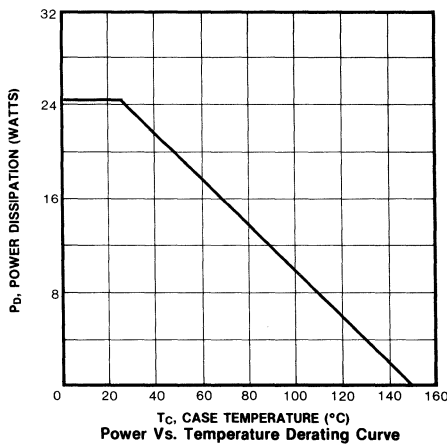
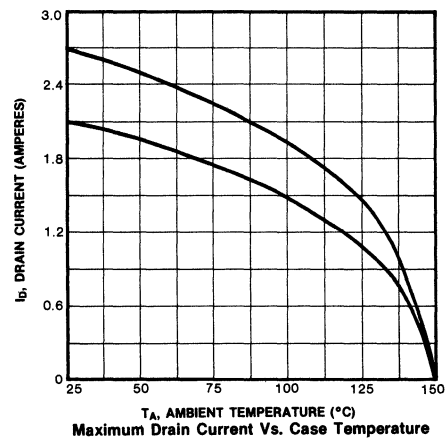
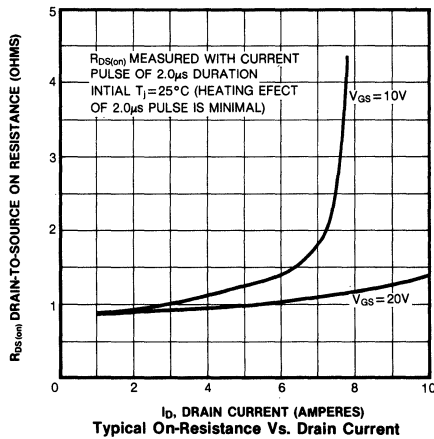
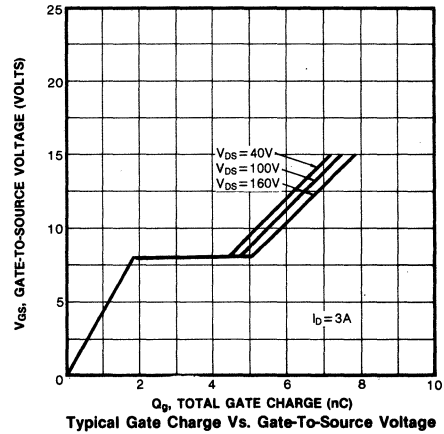
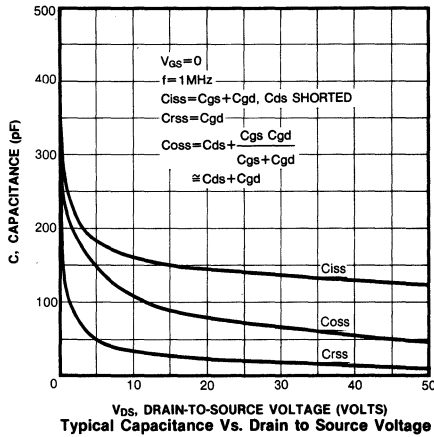
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	2.7	A	Modified MOSFET showing the integral reverse P-N junction rectifier 
I_{SM}	Pulse Source Current(Body Diode)(3)	—	—	11	A	
V_{SD}	Diode Forward Voltage (2)	—	—	2.0	V	$T_C=25^\circ\text{C}$, $I_S=2.7\text{A}$, $V_{GS}=0\text{V}$
t_{rr}	Reverse Recovery Time	—	170	400	ns	$T_J=150^\circ\text{C}$, $I_F=3.2\text{A}$, $dI_F/dt=100\text{A}/\mu\text{S}$

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature





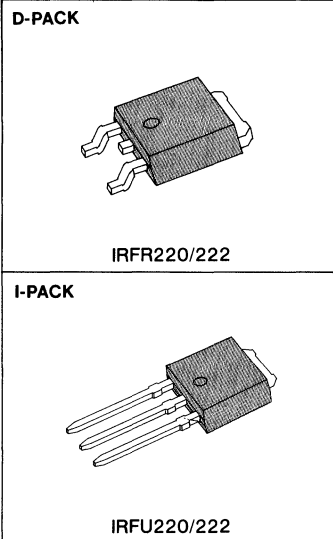


FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFR220/U220	200V	0.80Ω	4.6A
IRFR222/U222	200V	1.2Ω	3.8A



MAXIMUM RATINGS

Characteristic	Symbol	IRFR220/U220	IRFR222/U222	Unit
Drain-Source Voltage (1)	V _{DSS}	200		V _{dc}
Drain-Gate Voltage (R _{GS} =1.0MΩ)(1)	V _{DGR}	200		V _{dc}
Gate-Source Voltage	V _{GS}	±20		V _{dc}
Continuous Drain Current T _C =25 °C	I _D	4.6	3.8	A _{dc}
Continuous Drain Current T _C =100 °C	I _D	2.9	2.4	A _{dc}
Drain Current—Pulsed (3)	I _{DM}	18	15	A _{dc}
Gate Current—Pulsed	I _{GM}	±1.5		A _{dc}
Single Pulsed Avalanche Energy (4)	E _{AS}	50		mJ
Avalanche Current	I _{AS}	4.6		A
Total Power Dissipation @ T _C =25 °C	P _D	42		Watts W/°C
Derate above 25 °C		0.33		
Operating and Storage Junction Temperature Range	T _J , T _{stg}	−55 to 150		°C
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T _L	300		°C

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=4.5mH$, $V_{dd}=50V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage	200	—	—		$V_{GS}=0V$ $I_D=250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}$, $I_D=250\mu A$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS}=20V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	$V_{GS}=-20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS}=\text{Max. Rating}$, $V_{GS}=0V$
		—	—	1000	μA	$V_{DS}=\text{Max. Rating} \times 0.8$, $V_{GS}=0V$, $T_C=125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2) IRFR220/U220	4.6	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$, $V_{GS}=10V$
	IRFR222/U222	3.8	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance (2) IRFR220/U220	—	—	0.8	Ω	$V_{GS}=10V$, $I_D=2.4A$
	IRFR222/U222	—	—	1.2	Ω	
g_{fs}	Forward Transconductance (2)	1.7	2.6	—	Ω	$V_{DS} \geq 50V$, $I_D=2.4A$
C_{iss}	Input Capacitance	—	400	—	pF	$V_{GS}=0V$, $V_{DS}=25V$, $f=1.0MHz$
C_{oss}	Output Capacitance	—	82	—	pF	
C_{rss}	Reverse Transfer Capacitance	—	32	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	8.8	13	ns	$V_{DD}=0.5BV_{DSS}$, $I_D=5.1A$, $Z_O=18\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	27	41	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	21	32	ns	
t_f	Fall Time	—	14	21	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	12	18	nC	$V_{GS}=10V$, $I_D=5.1A$, $V_{DS}=0.8$ Max. Rating (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	2.3	3.4	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	4.5	6.8	nC	

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	MAX	3.0	K/W	
R_{thCS}	Case-to-Sink	TYP	1.7	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	MAX	110	K/W	Free Air Operation

Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

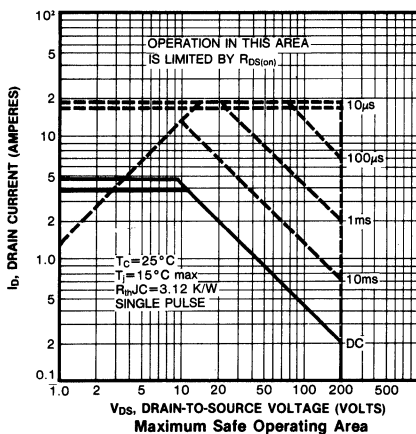
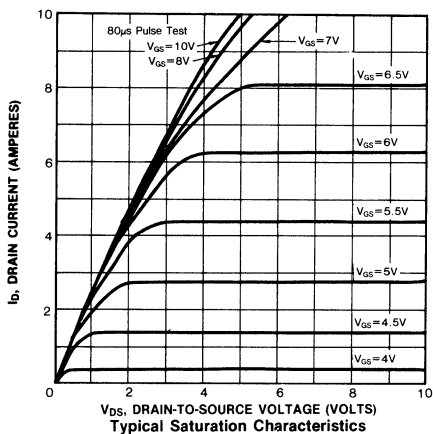
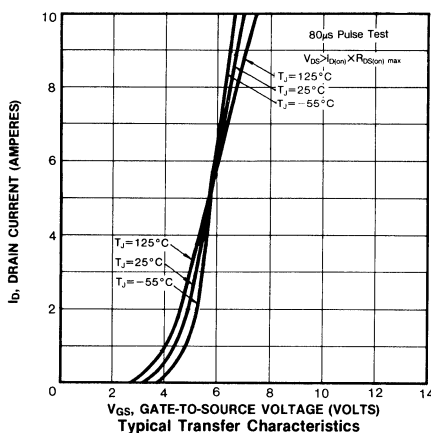
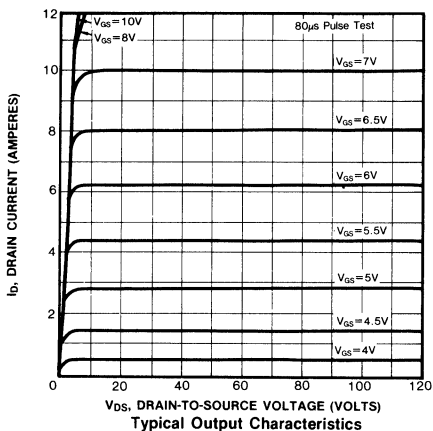
(3) Repetitive rating: Pulse width limited by max. junction temperature

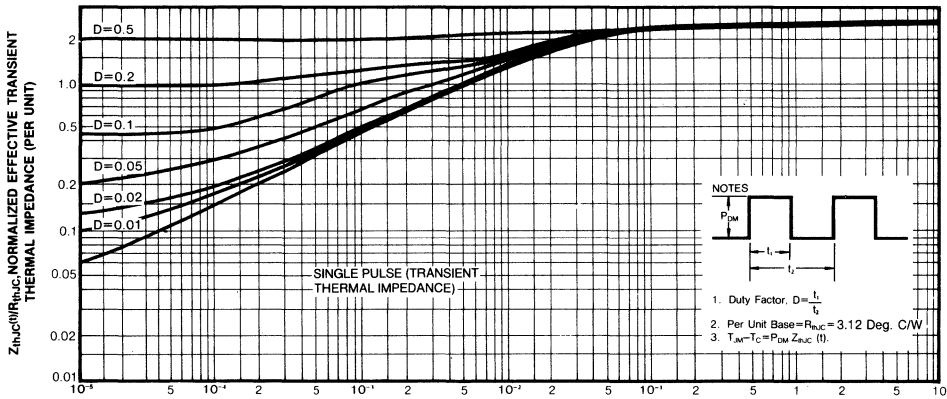
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	4.6	A	Modified MOSFET showing the integral reverse P-N junction rectifier
I_{SM}	Pulse Source Current(Body Diode)(3)	—	—	18	A	
V_{SD}	Diode Forward Voltage (2)	—	—	1.8	V	$T_C = 25^\circ\text{C}$, $I_S = 4.6\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	170	400	ns	$T_J = 150^\circ\text{C}$, $I_F = 5.1\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$

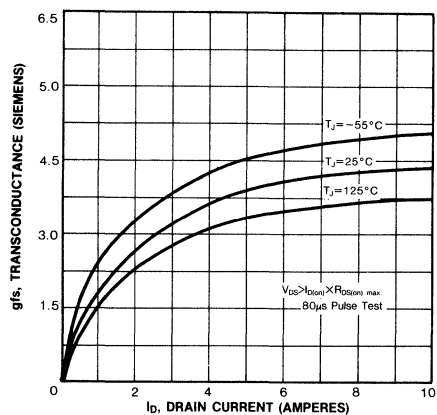
Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature

2

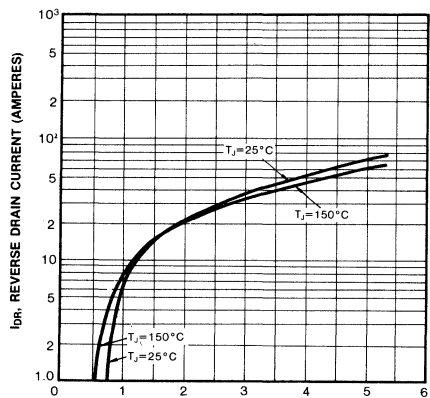




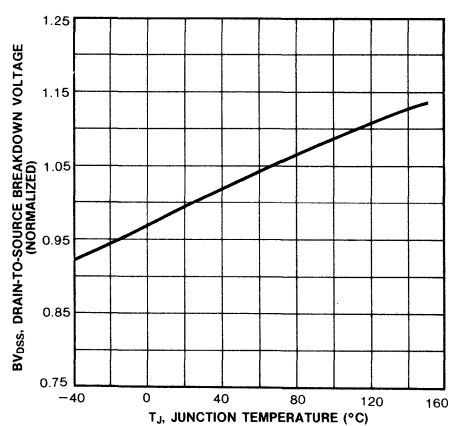
11. SQUARE WAVE PULSE DURATION (SECONDS)
Maximum Effective Transient Thermal Impedance Junction-to-Case Vs. Pulse Duration



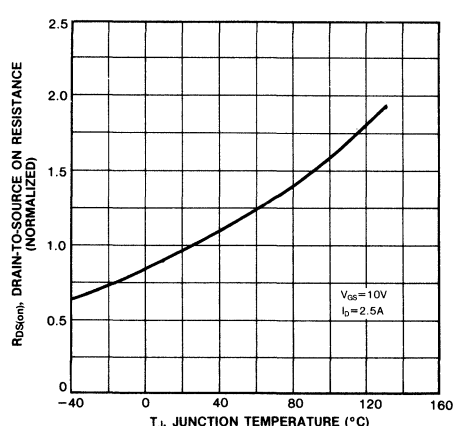
Typical Transconductance Vs. Drain Current



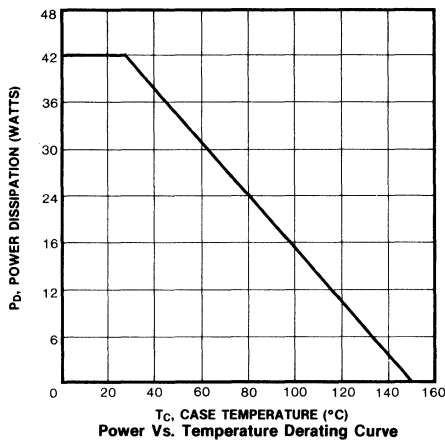
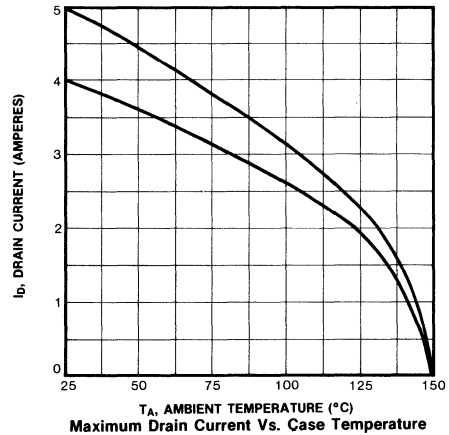
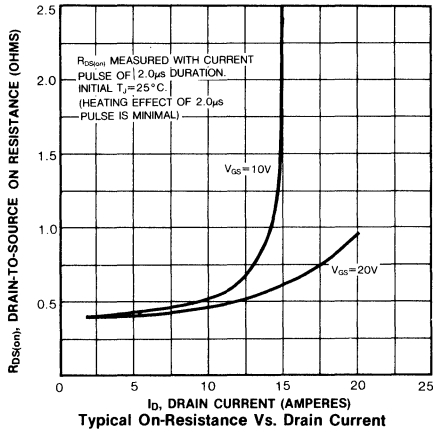
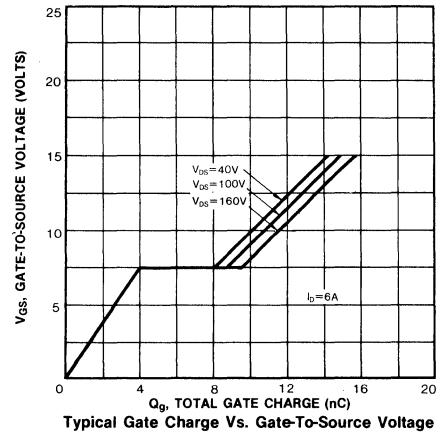
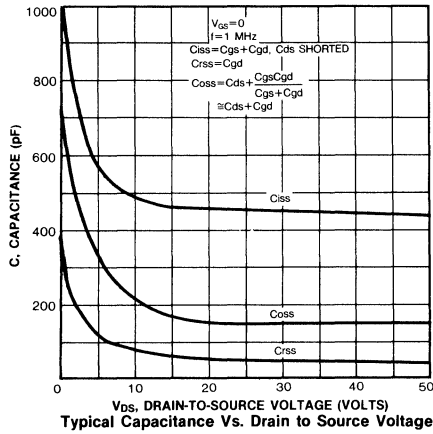
Typical Source-Drain Diode Forward Voltage



Breakdown Voltage Vs. Temperature



Normalized On-Resistance Vs. Temperature



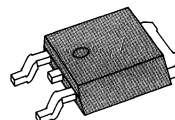
FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching time
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

PRODUCT SUMMARY

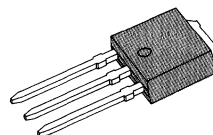
Part Number	V_{DS}	$R_{DS(on)}$	$I_{D(on)}$
IRFR310/U310	400V	3.6Ω	1.5A
IRFR312/U312	400V	5.0Ω	1.0A

D-PACK



IRFR310/312

I-PACK



IRFU310/312

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	IRFR310/U310	IRFR312/U312	Units
Drain-Source Voltage (1)	V_{DSS}	400		Vdc
Drain-Gate Voltage ($R_{GS} = 1.0M\Omega$) (1)	V_{DGR}	400		Vdc
Gate-Source Voltage	V_{GS}	± 20		Vdc
Continuous Drain Current $T_C = 25^\circ C$	I_D	1.5	1.0	Adc
Continuous Drain Current $T_C = 100^\circ C$	I_D	0.9	0.6	Adc
Drain Current — Pulsed (3)	I_{DM}	3.5	3.0	Adc
Gate Current — Pulsed	I_{GM}	± 1.5		Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	60		mj
Avalanche Current	I_{AS}	1.5		A
Total Power Dissipation at $T_C = 25^\circ C$ Derate above $25^\circ C$	P_D	25 0.20		Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	- 55 to $150^\circ C$		$^\circ C$
Maximum Lead Temp, for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300		$^\circ C$

Notes: (1) $T_J = 25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse width limited by max. junction temperature

(4) $L = 53 mH$, $V_{DD} = 50V$, $R_G = 25\Omega$, Starting $T_J = 25^\circ C$

ELECTRICAL CHARACTERISTIC ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage	400	—	—	V	$V_{GS} = 0V$ $I_D = 250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu A$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS} = 20V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	$V_{GS} = 20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS} = \text{Max. Rating}$ $V_{GS} = 0V$
$I_{D(on)}$	On-State Drain Source Current (2) IRFR310/U310	1.5	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max. $V_{GS} = 10V$
	IRFU312/U312	1.0	—	—		
$R_{DS(on)}$	Static Drain-Source On-State Resistance IRFR310/U310	—	3.3	3.6	Ω	$V_{GS} = 10V$, $I_D = 0.8A$
	IRFR312/U312	—	3.6	5.0	Ω	
g_{fs}	Forward Transconductance (2)	0.5	1.0	—	S	$V_{DS} > R_{DS} \times I_{D(on)}$, $I_D = 0.8A$
C_{iss}	Input Capacitance	—	180	—	pF	$V_{GS} = 0V$, $V_{DS} = 25V$, $f = 10\text{MHz}$
C_{oss}	Output Capacitance	—	40	—	pF	
C_{rss}	Reverse Transfer Capacitance	—	14	—	pF	
$t_d(on)$	Turn-On Delay Time	—	7.9	12	ns	$V_{DD} = 0.5 BV_{DSS}$, $I_D = 1.5A$, $Z_O = 24\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	9.9	15	ns	
$t_d(off)$	Turn-Off Delay Time	—	21	32	ns	
t_f	Fall Time	—	11	17	ns	$V_{GS} = 10V$, $I_D = 1.5A$ $V_{DS} = 0.8$ Max. Rating (Gate charge is essentially independent of operating temperature)
Q_g	Total Gate Charge (Gate-Source Pulse Gate-Drain)	—	7.7	12	nC	
Q_{gs}	Gate-Source Charge	—	1.2	1.9	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	4.0	5.9	nC	

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	MAX	5.0	K/W	
R_{thCS}	Case-to-Sink	TYP	1.7	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	MAX	110	K/W	Free Air Operation

Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C

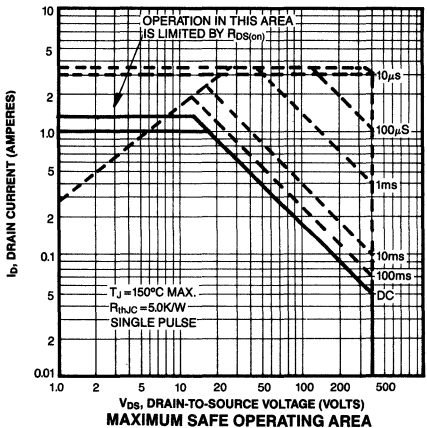
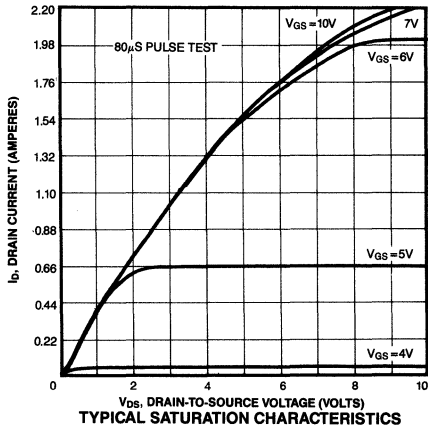
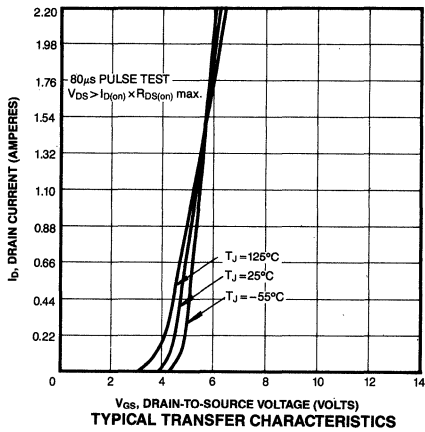
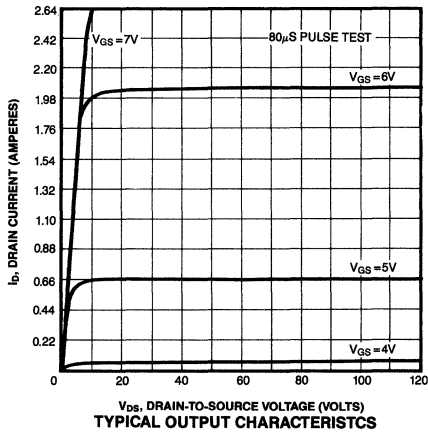
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

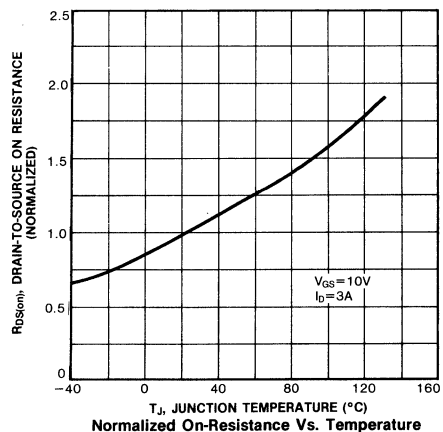
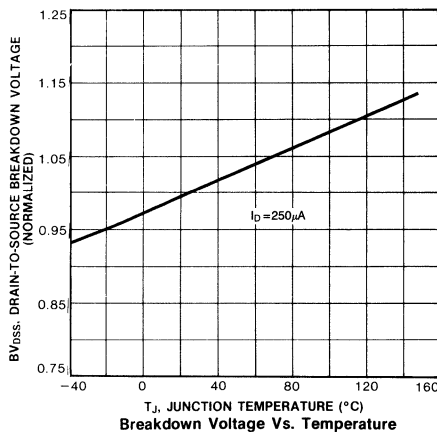
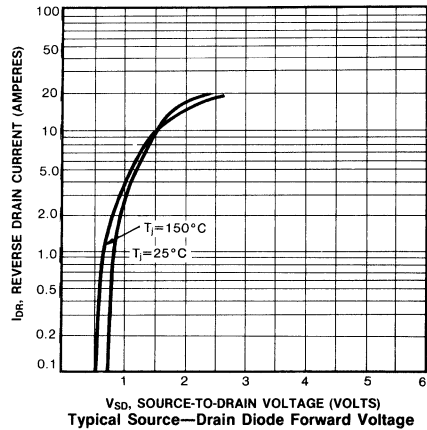
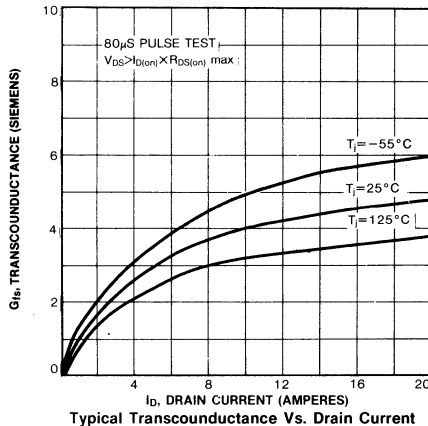
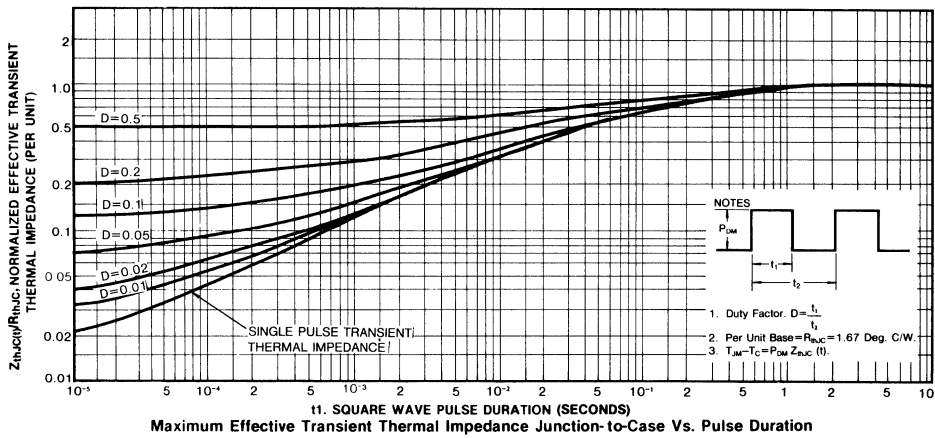
(3) Repetitive rating: Pulse width limited by max. junction temperature

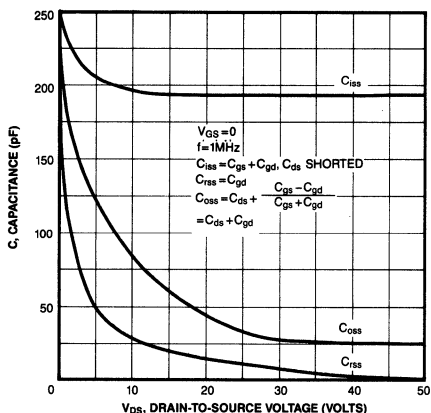
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
I_S	Continuous Source Current (Body Diode)	—	—	1.5	A	Modified MOSFET -integral reverse P-N junction rectifier
I_{SM}	Pulse-Source Current (3)	—	—	3.5	A	
V_{DS}	Diode Forward Voltage (2)	—	—	1.6	V	$T_C = 25^\circ\text{C}$, $I_S = 1.5\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery time	—	240	520	ns	$T_J = 25^\circ\text{C}$, $I_F = 1.5\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{s}$

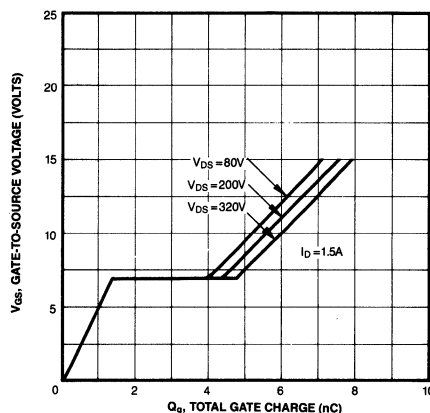
Notes: (1) $T_J = 25^\circ\text{C}$, to 150°C
(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature



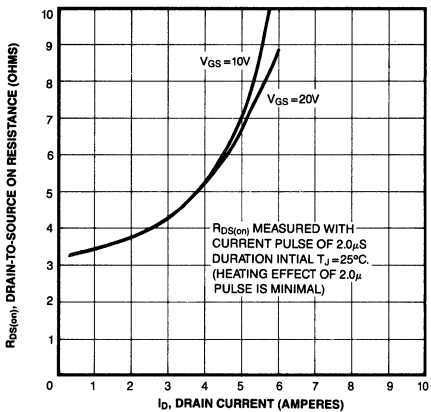




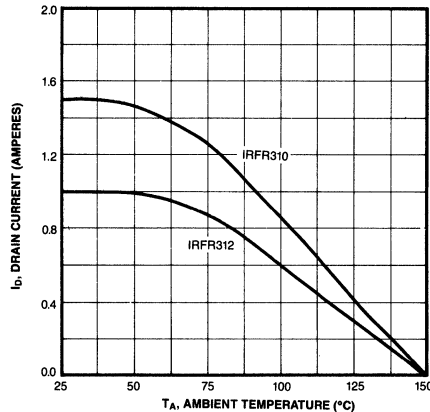
TYPICAL CAPACITANCE V_S. DRAIN TO SOURCE VOLTAGE



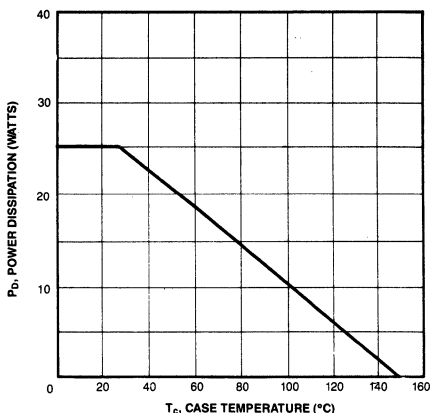
TYPICAL GATE CHARGE V_S. GATE-TO-SOURCE VOLTAGE



TYPICAL ON-RESISTANCE V_S. DRAIN CURRENT



MAXIMUM DRAIN CURRENT V_S. CASE TEMPERATURE



POWER V_S. TEMPERATURE DERATING CURVE.

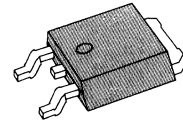
FEATURE

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching time
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

PRODUCT SUMMARY

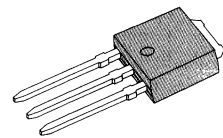
Part Number	V_{DS}	$R_{DS(on)}$	$I_{D(on)}$
IRFR320/U320	400V	1.8 Ω	2.7A
IRFR322/U322	400V	2.5 Ω	2.3A

D-PACK



IRFR320/322

I-PACK



IRFU320/322

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	IRFR320/U320	IRFR322/U322	Units
Drain-Source Voltage (1)	V_{DSS}	400		Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$) (1)	V_{DGR}	400		Vdc
Gate-Source Voltage	V_{GS}	± 20		Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	2.7	2.3	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	1.8	1.5	Adc
Drain Current — Pulsed (3)	I_{DM}	11.0	9.0	Adc
Gate Current — Pulsed	I_{GM}	± 1.5		Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	16		mJ
Avalanche Current	I_{AS}	2.7		A
Total Power Dissipation at $T_C=25^\circ C$	P_D	42		Watts
Derate above $25^\circ C$		0.33		W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ C$
Maximum Lead Temp, for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300		$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse width limited by max. junction temperature

(4) $L=4.5mH$, $V_{dd}=50V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTIC ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage	400	—	—	V	$V_{GS} = 0V$ $I_D = 250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu A$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS} = 20V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	- 100	nA	$V_{GS} = 20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0V$
$I_{D(on)}$	On-State Drain Source Current (2) IRFR320/U320	2.7	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max. $V_{GS} = 10V$
	IRFU322/U322	2.3	—	—		
$R_{DS(on)}$	Static Drain-Source On-State Resistance IRFR320/U320	—	—	1.8	Ω	$V_{GS} = 10V$, $I_D = 1.4A$
	IRFR322/U322	—	—	2.5		
g_{fs}	Forward Transconductance (2)	1.0	2.0	—	S	$V_{DS} > R_{DS} \times I_{D(on)}$, $I_D = 1.4A$
C_{iss}	Input Capacitance	—	400	—	pF	$V_{GS} = 0V$, $V_{DS} = 25V$, $f = 10MHz$
C_{oss}	Output Capacitance	—	59	—	pF	
C_{rss}	Reverse Transfer Capacitance	—	27	—	pF	
$t_d(on)$	Turn-On Delay Time	—	10	15	ns	$V_{DD} = 0.5 BV_{DSS}$, $I_D = 2.7A$, $Z_\theta = 18\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	14	20	ns	
$t_d(off)$	Turn-Off Delay Time	—	30	45	ns	
t_f	Fall Time	—	13	20	ns	
Q_g	Total Gate Charge (Gate-Source Pulse Gate-Drain)	—	12	15	nC	$V_{GS} = 10V$, $I_D = 2.7A$, $V_{DS} = 0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature)
Q_{gs}	Gate-Source Charge	—	2.8	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	9.7	—	nC	

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	MAX	3.0	K/W	
R_{thCS}	Case-to-Sink	TYP	1.7	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	MAX	110	K/W	Free Air Operation

Notes: (1) $T_J = 25^\circ$ to 150°

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse width limited by max. junction temperature

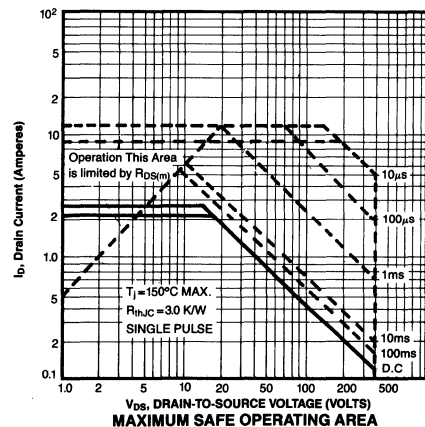
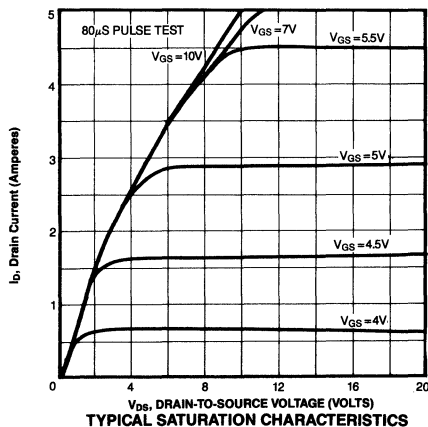
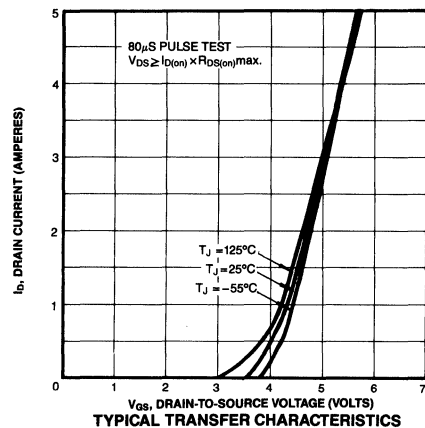
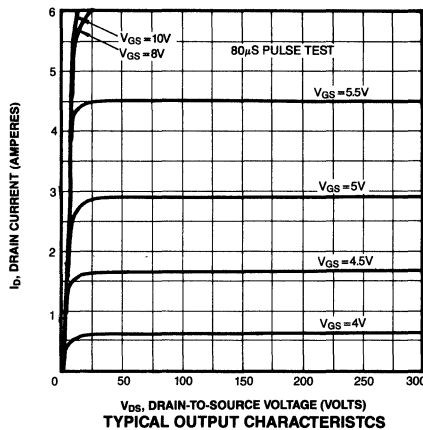
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

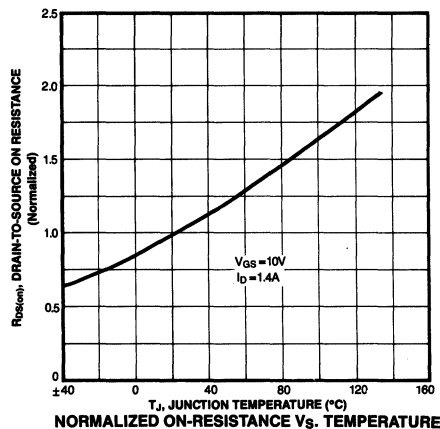
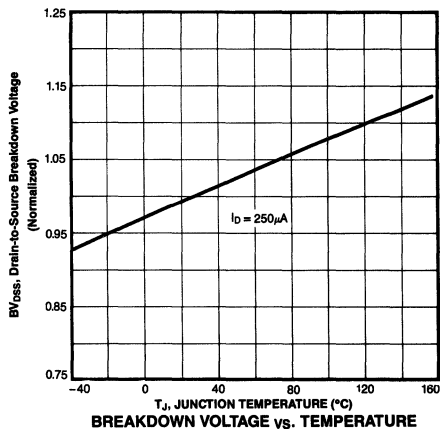
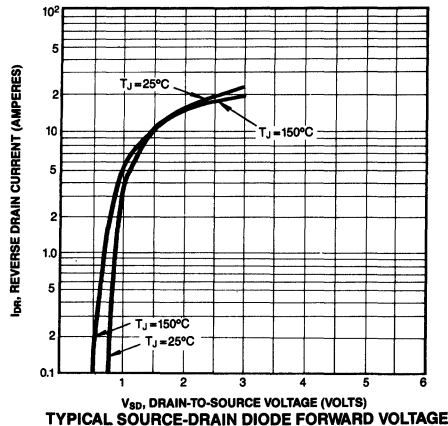
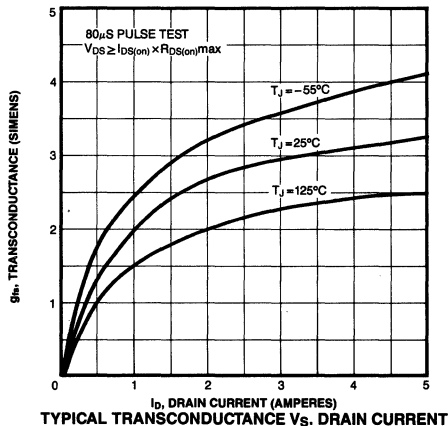
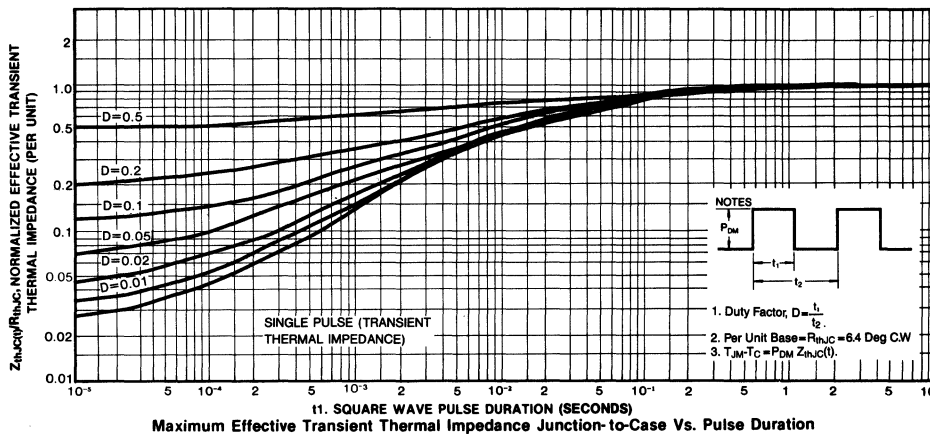
Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
I_S	Continuous Source Current (Body Diode)	—	—	2.7	A	Modified MOSFET integral reverse P-N junction rectifier
I_{SM}	Pulse-Source Current (3)	—	—	11	A	
V_{DS}	Diode Forward Voltage (2)	—	—	1.8	V	$T_c = 25^\circ\text{C}$, $I_S = 2.7\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery time	—	270	—	ns	$T_j = 25^\circ\text{C}$, $I_F = 2.7\text{A}$, $dI/dt = 100\text{A}/\mu\text{s}$

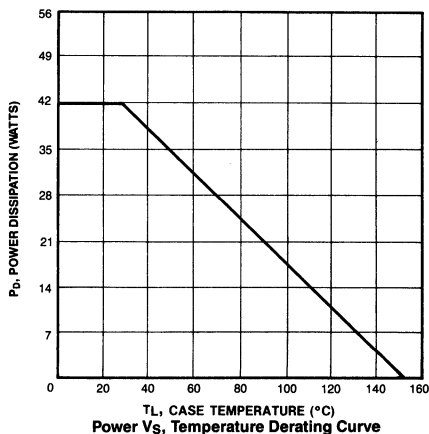
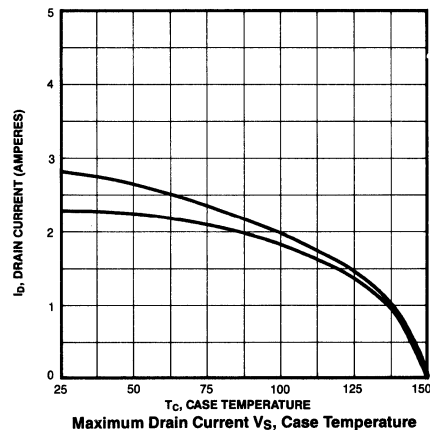
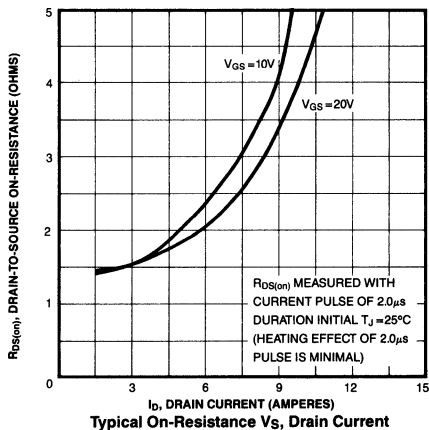
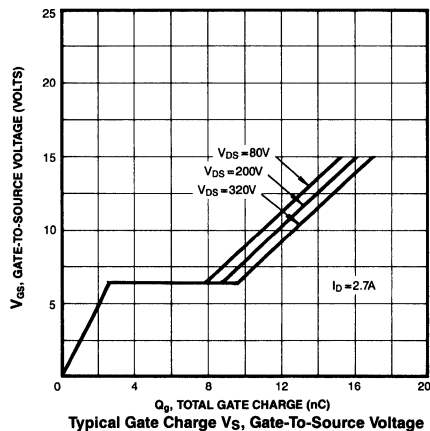
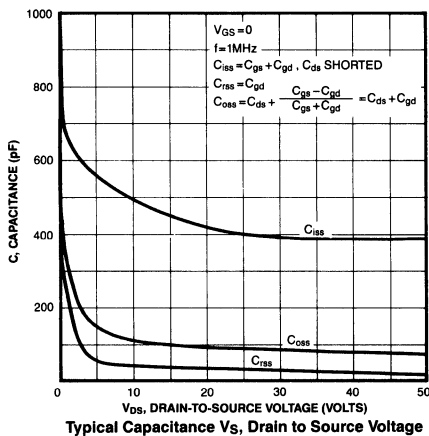
Notes: (1) $T_j = 25^\circ\text{C}$ to 150°C

(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature







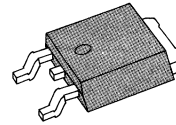
FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

PRODUCT SUMMARY

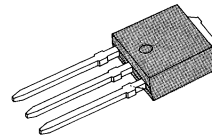
Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFR420/U420	500V	3.0Ω	2.5A
IRFR422/U422	500V	4.0Ω	2.2A

D-PACK



IRFR420/421

I-PACK



IRFU420/422

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	IRFR420/U420	IRFR422/U422	Unit
Drain-Source Voltage (1)	V_{DS}	500	500	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$) (1)	V_{DGR}	500	500	Vdc
Gate-Source Voltage	V_{GS}	± 20		Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	2.5	2.2	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	1.6	1.4	Adc
Drain Current—Pulsed (3)	I_{DM}	8.0	7.0	Adc
Gate Current—Pulsed	I_{GM}	± 1.5		Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	210		mJ
Avalanche Current	I_{AS}	2.5		A
Total Power Dissipation at $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	42 0.33		Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300		$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=60mH$, $V_{dd}=50V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Unit	Test Conditions
BV _{DSS}	Drain-Source Breakdown Voltage IRFR420/422	500	—	—	V	V _{GS} =0V, I _D =250μA
	IRFU420/422	500	—	—	V	
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} =V _{GS} , I _D =250μA
I _{GSS}	Gate-Source Leakage Forward	—	—	100	nA	V _{GS} =20V
I _{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	V _{GS} =-20V
I _{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	V _{DS} =Max. Rating×0.8, V _{GS} =0V
		—	—	1000	μA	V _{DS} =Max. Rating×0.8, T _C =125°C
I _{D(on)}	On-State Drain-Source Current (2) IRFR520/U420	2.5	—	—	A	V _{DS} ≥10V
	IRFR422/U422	2.0	—	—	A	V _{GS} =10V
R _{DS(on)}	Static Drain-Source On-State Resistance (2) IRFR420/U420	—	2.5	3.0	Ω	V _{GS} =10V, I _D =1.0A
	IRFR422/U422	—	3.0	4.0	Ω	
g _{fs}	Forward Transconductance (2)	1.4	2.3	—	U	V _{DS} ≥50V, I _D =1.0A
C _{iss}	Input Capacitance	—	390	—	pF	V _{GS} =0V
C _{oss}	Output Capacitance	—	52	—	pF	V _{DS} =25V
C _{rss}	Reverse Transfer Capacitance	—	22	—	pF	f=1.0MHz
t _{d(on)}	Turn-On Delay Time	—	10	15	ns	V _{DD} =0.5BV _{DSS} , I _D =2.5A Z _o =18Ω (MOSFET switching times are essentially independent of operating temperature)
t _r	Rise Time	—	12	18	ns	
t _{d(off)}	Turn-Off Delay Time	—	28	42	ns	
t _f	Fall Time	—	12	18	ns	
Q _g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	13	19	nC	V _{GS} =10V, I _D =2.5, V _{DS} =0.8 Max. Rating (Gate charge is essentially independent of operating temperature)
Q _{gs}	Gate-Source Charge	—	2.2	3.3	nC	
Q _{gd}	Gate-Drain ("Miller") Charge	—	6.8	10	nC	

THERMAL RESISTANCE

R _{thJC}	Junction-to-Case	MAX	3.0	K/W	
R _{thCS}	Case-to-Sink	TYP	1.7	K/W	Mounting surface flat, Smooth, and greased
R _{thJA}	Junction-to-Ambient	MAX	110	K/W	Free Air Operation

Notes: (1) T_J=25°C to 150°C

(2) Pulse test: Pulse width≤300μs, Duty Cycle≤2%

(3) Repetitive rating: Pulse width limited by max. junction temperature

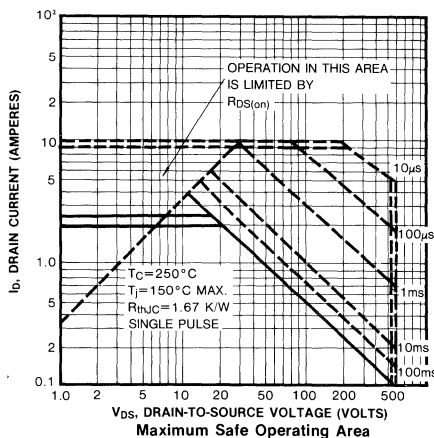
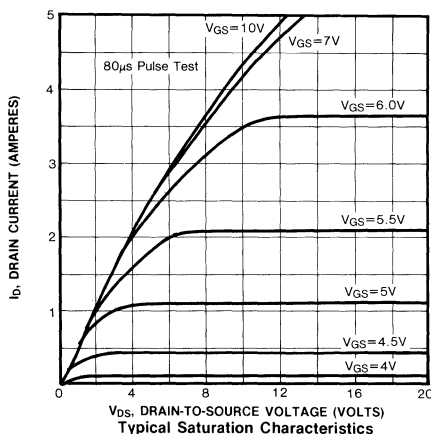
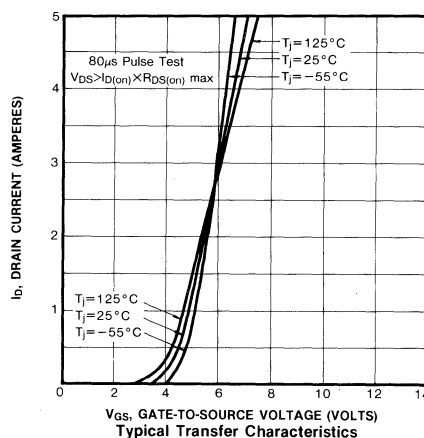
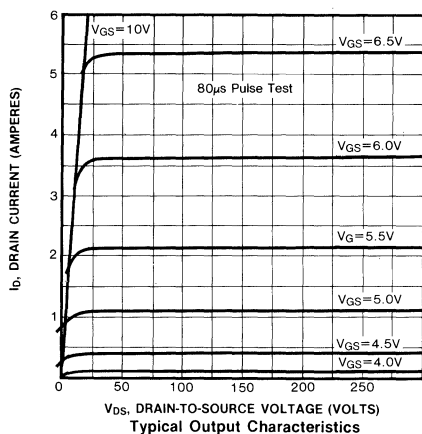
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

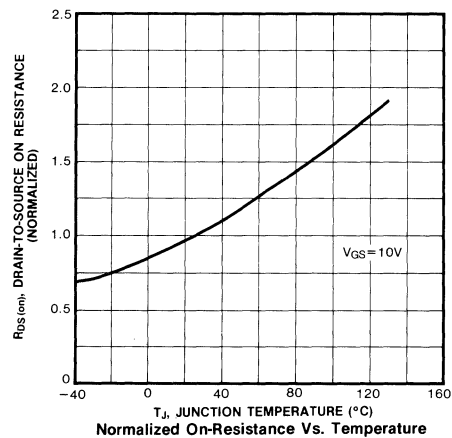
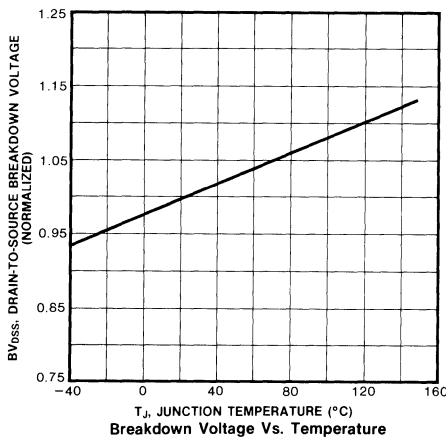
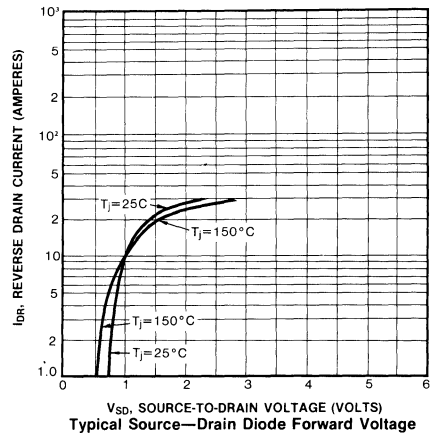
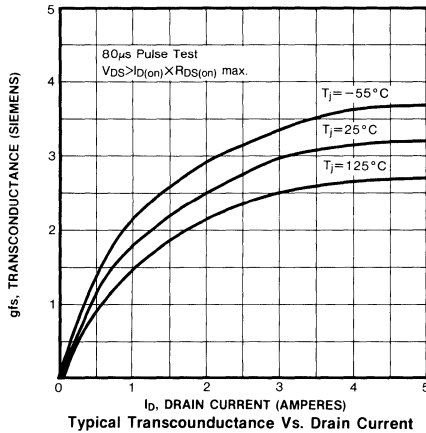
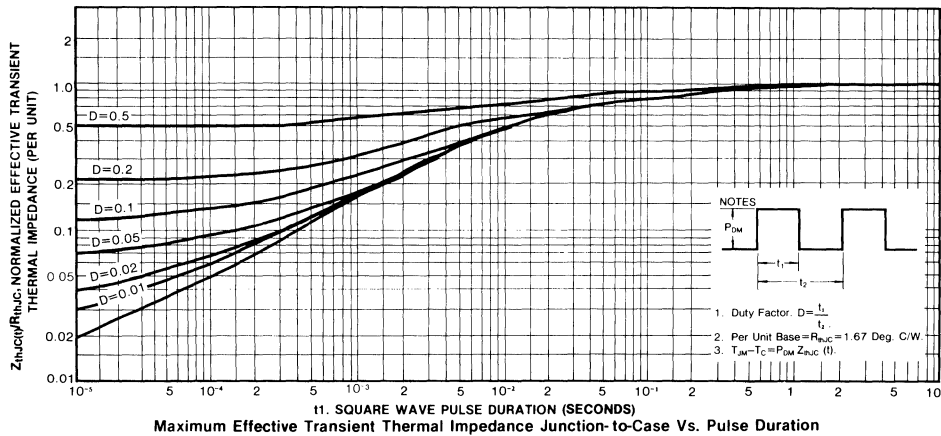
Symbol	Characteristic	Min	Typ	Max	Unit	Test Conditions
I_S	Continuous Source Current IRFR420/U420 (Body Diode) IRFR422/U422	—	—	2.5 2.2	A A	Modified MOSFET symbol showing integral reverse P-N junction rectifier
I_{SM}	Pulse Source Current (3) IRFR420/U420 IRFR422/U422	—	—	8.0 7.0	A A	
V_{DS}	Diode Forward Voltage (2) IRFR420/U420 IRFR422/U422	—	—	1.6 1.5	V V	$T_C=25^\circ\text{C}$, $I_S=2.5\text{A}$, $V_{GS}=0\text{V}$ $T_C=25^\circ\text{C}$, $I_S=2.2\text{A}$, $V_{GS}=0\text{V}$
t_{rr}	Reverse Recovery Time	—	270	540	ns	$T_J=25^\circ\text{C}$, $I_F=2.5\text{A}$, $dI_F/dt=100\text{A}/\mu\text{S}$

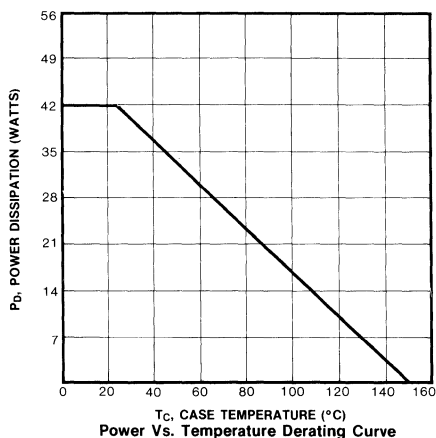
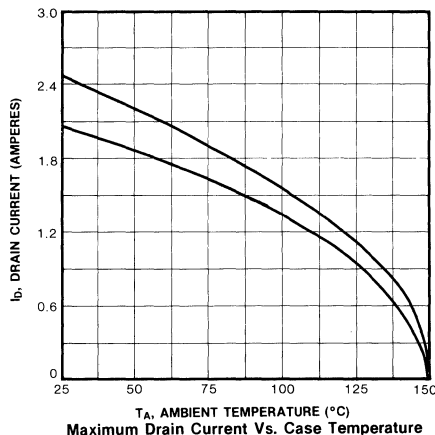
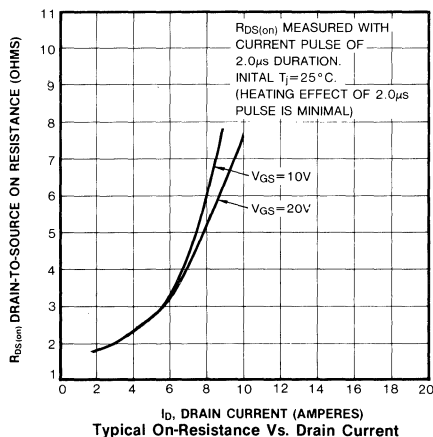
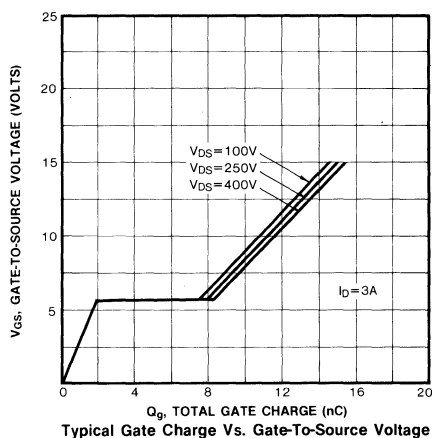
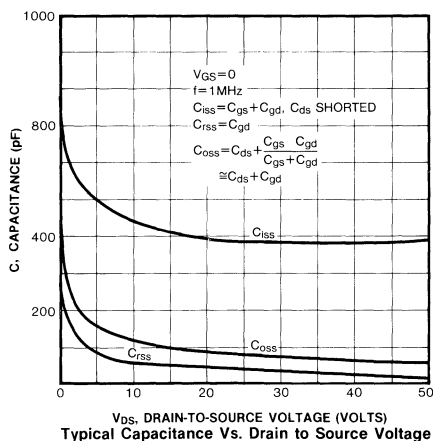
Notes: (1) $T_J=25^\circ\text{C}$ to 150°C

(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature





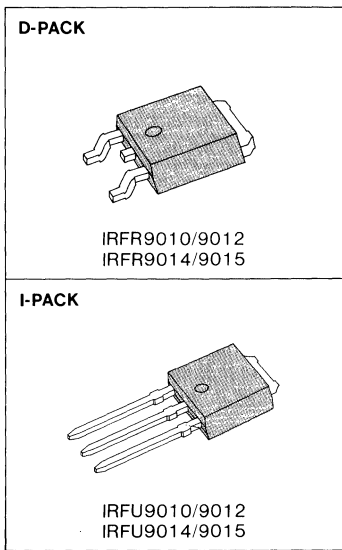


FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFR9010/U9010	-50V	0.50 Ω	-5.3A
IRFR9012/U9012	-50V	0.70 Ω	-4.5A
IRFR9014/U9014	-60V	0.50 Ω	-5.3A
IRFR9015/U9015	-60V	0.70 Ω	-4.5A



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	IRFR9010 IRFU9010	IRFR9012 IRFU9012	IRFR9014 IRFU9014	IRFR9015 IRFU9015	Unit
Drain-Source Voltage (1)	V_{DSS}	-50		-60V		Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	-50		-60		Vdc
Gate-Source Voltage	V_{GS}	± 20				Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	-5.3	-4.5	-5.3	-4.5	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	-3.3	-2.8	-3.3	-2.8	Adc
Drain Current—Pulsed (3)	I_{DM}	-21	-18	-21	-18	Adc
Gate Current—Pulsed	I_{GM}	± 1.5				Adc
Single Pulsed Aualanche Energy (4)	E_{AS}	240				mj
Avalanche Current	I_{AS}	-5.3				A
Total Power Dissipation at $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	25 0.20				Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150				$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300				$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature
(4) $L=9.7mH$, $V_{dd}=-25V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV_{DS}	Drain-Source Breakdown Voltage IRFR9014/9015, IRFU9014/9015 IRFR9010/9012, IRFU9010/9012	-60	—	—	V	$V_{GS}=0V$, $I_D = -250\mu A$
		-50	—	—	V	
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	$V_{DS}=V_{GS}$, $I_D = -250\mu A$
I_{GSS}	Gate-Source Leakage Forward	—	—	-500	nA	$V_{GS} = -20V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	500	nA	$V_{GS} = 20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0V$ $V_{DS} = 0.8 \text{ Max Rating}$, $V_{GS} = 20V$, $T_J = 125^\circ\text{C}$
		—	—	1000		
$I_{D(on)}$	On-State Drain-Source Current (2) IRFR9010/9014, IRFU9010/9014 IRFR9010/9015, IRFU9012/9015	—	—	—	—	$V_{DS} \leq -3.7V$, $V_{GS} = -10V$
		-5.3	—	—	A	
		-4.5	—	—		
$R_{DS(on)}$	Static Drain-Source IRFR9010/9014, IRFU9010/9014 IRFR9012/9015, IRFU9012/9015	—	—	0.50	Ω	$V_{GS} = 10V$, $I_D = -2.8A$
		—	—	0.70		
g_{fs}	Forward Transconductance (2)	1.1	—	—	U	$V_{DS} \leq -50V$, $I_D = -2.8A$
C_{iss}	Input Capacitance	—	308	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	123	—	pF	$V_{DS} = -25V$
C_{rss}	Reverse Transfer Capacitance	—	55	—	pF	$f = 1.0\text{MHz}$
$t_{d(on)}$	Turn-On Delay Time	—	—	9.2	ns	$V_{DD} = -25V$, $I_D = -4.7A$, $Z_O = 24\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	—	71	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	—	20	ns	
t_f	Fall Time	—	—	59	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	—	9.1	nC	$V_{GS} = -10V$, $I_D = -4.7A$, $V_{DS} = 0.8\text{Max. Rating}$ (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	—	3.0	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	—	5.9	nC	

THERMAL RESISTANCE

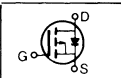
R_{thJC}	Junction-to-Case	MAX	5.0	K/W	
R_{thCS}	Case-to-Sink	TYP	1.7	K/W	Mounting surface flat smooth, and greased
R_{thJA}	Junction-to-Ambient	MAX	110	K/W	Free Air Operation

Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C

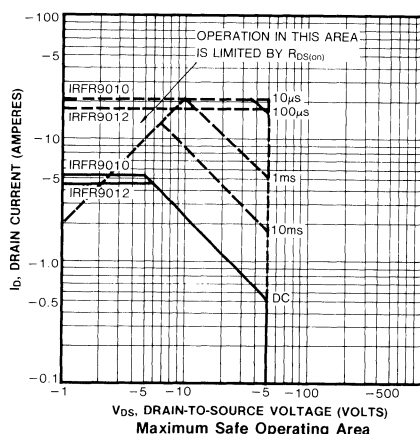
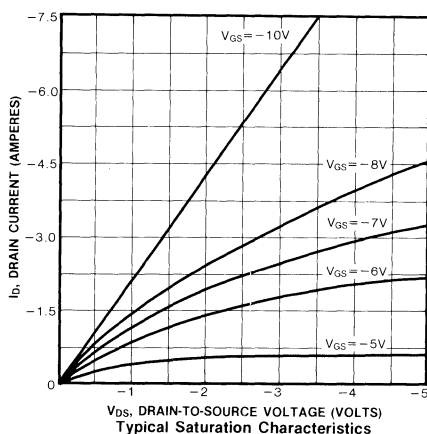
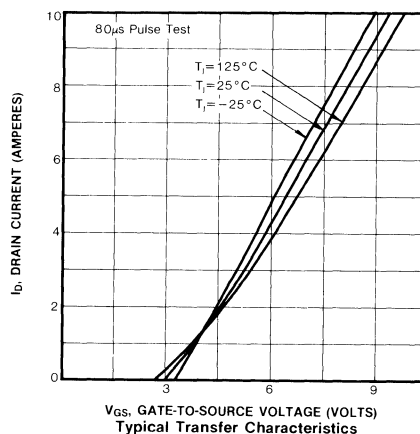
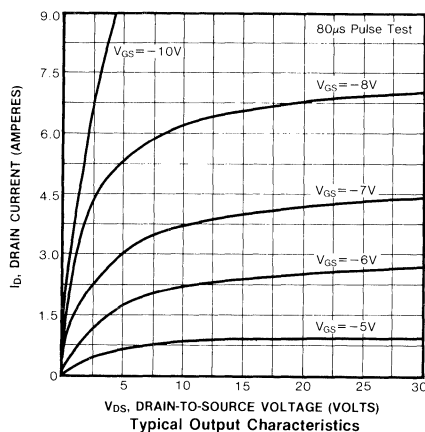
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

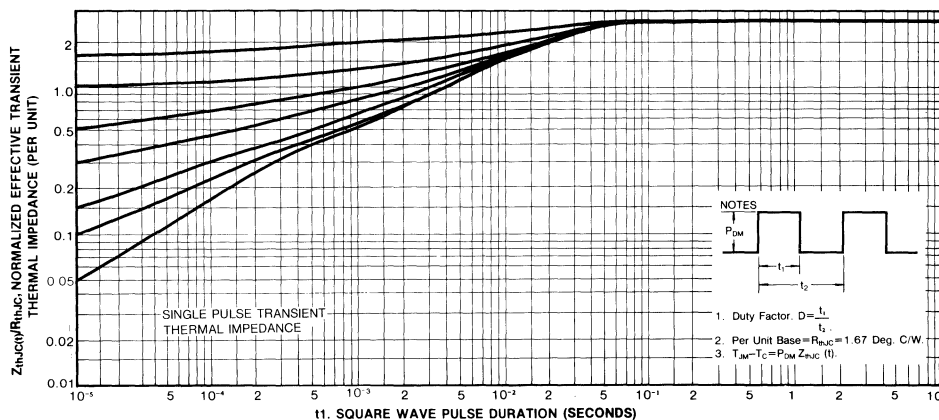
(3) Repetitive rating: Pulse width limited by max. junction temperature

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

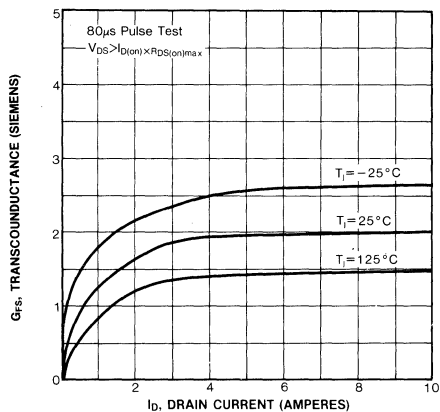
Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-5.3	A	Modified MOSFET integral reverse P-N junction rectifier 
I_{SM}	Pulse Source Current (3)	—	—	-18	A	
V_{SD}	Diode Forward Voltage	—	—	-5.5	V	$T_C = 25^\circ\text{C}$, $I_S = -5.3\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	—	160	ns	$T_J = 25^\circ\text{C}$, $I_F = -4.7\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{s}$

- Notes:** (1) $T_J = 25^\circ\text{C}$ to 150°C
(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature

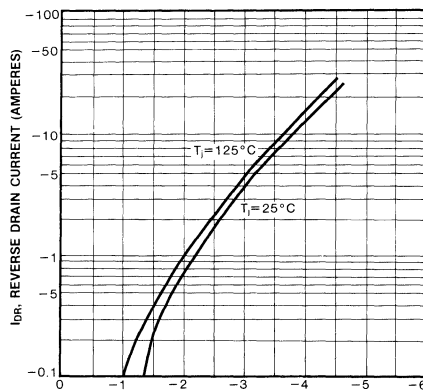




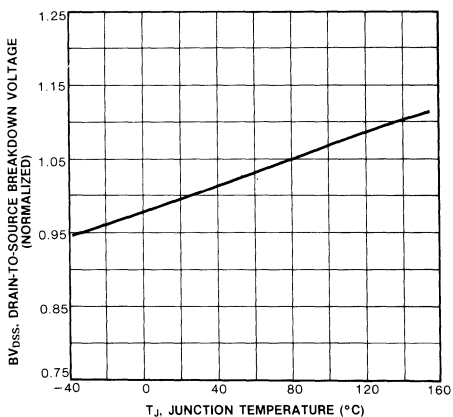
Maximum Effective Transient Thermal Impedance Junction-to-Case Vs. Pulse Duration



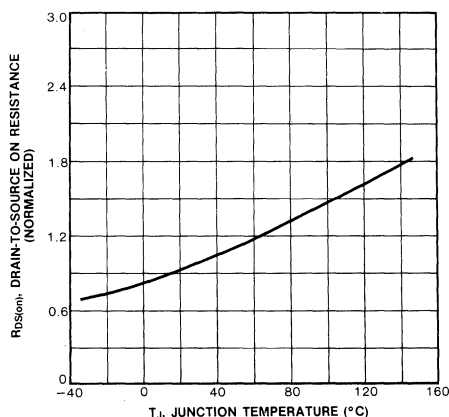
Typical Transconductance Vs. Drain Current



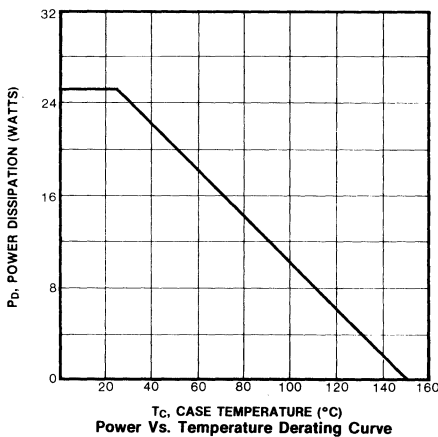
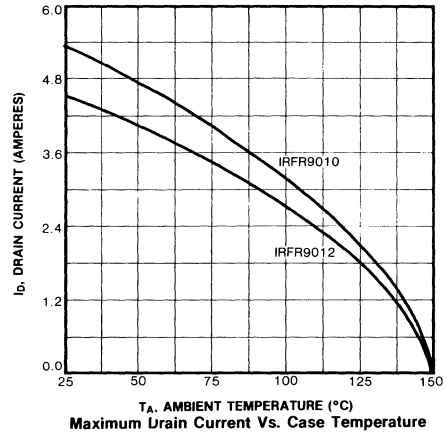
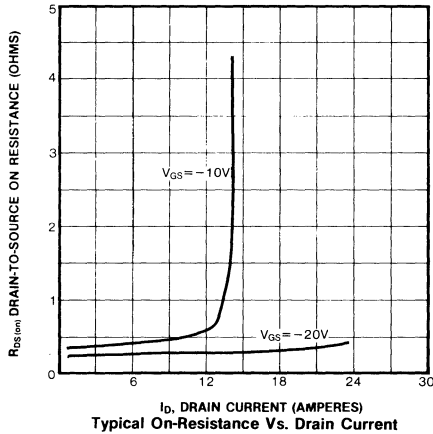
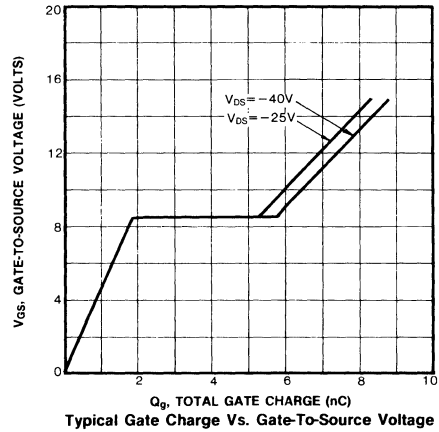
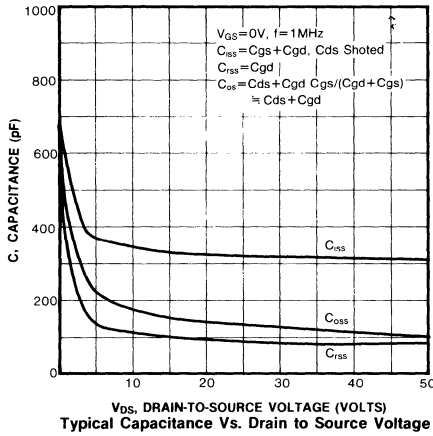
Typical Source-Drain Diode Forward Voltage



Breakdown Voltage Vs. Temperature



Normalized On-Resistance Vs. Temperature



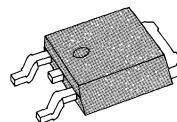
FEATURES

- Lower $R_{DS(ON)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

PRODUCT SUMMARY

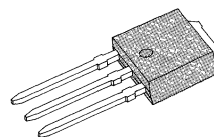
Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFR9020/U9020	-50V	0.29 Ω	-9.9A
IRFR9022/U9022	-50V	0.33 Ω	-9.0A
IRFR9024/U9024	-60V	0.29 Ω	-9.9A
IRFR9025/U9025	-60V	0.33 Ω	-9.0A

D-PACK



IRFR9020/9022
 IRFR9024/9025

I-PACK



IRFU9020/9022
 IRFU9024/9025

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	IRFR9020 IRFU9020	IRFR9022 IRFU9022	IRFR9024 IRFU9024	IRFR9025 IRFU9025	Unit
Drain-Source Voltage (1)	V _{DSS}	-50		-60V		Vdc
Drain-Gate Voltage (R _{GS} =1.0MΩ)(1)	V _{DGR}	-50		-60		Vdc
Gate-Source Voltage	V _{GS}	±20				Vdc
Continuous Drain Current T _C =25°C	I _D	-9.9	-9.0	-9.9	-9.0	Adc
Continuous Drain Current T _C =100°C	I _D	-6.3	-5.7	-6.3	-5.7	Adc
Drain Current—Pulsed (3)	I _{DM}	-40	-36	-40	-36	Adc
Gate Current—Pulsed	I _{GM}	±1.5				Adc
Single Pulsed Aualanche Energy (4)	E _{AS}	440				mj
Avalanche Current	I _{AS}	-9.9				A
Total Power Dissipation at T _C =25°C Derate above 25°C	P _D	42 0.32				Watts W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-55 to 150				°C
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T _L	300				°C

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=5.1mH$, $V_{dd}=-25V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-Source Breakdown Voltage	-60	—	—	V	V _{GS} =0V, I _D =-250μA
	IRFR9024/9025, IRFU9024/9025	-50	—	—	V	
	IRFR9020/9022, IRFU9020/9022	—	—	—	—	—
V _{GS(th)}	Gate Threshold Voltage	-2.0	—	-4.0	V	V _{DS} =V _{GS} , I _D =-250μA
I _{GSS}	Gate-Source Leakage Forward	—	—	-100	nA	V _{GS} =-20V
I _{GSS}	Gate-Source Leakage Reverse	—	—	100	nA	V _{GS} =20V
I _{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	V _{DS} =Max. Rating, V _{GS} =0V V _{DS} =0.8 Max. Rating, V _{GS} =0V, T _J =125°C
I _{D(on)}	On-State Drain-Source Current (2)	—	—	—	A	V _{DS} ≤-3.2V, V _{GS} =-10V
	IRFR9020/9024, IRFU9020/9024	-9.9	—	—	—	
	IRFR9022/9025, IRFU9022/9025	-9.0	—	—	—	—
R _{DS(on)}	Static Drain-Source	—	0.20	0.28	Ω	V _{GS} =-10V, I _D =-5.7A
	IRFR9020/9024, IRFU9020/9024	—	—	0.33	—	
	IRFR9022/9025, IRFU9022/9025	—	—	—	—	—
g _{fs}	Forward Transconductance (2)	2.3	—	—	U	V _{DS} ≤-50V, I _D =-5.7A
C _{iss}	Input Capacitance	—	650	—	pF	V _{GS} =0V
C _{oss}	Output Capacitance	—	220	—	pF	V _{DS} =-25V
C _{rss}	Reverse Transfer Capacitance	—	110	—	pF	f=1.0MHz
t _{d(on)}	Turn-On Delay Time	—	15.4	—	ns	V _{DD} =-25V, I _D =-9.7A, Z _O =18Ω (MOSFET switching times are essentially independent of operating temperature)
t _r	Rise Time	—	25.4	—	ns	
t _{d(off)}	Turn-Off Delay Time	—	20.5	—	ns	
t _f	Fall Time	—	48.1	—	ns	
Q _g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	23.7	—	nC	V _{GS} =-10V, I _D =-9.7A, V _{DS} =0.8Max. Rating (Gate charge is essentially independent of operating temperature.)
Q _{gs}	Gate-Source Charge	—	8.8	—	nC	
Q _{gd}	Gate-Drain ("Miller") Charge	—	10.8	—	nC	

THERMAL RESISTANCE

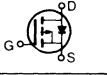
R _{thJC}	Junction-to-Case	MAX	3.0	K/W	
R _{thCS}	Case-to-Sink	TYP	1.7	K/W	Mounting surface flat smooth, and grased
R _{thJA}	Junction-to-Ambient	MAX	110	K/W	Free Air Operation

Notes: (1) T_J=25°C to 150°C

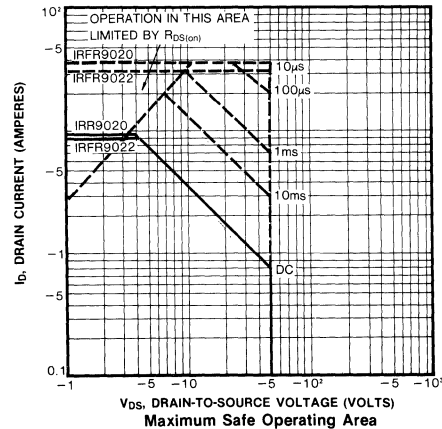
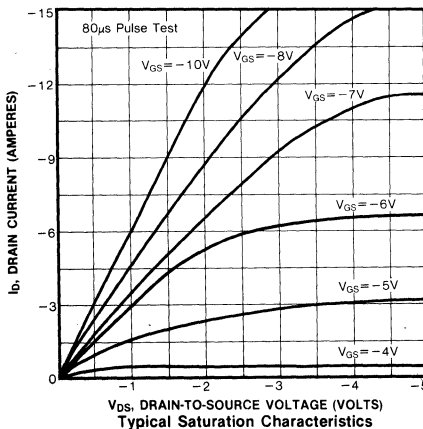
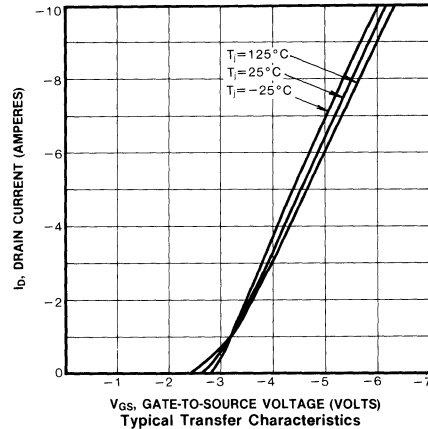
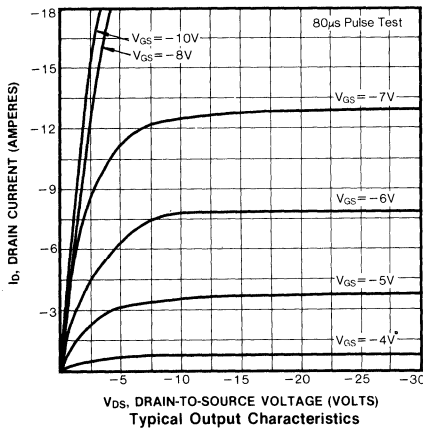
(2) Pulse test: Pulse width≤300μs, Duty Cycle≤2%

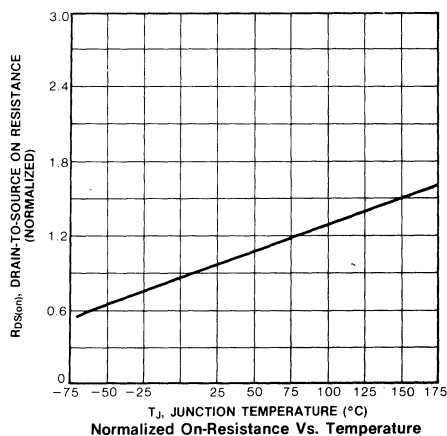
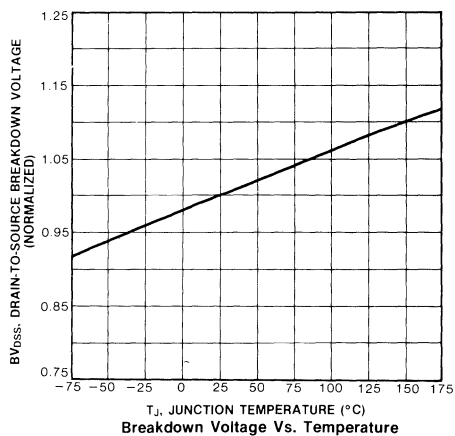
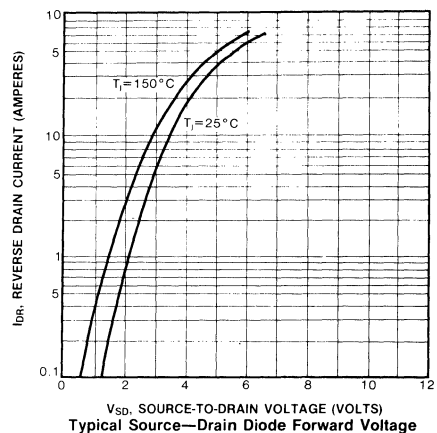
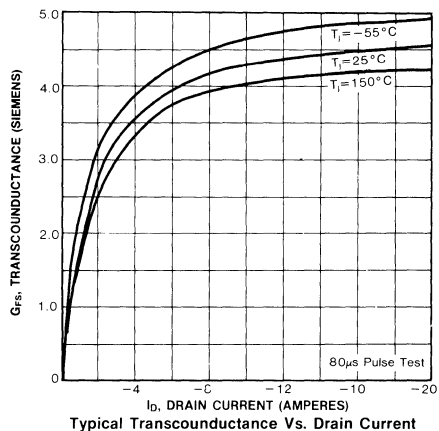
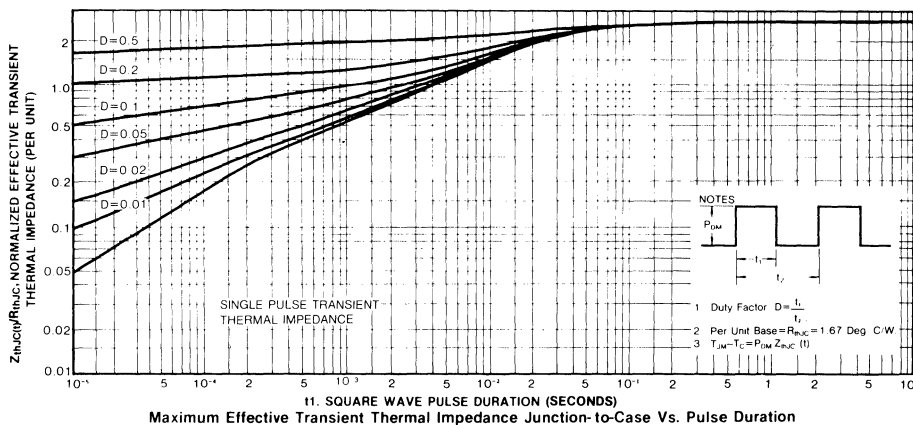
(3) Repetitive rating: Pulse width limited by max. junction temperature

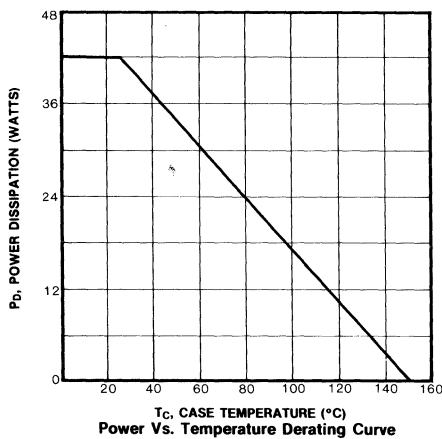
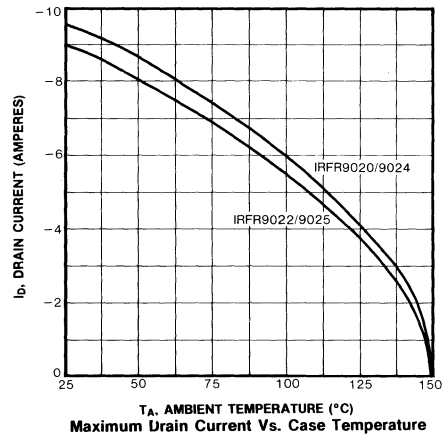
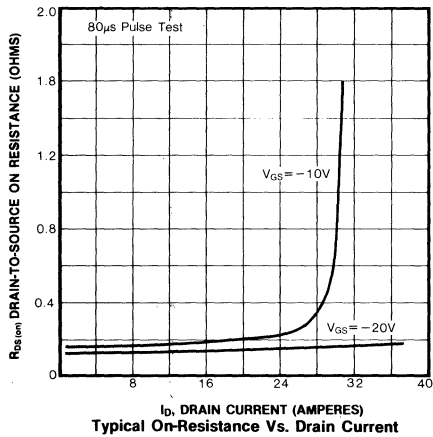
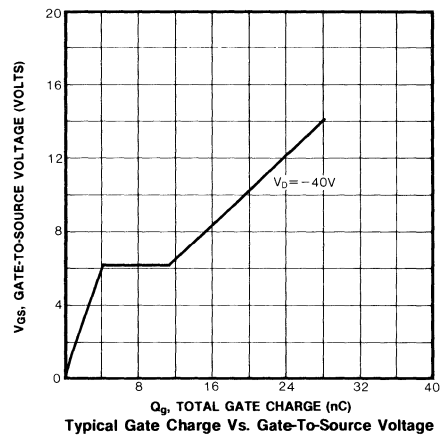
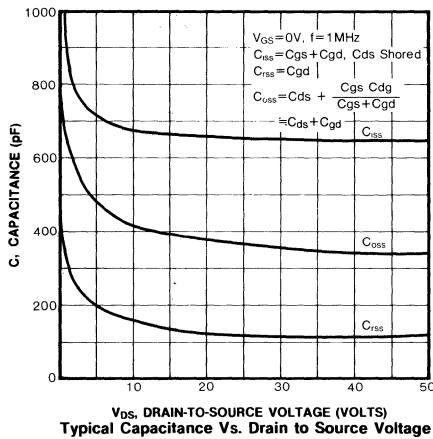
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-9.9	A	Modified MOSFET integral reverse P-N junction rectifier 
I_{SM}	Pulse Source Current (3)	—	—	-40	A	
V_{SD}	Diode Forward Voltage	—	—	-6.3	V	$T_J = 25^\circ\text{C}$, $I_S = -5.3\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	—	280	ns	$T_J = 25^\circ\text{C}$, $I_F = -4.7\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$

- Notes:** (1) $T_J = 25^\circ\text{C}$ to 150°C
(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature







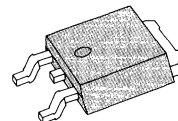
FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

PRODUCT SUMMARY

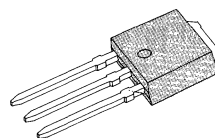
Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFR9120/U9120	−100V	0.60Ω	−5.9A
IRFR9121/U9121	−80V	0.60Ω	−5.9A

D-PACK



IRFR9120/9121

I-PACK



IRFU9120/9121

MAXIMUM RATINGS

Characteristic	Symbol	IRFR9120/U9120	IRFR9121/U9121	Unit
Drain-Source Voltage (1)	V_{DS}	−100	−80	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	−100	−80	Vdc
Gate-Source Voltage	V_{GS}	± 20		Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	−5.9		Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	−3.7		Adc
Drain Current—Pulsed (3)	I_{DM}	−24		Adc
Gate Current—Pulsed	I_{GM}	± 1.5		Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	370		mJ
Avalanche Current	I_{AS}	−5.9		A
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	42 0.33		Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to 150		$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300		$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=18mH$, $V_{dd}=-25V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-Source Breakdown Voltage IRFR9120/U9120	-100	—	—	V	V _{GS} =0V
	IRFR9121/U9121	-80	—	—	V	I _D =-250μA
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} =V _{GS} , I _D =-250μA
I _{GSS}	Gate-Source Leakage Forward	—	—	100	nA	V _{GS} =-20V
I _{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	V _{GS} =20V
I _{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	V _{DS} =Max. Rating, V _{GS} =0V
		—	—	1000	μA	V _{DS} =Max. Rating×0.8, V _{GS} =0V, T _C =125°C
I _{D(on)}	On-State Drain-Source Current (2)	-5.9	—	—	A	V _{DS} >I _{D(on)} ×R _{DS(on)max} , V _{GS} =-10V
R _{DS(on)}	Static Drain-Source On-State Resistance (2)	—	0.50	0.60	Ω	V _{GS} =-10V, I _D =-3.7A
g _{fs}	Forward Transconductance (2)	1.5	—	—	Ω	V _{DS} ≤-50V, I _D =-3.7A
C _{iss}	Input Capacitance	—	427	—	pF	V _{GS} =0V, V _{DS} =-25V, f=1.0MHz
C _{oss}	Output Capacitance	—	128	—	pF	
C _{rss}	Reverse Transfer Capacitance	—	44.5	—	pF	
t _{d(on)}	Turn-On Delay Time	—	9.0	13	ns	V _{DD} =0.5BV _{DSS} , I _D =-6.4A, Z _O =18Ω (MOSFET switching times are essentially independent of operating temperature)
t _r	Rise Time	—	44	66	ns	
t _{d(off)}	Turn-Off Delay Time	—	10	15	ns	
t _f	Fall Time	—	22	33	ns	
Q _g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	13	20	nC	V _{GS} =-10V, I _D =-6.4A, V _{DS} =0.8 Max. Rating (Gate charge is essentially independent of operating temperature.)
Q _{gs}	Gate-Source Charge	—	2.0	3.0	nC	
Q _{gd}	Gate-Drain ("Miller") Charge	—	6.8	10	nC	

THERMAL RESISTANCE

R _{thJC}	Junction-to-Case	MAX	3.0	K/W	
R _{thCS}	Case-to-Sink	TYP	1.7	K/W	Mounting surface flat, smooth, and greased
R _{thJA}	Junction-to-Ambient	MAX	110	K/W	Free Air Operation

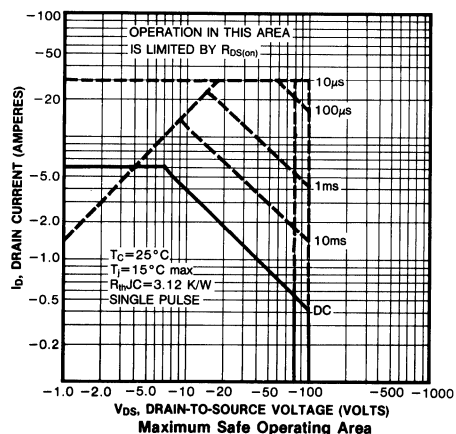
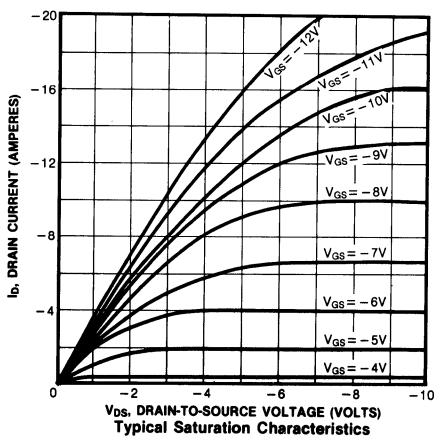
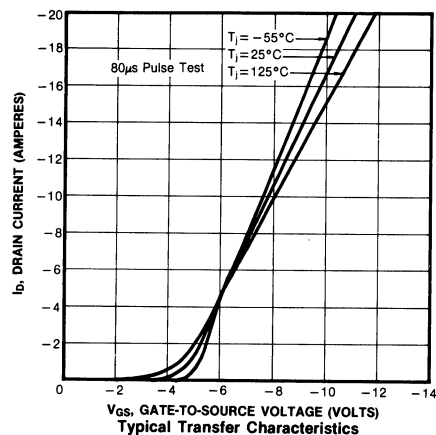
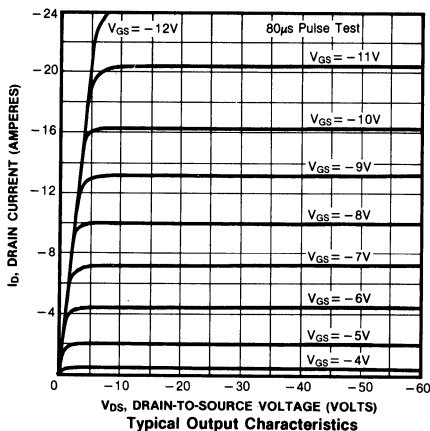
- Notes:** (1) T_J=25°C to 150°C
(2) Pulse test: Pulse width≤300μs, Duty Cycle≤2%
(3) Repetitive rating: Pulse width limited by max. junction temperature

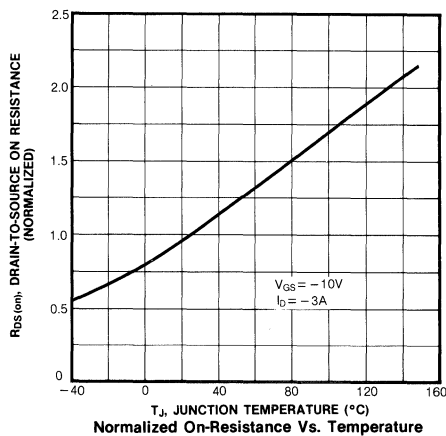
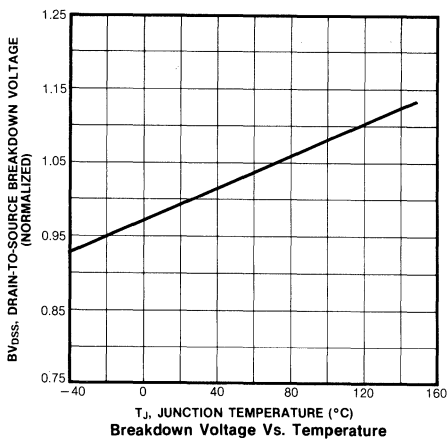
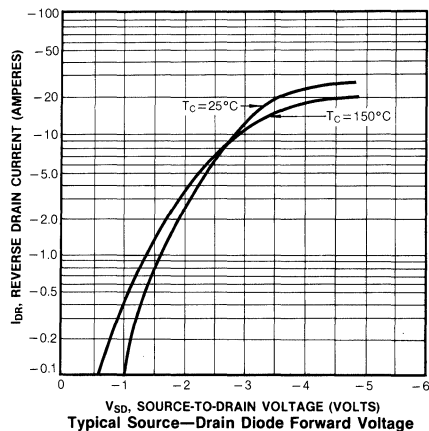
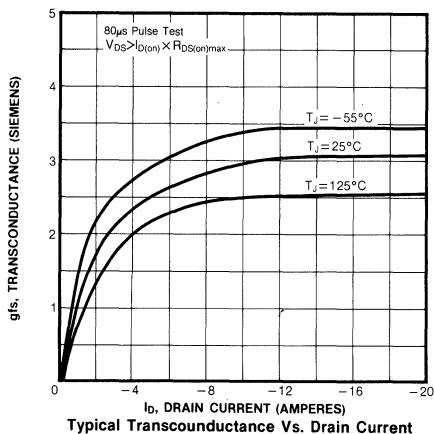
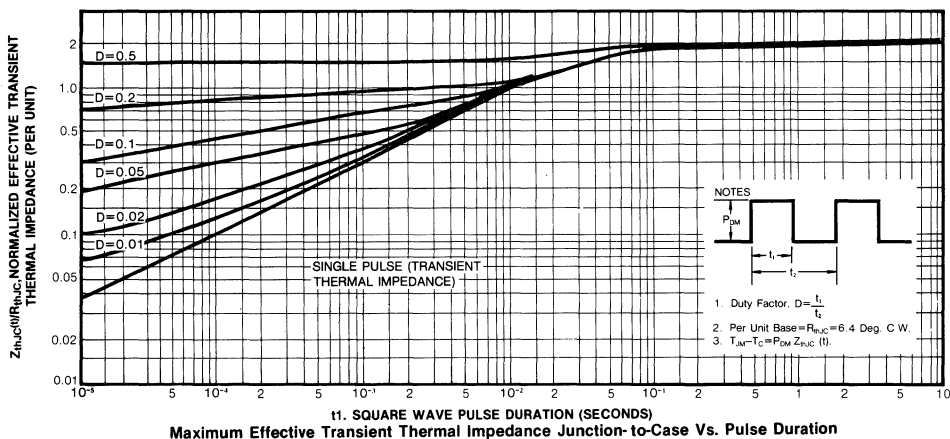
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

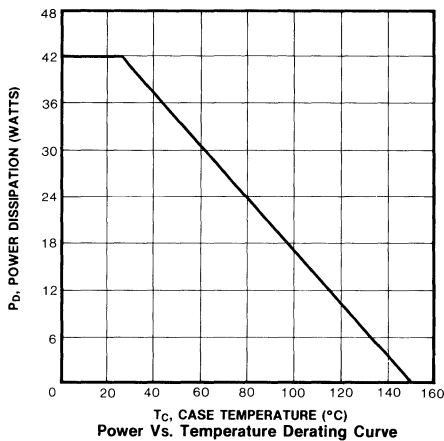
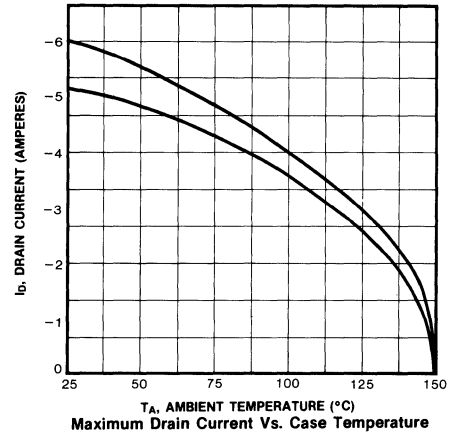
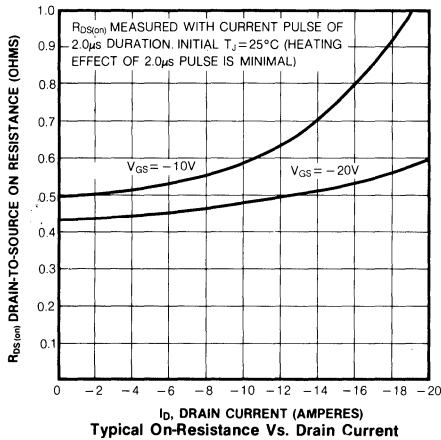
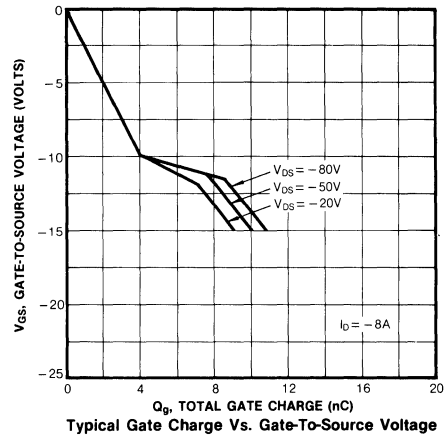
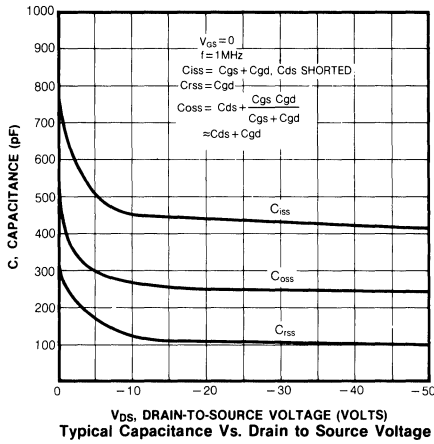
Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-5.9	A	Modified MOSFET showing the integral reverse P-N junction rectifier
I_{SM}	Pulse Source Current(Body Diode)(3)	—	—	-24	A	
V_{SD}	Diode Forward Voltage (2)	—	—	-6.3	V	$T_C = 25^\circ\text{C}$, $I_S = -5.9\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	—	—	ns	$T_J = 150^\circ\text{C}$, $I_F = -6.4\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$

Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature

2







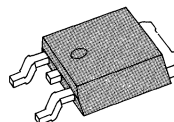
FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

PRODUCT SUMMARY

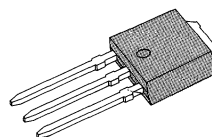
Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFR9210/U9210	-200V	3.0Ω	-2.0A
IRFR9212/U9212	-200V	4.5Ω	-1.6A

D-PACK



IRFR9210/9212

I-PACK



IRFU9210/9212

MAXIMUM RATINGS

Characteristic	Symbol	IRFR9210/U9120	IRFR9212/U9212	Unit
Drain-Source Voltage (1)	V_{DSS}	-200		Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	-200		Vdc
Gate-Source Voltage	V_{GS}	± 20		Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	-2.0	-1.6	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	-1.2	-1.0	Adc
Drain Current—Pulsed (3)	I_{DM}	-8.0	-6.4	Adc
Gate Current—Pulsed	I_{GM}	± 1.5		Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	150		mJ
Avalanche Current	I_{AS}	-2.0		A
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	25 0.20		Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300		$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=59mH$, $V_{dd}=-50V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage	-200	—	—		$V_{GS}=0V$ $I_D=-250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}$, $I_D=-250\mu A$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS}=-20V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	$V_{GS}=20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS}=\text{Max. Rating}$, $V_{GS}=0V$
		—	—	1000	μA	$V_{DS}=\text{Max. Rating} \times 0.8$, $V_{GS}=0V$, $T_C=125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2) IRFR9210/U9210	-2.0	—	—	A	$V_{DS}>I_{D(on)} \times R_{DS(on)max}$, $V_{GS}=-10V$
	IRFR9212/U9212	-1.6	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance (2) IRFR9210/U9210	—	—	3.0	Ω	$V_{GS}=-10V$, $I_D=-1.0A$
	IRFR9212/U9212	—	—	4.5	Ω	
		—	—	—	—	
g_{fs}	Forward Transconductance (2)	0.61	—	—	S	$V_{DS} \leq -50V$, $I_D=-1.0A$
C_{iss}	Input Capacitance	—	180	—	pF	$V_{GS}=0V$, $V_{DS}=-25V$, $f=1.0\text{MHz}$
C_{oss}	Output Capacitance	—	53	—	pF	
C_{rss}	Reverse Transfer Capacitance	—	17	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	8.0	12	ns	$V_{DD}=0.5BV_{DSS}$, $I_D=-2.3A$, $Z_\theta=24.1$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	12	18	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	11	17	ns	
t_f	Fall Time	—	13	20	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	6.5	9.7	nC	$V_{GS}=-10V$, $I_D=-2.3A$, $V_{DS}=0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	1.4	2.2	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	3.3	5.7	nC	

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	MAX	5.0	K/W	
R_{thCS}	Case-to-Sink	TYP	1.7	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	MAX	110	K/W	Free Air Operation

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C

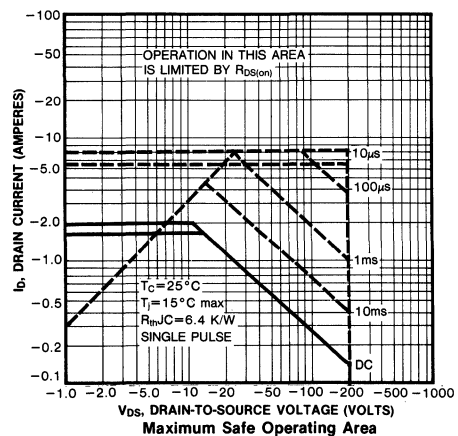
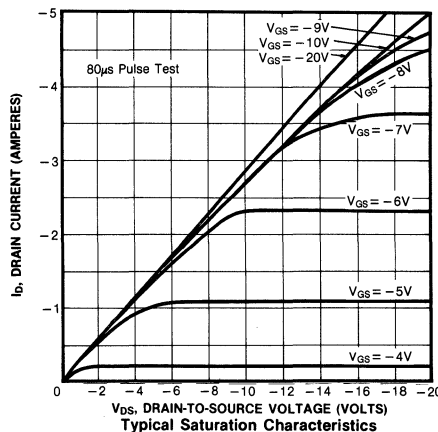
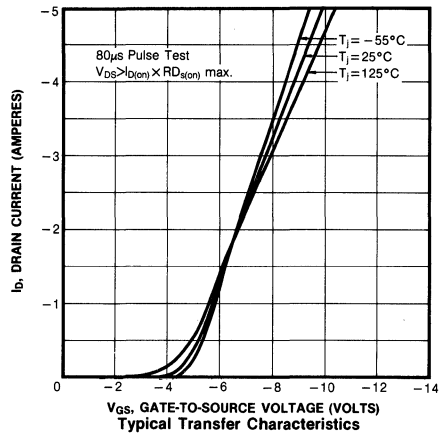
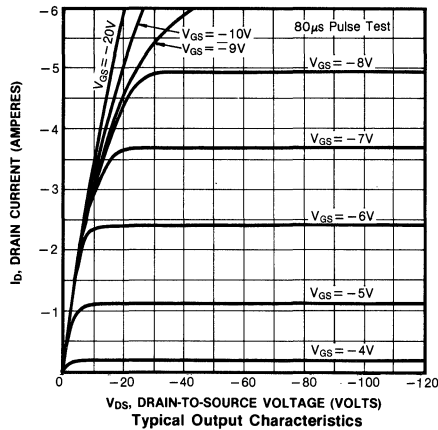
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

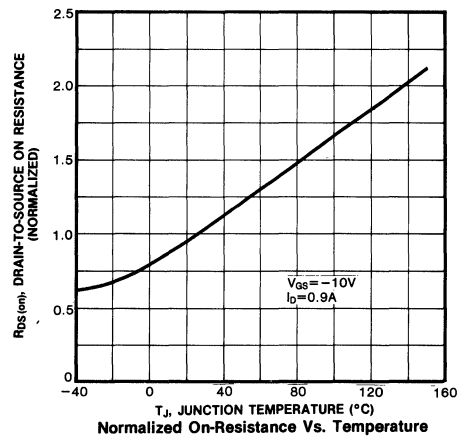
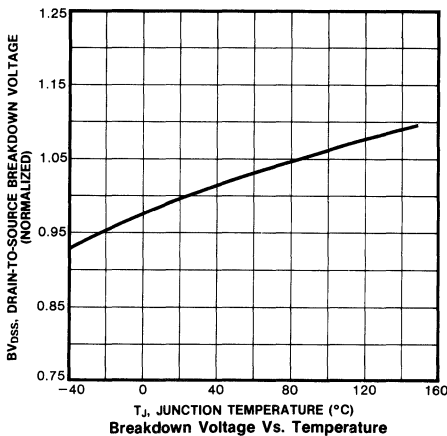
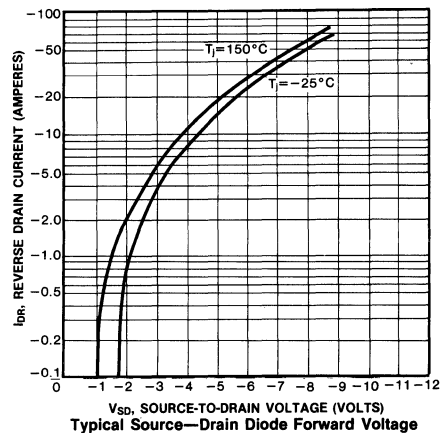
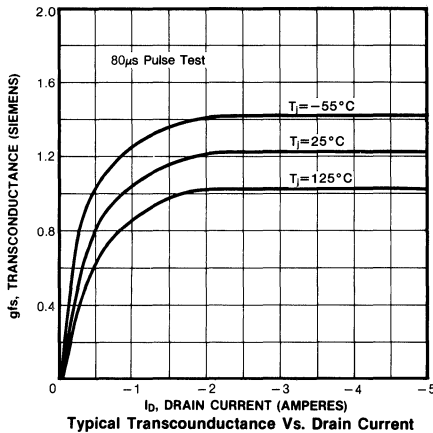
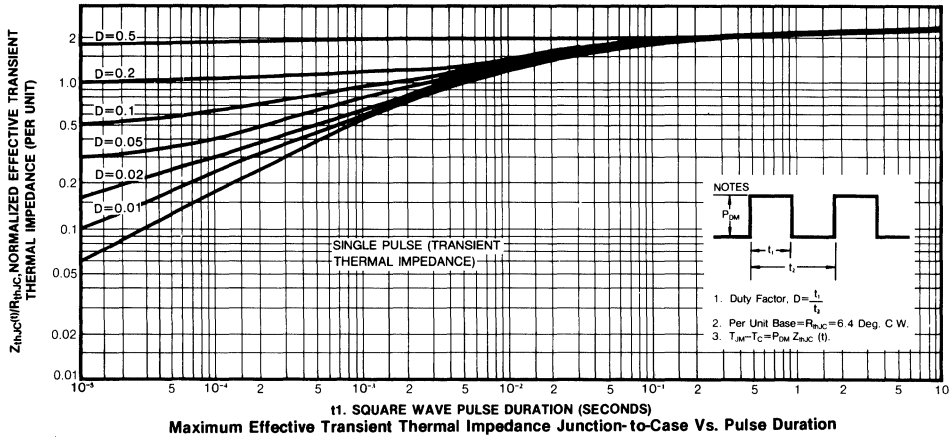
(3) Repetitive rating: Pulse width limited by max. junction temperature

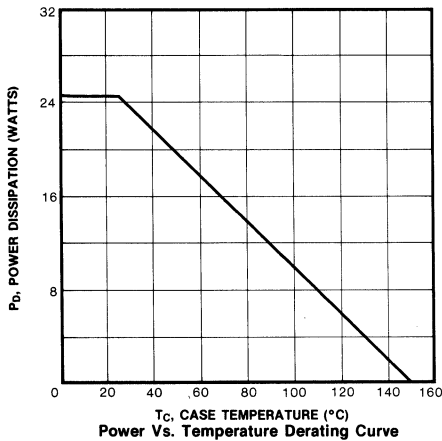
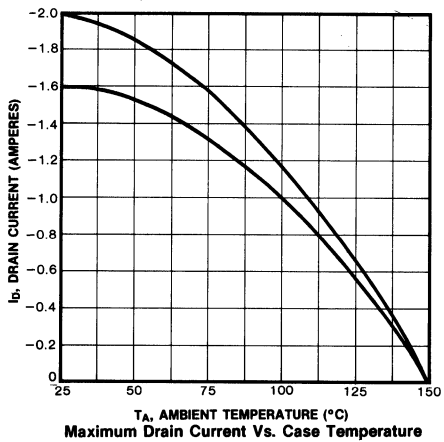
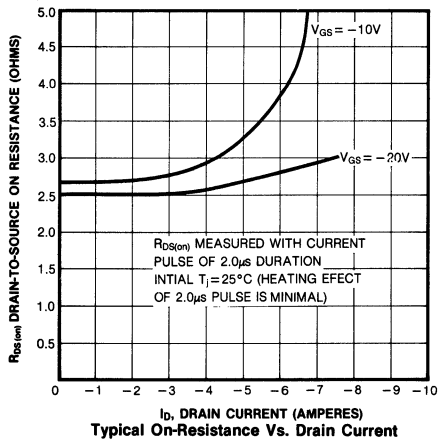
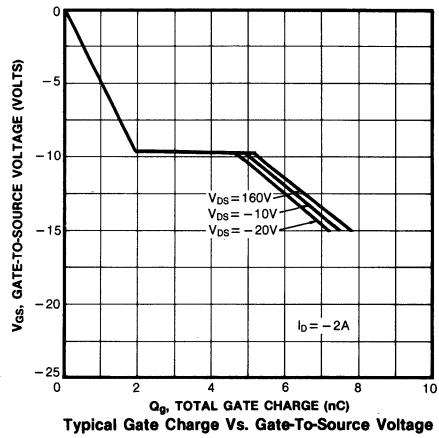
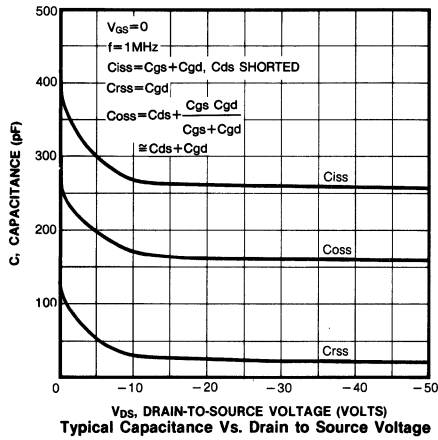
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-2.0	A	Modified MOSFET showing the integral reverse P-N junction rectifier 
I_{SM}	Pulse Source Current(Body Diode)(3)	—	—	-8.0	A	
V_{SD}	Diode Forward Voltage (2)	—	—	-5.8	V	$T_C = 25^\circ\text{C}$, $I_S = -2.0\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	99	214	ns	$T_J = 150^\circ\text{C}$, $I_F = -2.3\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$

Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature

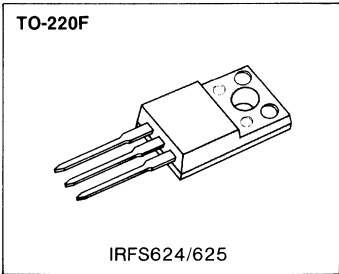






FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability



PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFS624	250V	$1.1\ \Omega$	3.3A
IRFS625	250V	$1.5\ \Omega$	2.9A

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	IRFS624	IRFS625	Unit
Drain-Source Voltage (1)	V_{DSS}	250	250	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	250	250	Vdc
Gate-Source Voltage	V_{GS}	± 20		Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	3.3	2.9	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	2.1	1.8	Adc
Drain Current—Pulsed (3)	I_{DM}	15	13	Adc
Gate Current—Pulsed	I_{GM}	± 1.5		Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	83		mJ
Avalanche Current	I_{AS}	3.3		A
Total Power Dissipation at $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	30 0.24		Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300		$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature
(4) $L=12mH$, $V_{dd}=50V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-Source Breakdown Voltage	IRFS624 250	—	—	V	V _{GS} =0V, I _D =250μA
		IRFS625 250	—	—	V	
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} =V _{GS} , I _D =250μA
I _{GSS}	Gate-Source Leakage Forward	—	—	100	nA	V _{GS} =20V
I _{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	V _{GS} =-20V
I _{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	V _{DS} =Max. Rating×0.8, V _{GS} =0V
		—	—	1000	μA	V _{DS} =Max. Rating×0.8, V _{GS} =0V, T _C =125°C
I _{D(on)}	On-State Drain-Source Current (2)	IRFS624 3.3	—	—	A	V _{DS} ≥4.9V
		IRFS625 2.9	—	—	A	V _{GS} =10V
R _{DS(on)}	Static Drain-Source On-State Resistance	IRFS624 —	—	1.1	Ω	V _{GS} =10V, I _D =2.1A
		IRFS625 —	—	1.50	Ω	
g _{ts}	Forward Transconductance (2)	1.4	2.1	—	∅	V _{DS} ≥50V, I _D =1.9A
C _{iss}	Input Capacitance	—	390	—	pF	V _{GS} =0V
C _{oss}	Output Capacitance	—	150	—	pF	V _{DS} =25V
C _{rss}	Reverse Transfer Capacitance	—	50	—	pF	f=1.0MHz
t _{d(on)}	Turn-On Delay Time	—	11	17	ns	V _{DD} =0.5 BV _{DSS} , I _D =3.3A Z _O =18Ω (MOSFET switching times are essentially independent of operating temperature)
t _r	Rise Time	—	24	36	ns	
t _{d(off)}	Turn-Off Delay Time	—	21	32	ns	
t _f	Fall Time	—	13	20	ns	
Q _g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	15	22	nC	V _{GS} =10V, I _D =3.3A, V _{DS} =0.8, Max. Rating (Gate charge is essentially independent of operating temperature.)
Q _{gs}	Gate-Source Charge	—	4.0	6.0	nC	
Q _{gd}	Gate-Drain ("Miller") Charge	—	7.2	11	nC	

THERMAL RESISTANCE

R _{thJC}	Junction-to-Case	MAX	4.16	K/W	
R _{thCS}	Case-to-Sink	TYP	1.0	K/W	Mounting surface flat smooth, and greased
R _{thJA}	Junction-to-Ambient	MAX	80	K/W	Free Air Operation

- Notes:** (1) T_J=25°C to 150°C
(2) Pulse test: Pulse width≤300μs, Duty Cycle≤2%
(3) Repetitive rating: Pulse width limited by max. junction temperature

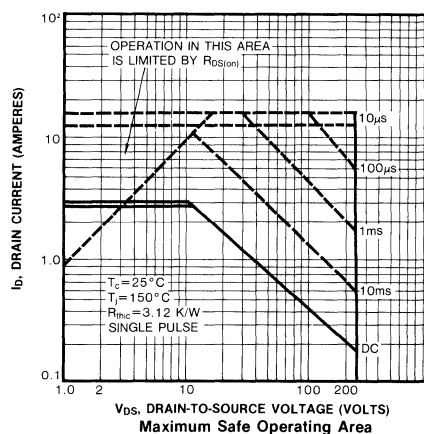
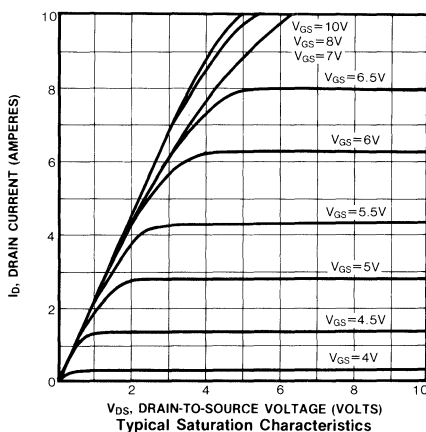
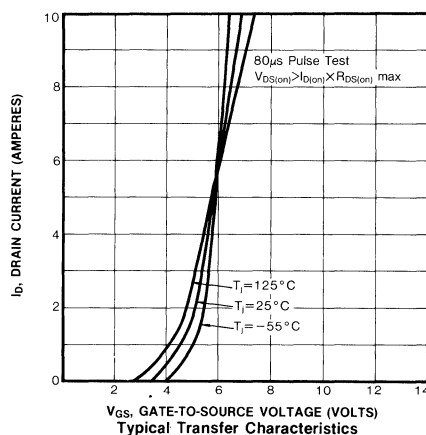
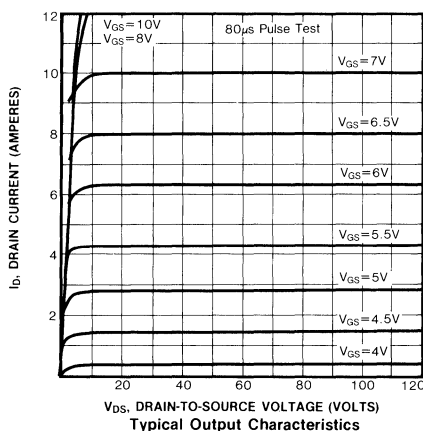
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

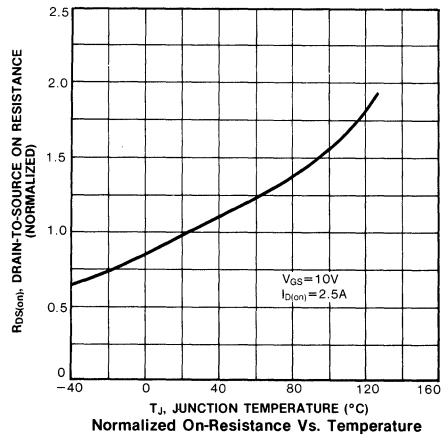
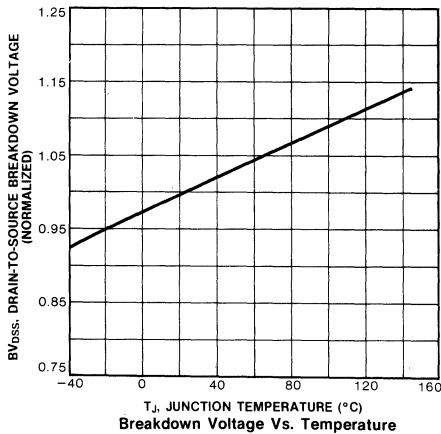
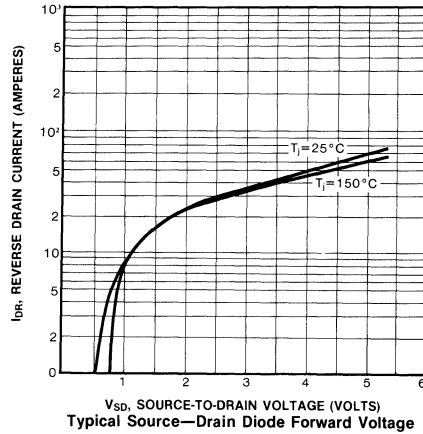
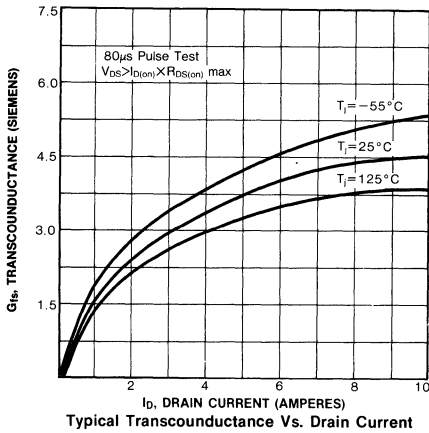
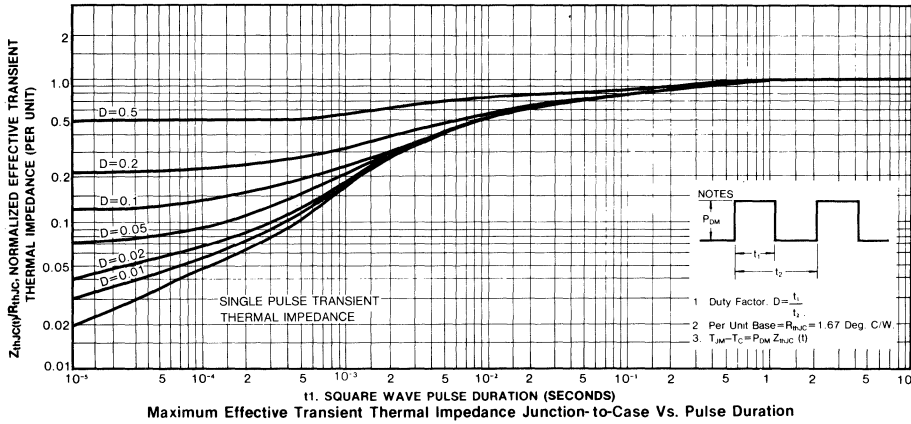
Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	IRFS624	—	3.3	A	Modified MOSFET integral reverse P-N junction rectifier
		IRFS625	—	2.9	A	
I_{SM}	Pulse Source Current (3)	IRFS624	—	15	A	
		IRFS625	—	13	A	
V_{SD}	Diode Forward Voltage	—	—	1.8	V	$T_C = 25^\circ\text{C}$, $I_S = 3.3\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	180	—	ns	$T_J = 25^\circ\text{C}$, $I_F = 3.3\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{s}$

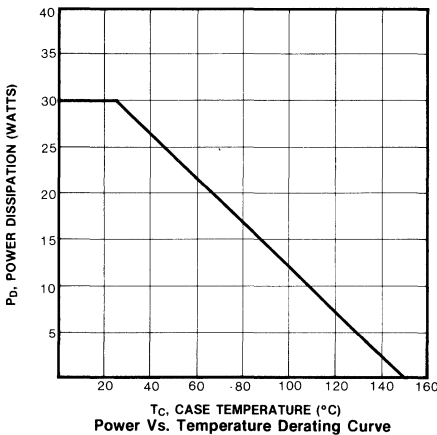
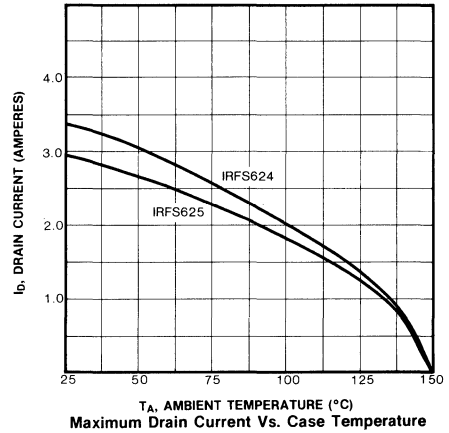
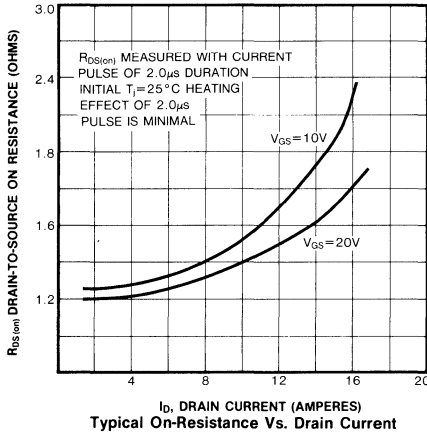
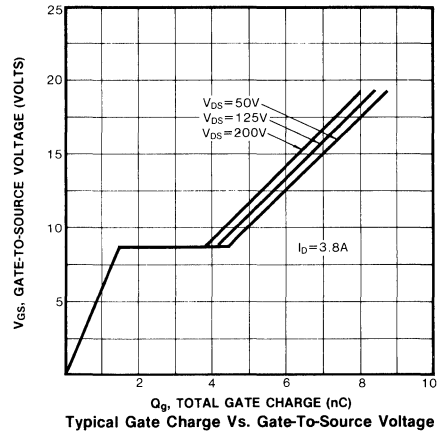
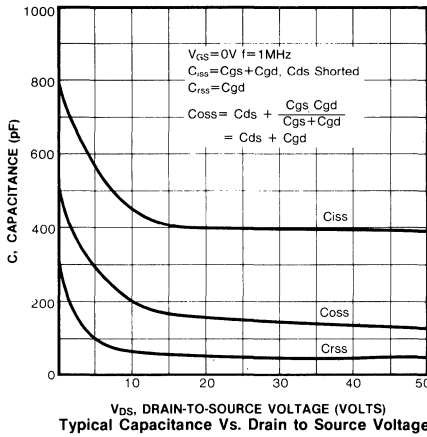
Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C

(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature



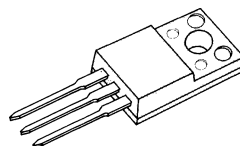




FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

TO-220F



IRFS634/635

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFS634	250V	0.45Ω	5.5A
IRFS635	250V	0.68Ω	4.4A

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	IRFS634	IRFS635	Unit
Drain-Source Voltage (1)	V_{DSS}	250	250	Vdc
Drain-Gate Voltage ($R_{GS}=1.0\text{Mohm}$)(1)	V_{DGR}	250	250	Vdc
Gate-Source Voltage	V_{GS}	± 20		Vdc
Continuous Drain Current $T_C=25^\circ\text{C}$	I_D	5.5	4.4	Adc
Continuous Drain Current $T_C=100^\circ\text{C}$	I_D	3.5	2.8	Adc
Drain Current—Pulsed (3)	I_{DM}	32	26	Adc
Gate Current—Pulsed	I_{GM}	± 1.5		Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	90		mJ
Avalanche Current	I_{AS}	5.5		A
Total Power Dissipation at $T_C=25^\circ\text{C}$ Derate above 25°C	P_D	35 0.28		Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300		$^\circ\text{C}$

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C

(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=5.5\text{mH}$, $V_{dd}=50\text{V}$, $R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
$B_{V_{DS}}$	Drain-Source Breakdown Voltage IRFS634 IRFS635	250 250	— —	— —	V	$V_{GS}=0V$, $I_D=250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}$, $I_D=250\mu A$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS}=20V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	$V_{GS}=-20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS}=\text{Max. Rating}$, $V_{GS}=0V$
		—	—	1000	μA	$V_{DS}=\text{Max. Rating}$, $T_C=125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2) IRFS634 IRFS635	8.1 6.5	— —	— —	A	$V_{DS}\geq 5.5V$ $V_{GS}=10V$
$R_{DS(on)}$	Static Drain-Source On-State Resistance (2) IRFS634 IRFS635	— —	0.40 0.45	0.45 0.68	Ω	$V_{GS}=10V$, $I_D=4.1A$
g_{ts}	Forward Transconductance (2)	2.9	—	—	U	$V_{DS}\geq 50V$, $I_D=4.1A$
C_{iss}	Input Capacitance	—	764	—	pF	$V_{GS}=0V$
C_{oss}	Output Capacitance	—	100	—	pF	$V_{DS}=25V$
C_{rss}	Reverse Transfer Capacitance	—	32	—	pF	$f=1.0\text{MHz}$
$t_{d(on)}$	Turn-On Delay Time	—	9.1	14	ns	$V_{DD}=0.5 B_{V_{DS}}$, $I_D=8.1A$, $Z_O=12\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	—	35	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	31	47	ns	
t_f	Fall Time	—	19	29	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	24	35	nC	$V_{GS}=10V$, $I_D=8.1A$, $V_{DS}=0.8$, Max. Rating (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	5.1	7.7	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	12	8.1	nC	

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	MAX	3.57	K/W	
R_{thCS}	Case-to-Sink	TYP	0.5	K/W	Mounting surface flat smooth, and greased
R_{thJA}	Junction-to-Ambient	MAX	80	K/W	Free Air Operation

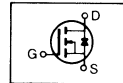
Notes: (1) $T_J=25^\circ\text{C}$ to 150°C

 (2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

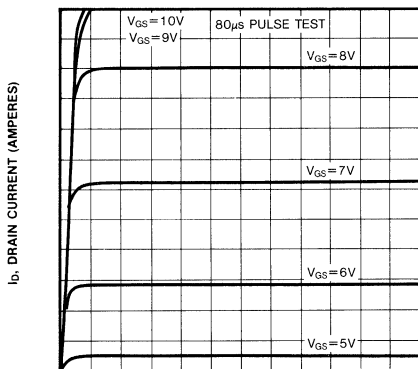
(3) Repetitive rating: Pulse width limited by max. junction temperature

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

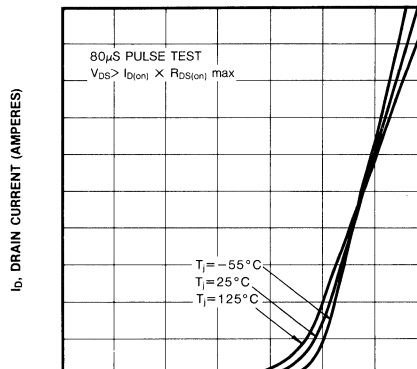
Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	IRFS634 IRFS635	— —	8.1 6.5	A	Modified MOSFET integral reverse P-N junction rectifier
I_{SM}	Pulse Source Current (3)	IRFS634 IRFS635	— —	32 26	A	
V_{SD}	Diode Forward Voltage (2)	IRFS634 IRFS635	— —	2.0 2.0	V	$T_C = 25^\circ\text{C}$, $I_S = 8.1\text{A}$, $V_{GS} = 0\text{V}$ $T_C = 25^\circ\text{C}$, $I_S = 8.1\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	190	390	ns	$T_J = 25^\circ\text{C}$, $I_F = 8.1\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$



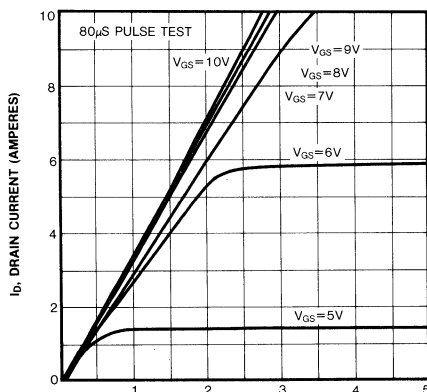
- Notes:** (1) $T_J = 25^\circ\text{C}$ to 150°C
(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature



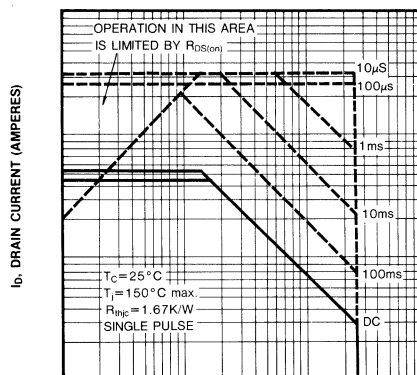
V_{DS} , DRAIN-TO-SOURCE VOLTAGE (VOLTS)
Typical Output Characteristics



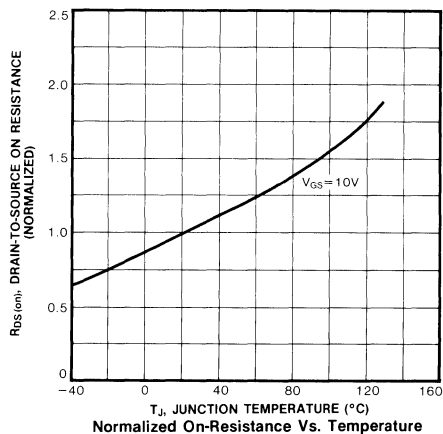
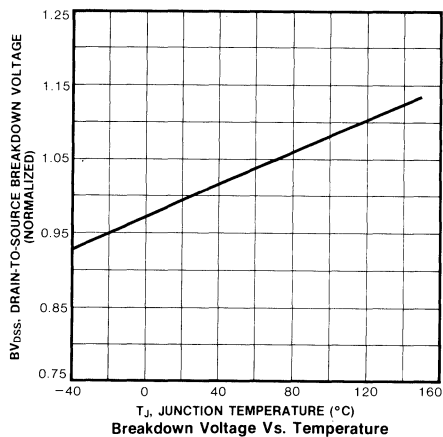
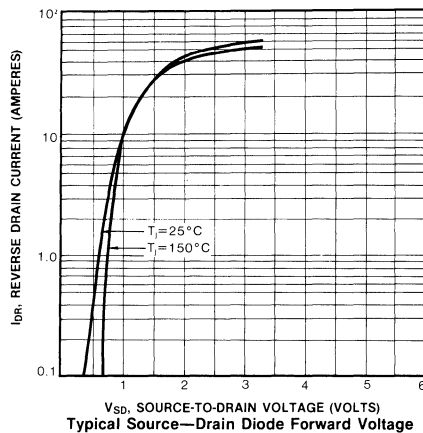
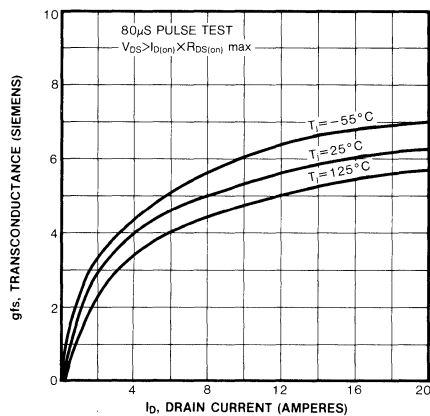
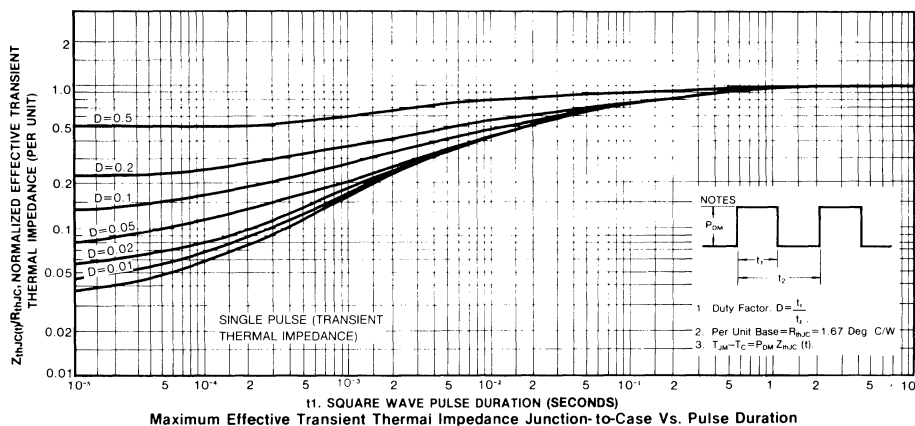
V_{GS} , GATE-TO-SOURCE VOLTAGE (VOLTS)
Typical Transfer Characteristics

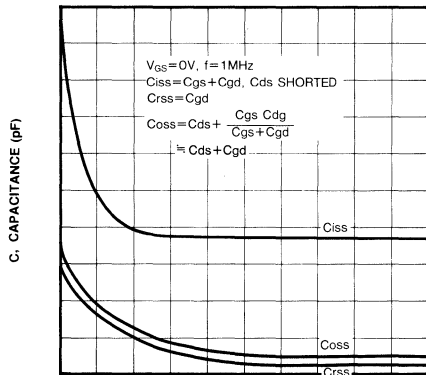


V_{DS} , DRAIN-TO-SOURCE VOLTAGE (VOLTS)
Typical Saturation Characteristics

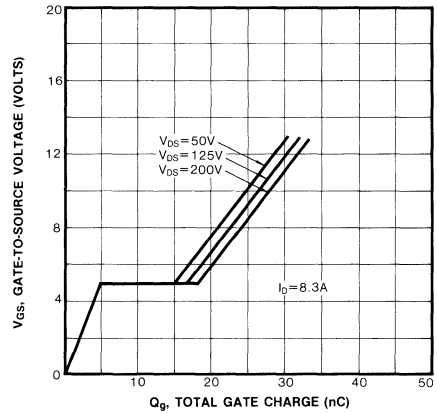


V_{DS} , DRAIN-TO-SOURCE VOLTAGE (VOLTS)
Maximum Safe Operating Area

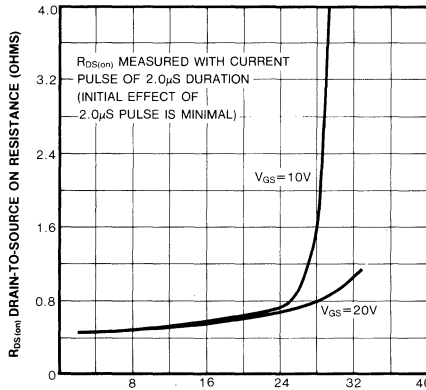




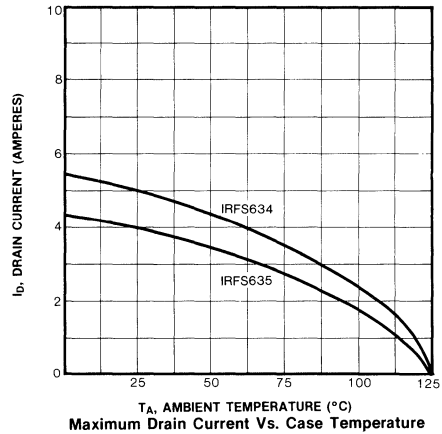
Typical Capacitance Vs. Drain to Source Voltage



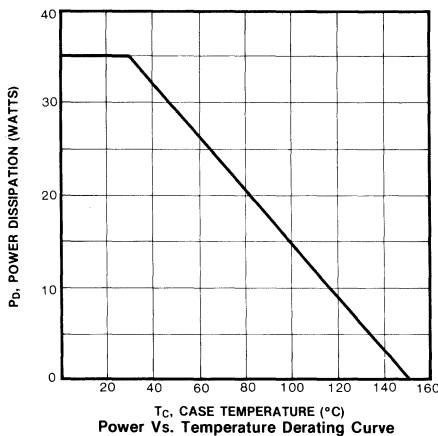
Typical Gate Charge Vs. Gate-To-Source Voltage



Typical On-Resistance Vs. Drain Current



Maximum Drain Current Vs. Case Temperature

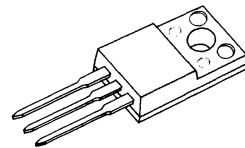


Power Vs. Temperature Derating Curve

FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

TO-220F



IRFS644/645

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFS644	250V	$0.28\ \Omega$	8.5A
IRFS645	250V	$0.34\ \Omega$	7.4A

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	IRFS644	IRFS645	Unit
Drain-Source Voltage (1)	V_{DSS}	250	250	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	250	250	Vdc
Gate-Source Voltage	V_{GS}	± 20		Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	8.5	7.4	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	5	4.5	Adc
Drain Current—Pulsed (3)	I_{DM}	56	52	Adc
Gate Current—Pulsed	I_{GM}	± 1.5		Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	177		mJ
Avalanche Current	I_{AS}	8.5		A
Total Power Dissipation at $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	40 0.32		Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300		$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$ (2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=4mH$, $V_{dd}=50V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage IRFS644 IRFS645	250 250	— —	— —	V	$V_{GS}=0V$, $I_D=250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}$, $I_D=250\mu A$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS}=20V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	$V_{GS}=-20V$
I_{DSS}	Zero Gate Voltage Drain Current	— —	— —	250 1000	μA μA	$V_{DS}=\text{Max. Rating}$, $V_{GS}=0V$ $V_{DS}=\text{Max. Rating}$, $T_C=125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2) IRFS644 IRFS645	14 13	— —	— —	A	$V_{DS}\geq 4.7V$ $V_{GS}=10V$
$R_{DS(on)}$	Static Drain-Source On-State Resistance (2) IRFS644 IRFS645	— —	0.23 0.28	0.28 0.34	Ω	$V_{GS}=10V$, $I_D=8A$
g_{fs}	Forward Transconductance (2)	6.7	10.2	—	S	$V_{DS}\geq 50V$, $I_D=8A$
C_{iss}	Input Capacitance	—	1472	—	pF	$V_{GS}=0V$
C_{oss}	Output Capacitance	—	190	—	pF	$V_{DS}=25V$
C_{rss}	Reverse Transfer Capacitance	—	69	—	pF	$f=1.0\text{MHz}$
$t_{d(on)}$	Turn-On Delay Time	—	16	20	ns	$V_{DD}=0.5 BV_{DSS}$, $I_D=14A$, $Z_O=9.1\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	67	100	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	53	80	ns	
t_f	Fall Time	—	49	74	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	39	59	nC	$V_{GS}=10V$, $I_D=14A$, $V_{DS}=0.8$, Max. Rating (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	6.6	9.9	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	20	30	nC	

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	MAX	3.12	K/W	
R_{thCS}	Case-to-Sink	TYP	0.5	K/W	Mounting surface flat, Smooth, and greased
R_{thJA}	Junction-to-Ambient	MAX	80	K/W	Free Air Operation

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C

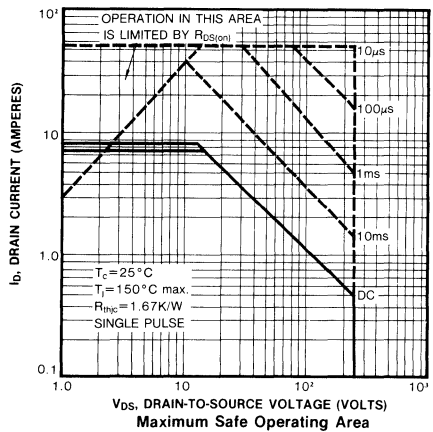
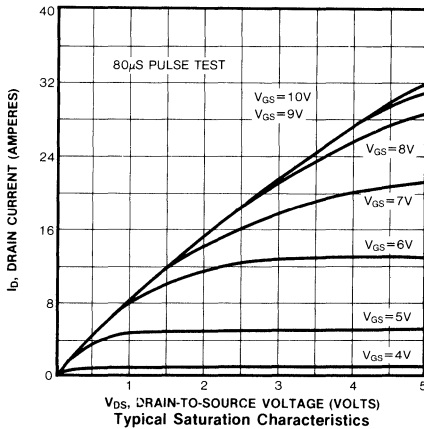
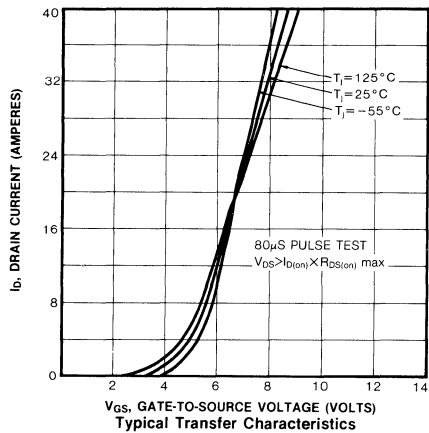
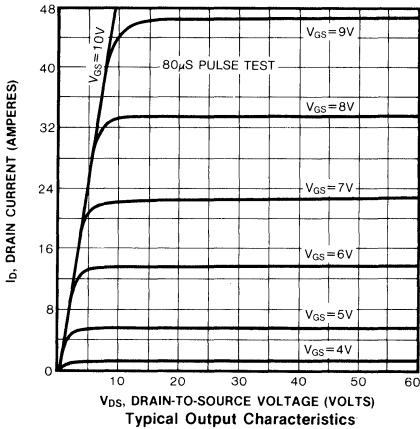
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

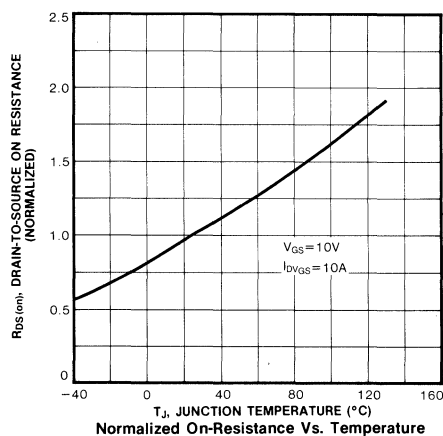
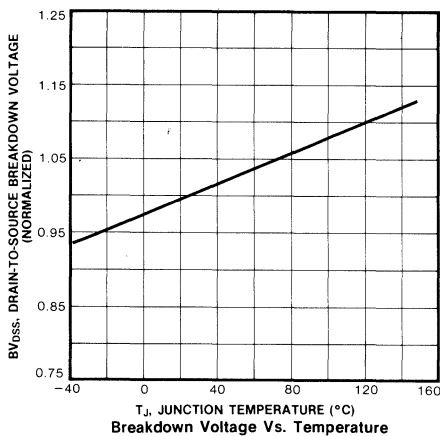
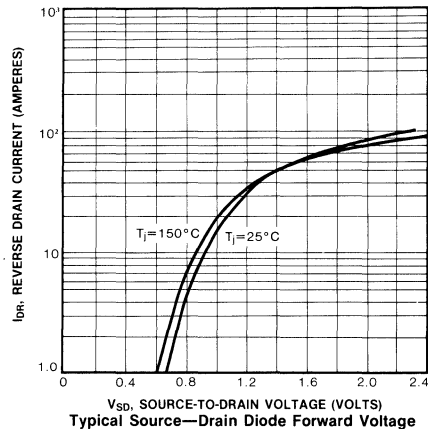
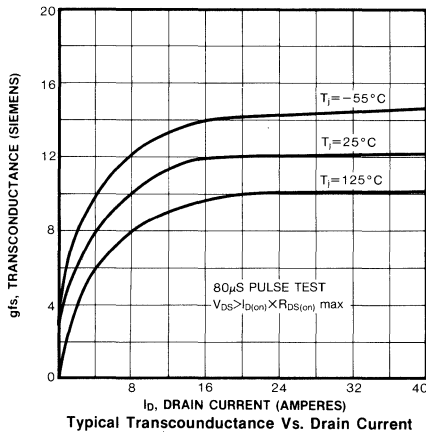
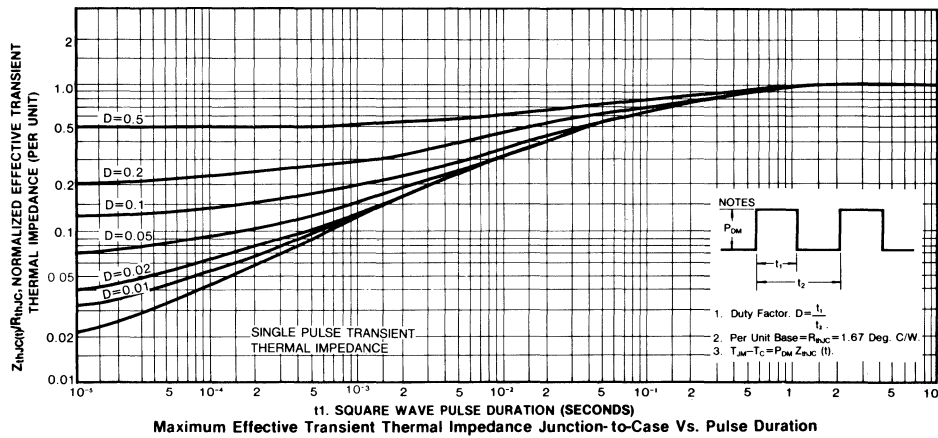
(3) Repetitive rating: Pulse width limited by max. junction temperature

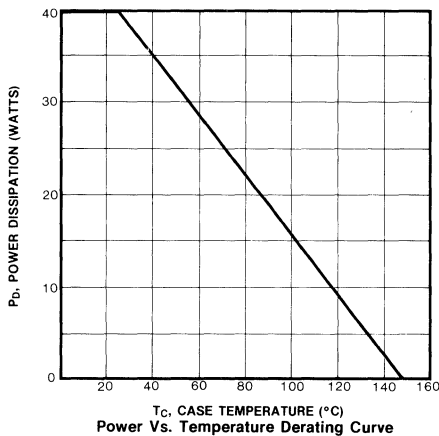
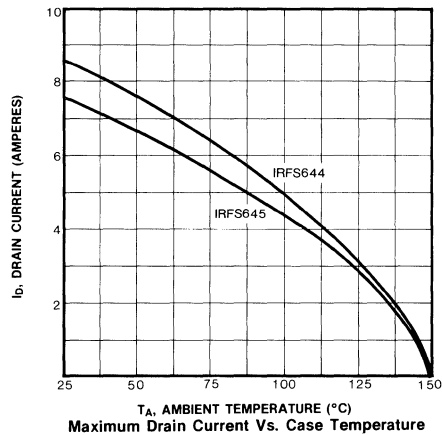
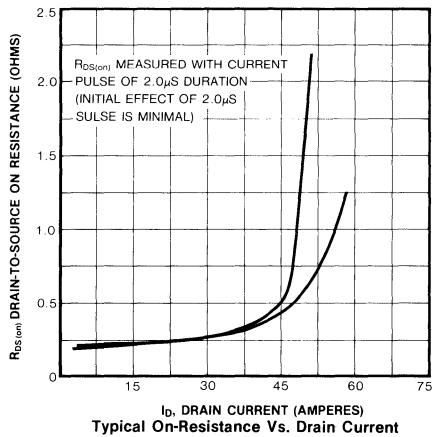
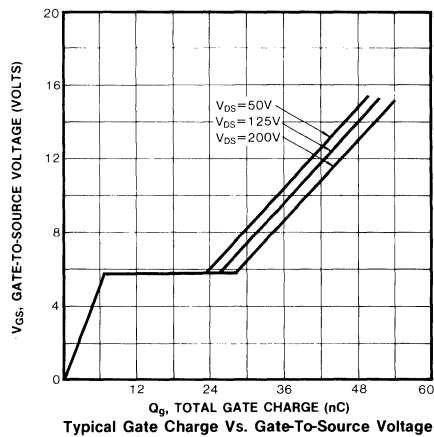
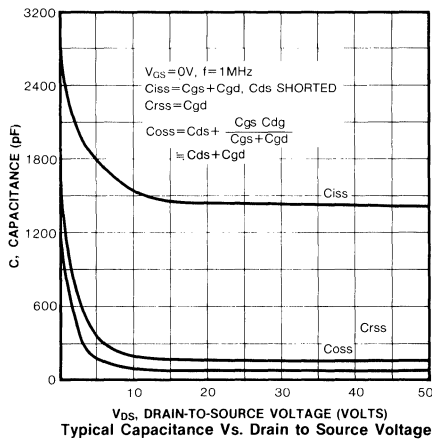
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic		Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	IRFS644 IRFS645	— —	— —	14 13	A	Modified MOSFET integral reverse P-N junction rectifier
I_{SM}	Pulse Source Current (3)	IRFS644 IRFS645	— —	— —	56 52	A	
V_{SD}	Diode Forward Voltage (2)	IRFS644 IRFS645	— —	— —	1.8 1.8	V	$T_C=25^{\circ}\text{C}$, $I_S=14\text{A}$, $V_{GS}=0\text{V}$ $T_C=25^{\circ}\text{C}$, $I_S=14\text{A}$, $V_{GS}=0\text{V}$
t_{rr}	Reverse Recovery Time		—	300	—	ns	$T_J=25^{\circ}\text{C}$, $I_F=14\text{A}$, $dI_F/dt=100\text{A}/\mu\text{S}$

- Notes: (1) $T_J=25^{\circ}\text{C}$ to 150°C
(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature



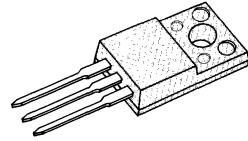




FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

TO-220F



IRFS730/731/732/733

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFS730	400V	$1.0\ \Omega$	3.5A
IRFS731	350V	$1.0\ \Omega$	3.5A
IRFS732	400V	$1.5\ \Omega$	3.0A
IRFS733	350V	$1.5\ \Omega$	3.0A

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	IRFS730	IRFS731	IRFS732	IRFS733	Unit
Drain-Source Voltage (1)	V_{DS}	400	350	400	350	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	400	350	400	350	Vdc
Gate-Source Voltage	V_{GS}	± 20				Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	3.5	3.5	3	3	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	2	2	1.8	1.8	Adc
Drain Current—Pulsed (3)	I_{DM}	32	32	18	18	Adc
Gate Current—Pulsed	I_{GM}	± 1.5				Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	117				mJ
Avalanche Current	I_{AS}	3.5				A
Total Power Dissipation at $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	35 0.28				Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150				$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300				$^\circ C$

- Notes:** (1) $T_J=25^\circ C$ to $150^\circ C$
 (2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
 (3) Repetitive rating: Pulse with limited by max. junction temperature
 (4) $L=17mH$, $V_{dd}=50V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-Source Breakdown Voltage IRFS730/732 IRFS731/733	400 350	— —	— —	V	V _{GS} =0V, I _D =250μA
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} =V _{GS} , I _D =250μA
I _{GSS}	Gate-Source Leakage Forward	—	—	100	nA	V _{GS} =20V
I _{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	V _{GS} =-20V
I _{DSS}	Zero Gate Voltage Drain Current	— —	— —	250 1000	μA	V _{DS} =Max. Rating, V _{GS} =0V V _{DS} =0.8Max. Rating, T _C =125°C
I _{D(on)}	On-State Drain-Source Current (2) IRFS730/731 IRFS732/733	5.5 4.5	— —	— —	A	V _{DS} ≥8.2V, V _{GS} =10V
R _{DS(on)}	Static Drain-Source On-State Resistance (2) IRFS730/731 IRFS732/733	— —	0.8 1.0	1.0 1.5	Ω	V _{GS} =10V, I _D =3A
g _{fs}	Forward Transconductance (2)	2.9	4.4	—	U	V _{DS} ≥50V, I _D =3.0A
C _{iss}	Input Capacitance	—	780	—	pF	V _{GS} =0V
C _{oss}	Output Capacitance	—	99	—	pF	V _{DS} =25V
C _{rss}	Reverse Transfer Capacitance	—	43	—	pF	f=1.0MHz
t _{d(on)}	Turn-On Delay Time	—	11	17	ns	V _{DD} =0.5 BV _{DSS} , I _D =5.5A, Z _O =12Ω (MOSFET switching times are essentially independent of operating temperature)
t _r	Rise Time	—	19	29	ns	
t _{d(off)}	Turn-Off Delay Time	—	37	56	ns	
t _f	Fall Time	—	16	24	ns	
Q _g	Total Gate Charge (Gate-Source Pulse Gate-Drain)	—	18	30	nC	V _{GS} =10V, I _D =5.5A, V _{DS} =0.8Max. Rating (Gate charge is essentially independent of operating temperature.)
Q _{gs}	Gate-Source Charge	—	40	—	nC	
Q _{gd}	Gate-Drain ("Miller") Charge	—	14	—	nC	

THERMAL RESISTANCE

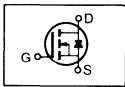
R _{thJC}	Junction-to-Case	Max	3.57	K/W	
R _{thCS}	Case-to-Sink	Typ	0.5	K/W	Mounting surface flat, Smooth, and greased
R _{thJA}	Junction-to-Ambient	Max	80	K/W	Free Air Operation

Notes: (1) T_J=25°C to 150°C

(2) Pulse test: Pulse width≤300μs, Duty Cycle≤2%

(3) Repetitive rating: Pulse width limited by max. junction temperature

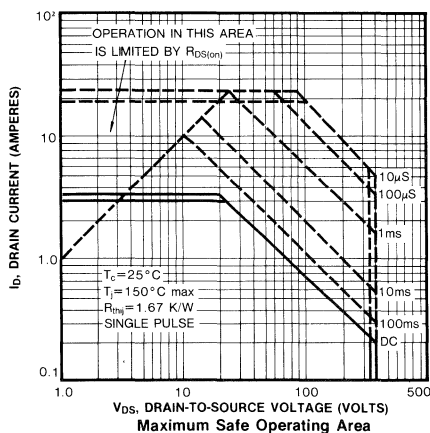
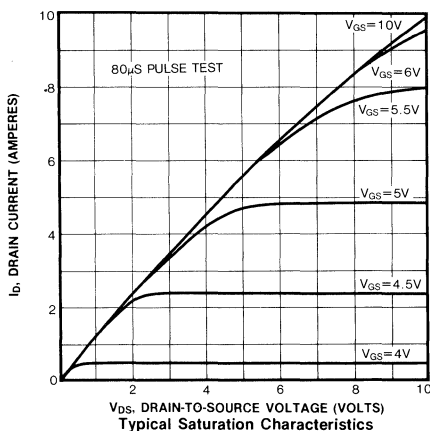
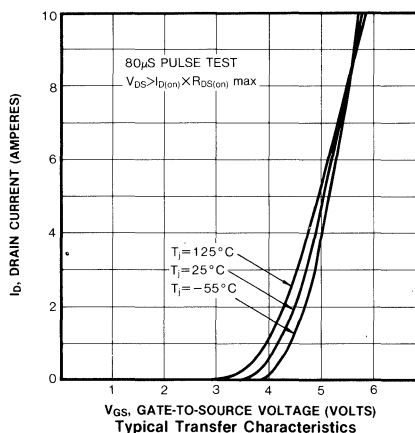
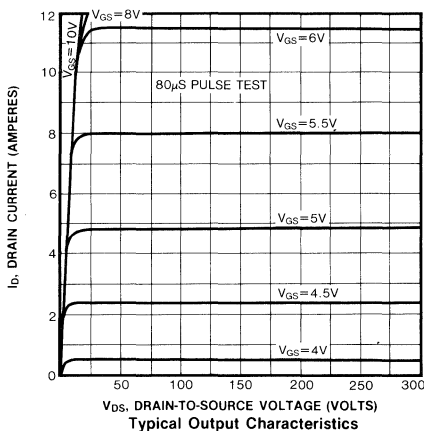
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

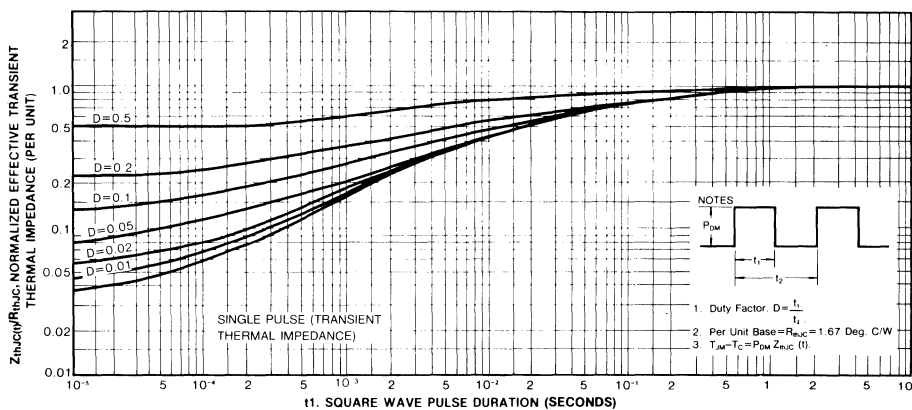
Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode) IRFS730/731 IRFS732/733	—	—	5.5 4.5	A	Modified MOSFET integral reverse P-N junction rectifier 
I_{SM}	Pulse Source Current (3) IRFS730/731 IRFS732/733	—	—	22 18	A	
V_{SD}	Diode Forward Voltage (2) IRFS730/731 IRFS732/733	—	—	1.8 1.6	V	$T_C=25^\circ\text{C}$, $I_S=5.5\text{A}$, $V_{GS}=0\text{V}$ $T_C=25^\circ\text{C}$, $I_S=4.5\text{A}$, $V_{GS}=0\text{V}$
t_{rr}	Reverse Recovery Time	—	310	660	ns	$T_J=25^\circ\text{C}$, $I_F=5.5\text{A}$, $dI_F/dt=100\text{A}/\mu\text{S}$

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C

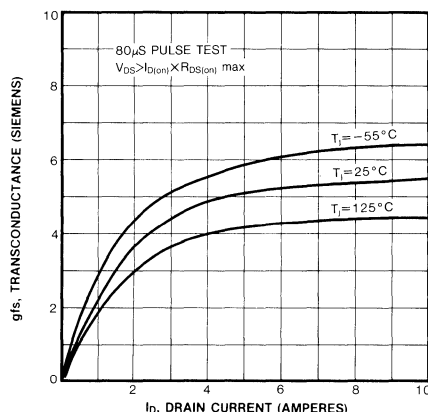
(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

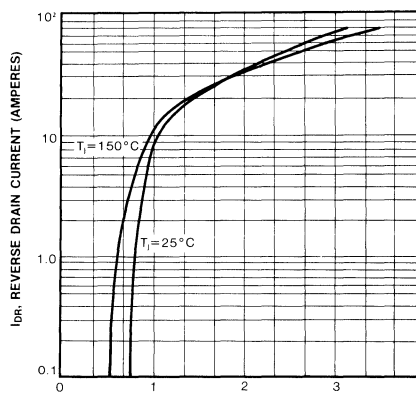




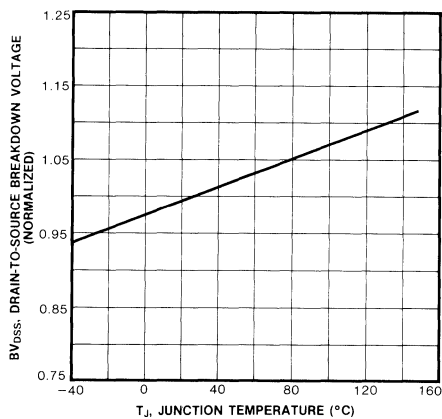
Maximum Effective Transient Thermal Impedance Junction-to-Case Vs. Pulse Duration



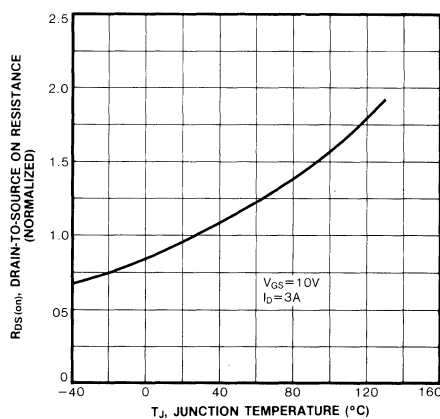
Typical Transconductance Vs. Drain Current



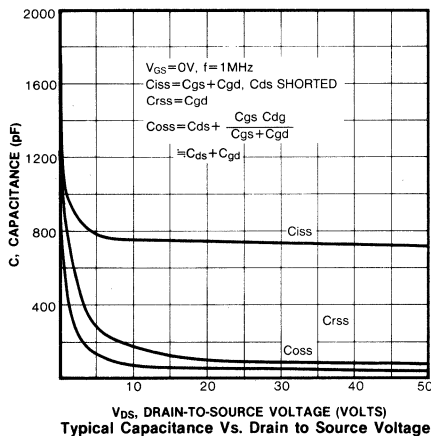
Typical Source-Drain Diode Forward Voltage



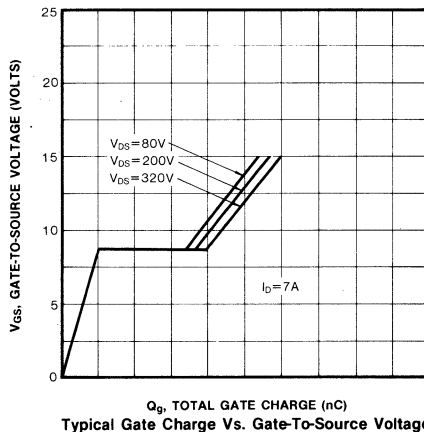
Breakdown Voltage Vs. Temperature



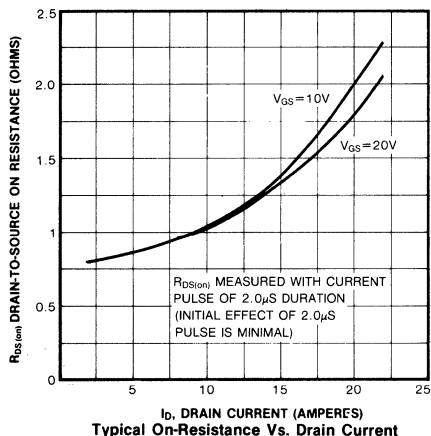
Normalized On-Resistance Vs. Temperature



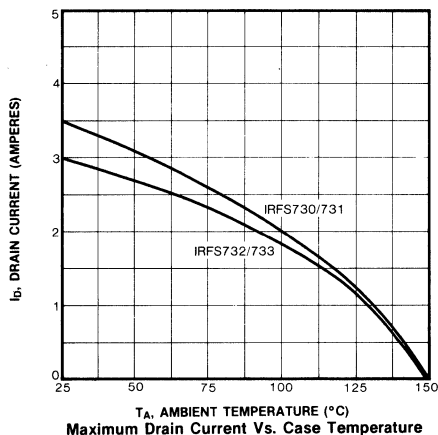
V_{DS}, DRAIN-TO-SOURCE VOLTAGE (VOLTS)
Typical Capacitance Vs. Drain to Source Voltage



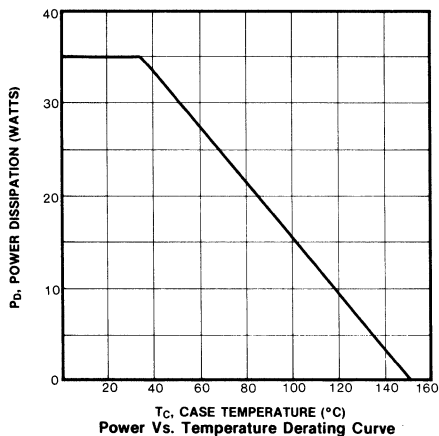
Q_g, TOTAL GATE CHARGE (nC)
Typical Gate Charge Vs. Gate-to-Source Voltage



I_D, DRAIN CURRENT (AMPERES)
Typical On-Resistance Vs. Drain Current



T_A, AMBIENT TEMPERATURE (°C)
Maximum Drain Current Vs. Case Temperature

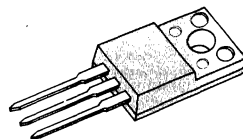


T_C, CASE TEMPERATURE (°C)
Power Vs. Temperature Derating Curve

FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

TO-220F



IRFS740/741/742/743

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFS740	400V	0.55Ω	5.5A
IRFS741	350V	0.55Ω	5.5A
IRFS742	400V	0.80Ω	4.5A
IRFS743	350V	0.80Ω	4.5A

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	IRFS740	IRFS741	IRFS742	IRFS743	Unit
Drain-Source Voltage (1)	V_{DSS}	400	350	400	350	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	400	350	400	350	Vdc
Gate-Source Voltage	V_{GS}	± 20				Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	5.5	5.5	4.5	4.5	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	3	3	2.5	2.5	Adc
Drain Current—Pulsed (3)	I_{DM}	40	40	33	33	Adc
Gate Current—Pulsed	I_{GM}	± 1.5				Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	157				mJ
Avalanche Current	I_{AS}	5.5				A
Total Power Dissipation at $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	40 0.32				Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150				$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300				$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=9.1mH$, $V_{dd}=50V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-Source Breakdown Voltage IRFS740/742 IRFS741/743	400 350	— —	— —	V	V _{GS} =0V, I _D =250μA
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} =V _{GS} , I _D =250μA
I _{GSS}	Gate-Source Leakage Forward	—	—	100	nA	V _{GS} =20V
I _{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	V _{GS} =-20V
I _{DSS}	Zero Gate Voltage Drain Current	— —	— —	250 1000	μA	V _{DS} =Max. Rating, V _{GS} =0V V _{DS} =0.8Max. Rating, T _C =125°C
I _{D(on)}	On-State Drain-Source Current (2) IRFS740/741 IRFS742/743	10 8.3	— —	— —	A	V _{DS} ≥8.8V, V _{GS} =10V
R _{DS(on)}	Static Drain-Source On-State Resistance (2) IRFS740/741 IRFS742/743	— —	— —	0.55 0.80	Ω	V _{GS} =10V, I _D =5.2A
g _{fs}	Forward Transconductance (2)	5.8	87	—	∅	V _{DS} ≥50V, I _D =5.2A
C _{iss}	Input Capacitance	—	1500	—	pF	V _{GS} =0V
C _{oss}	Output Capacitance	—	178	—	pF	V _{DS} =25V
C _{rss}	Reverse Transfer Capacitance	—	75	—	pF	f=1.0MHz
t _{d(on)}	Turn-On Delay Time	—	14	21	ns	V _{DD} =0.5 BV _{DSS} , I _D =10A, Z _O =9.1Ω (MOSFET switching times are essentially independent of operating temperature)
t _r	Rise Time	—	27	41	ns	
t _{d(off)}	Turn-Off Delay Time	—	50	75	ns	
t _f	Fall Time	—	24	36	ns	
Q _g	Total Gate Charge (Gate-Source Pulse Gate-Drain)	—	42	63	nC	V _{GS} =10V, I _D =10A, V _{DS} =0.8Max. Rating (Gate charge is essentially independent of operating temperature.)
Q _{gs}	Gate-Source Charge	—	6.0	9.0	nC	
Q _{gd}	Gate-Drain ("Miller") Charge	—	21	32	nC	

THERMAL RESISTANCE

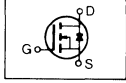
R _{thJC}	Junction-to-Case	Max	3.12	K/W	
R _{thCS}	Case-to-Sink	Typ	0.5	K/W	Mounting surface flat
R _{thJA}	Junction-to-Ambient	Max	80	K/W	Free Air Operation

Notes: (1) T_J=25°C to 150°C

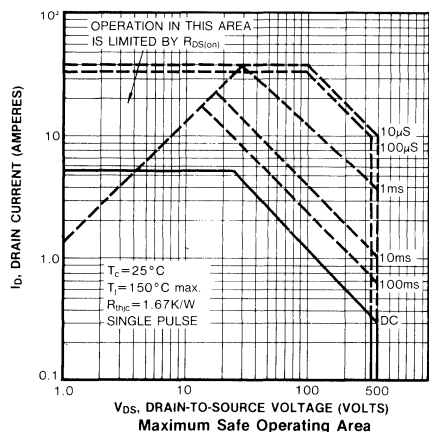
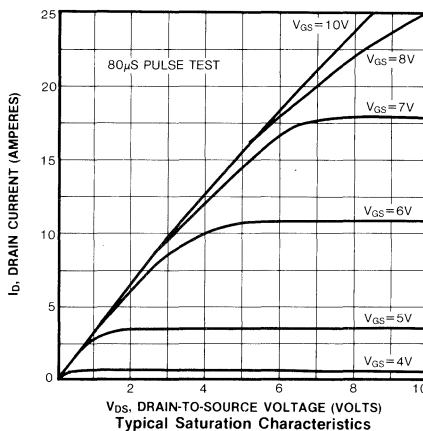
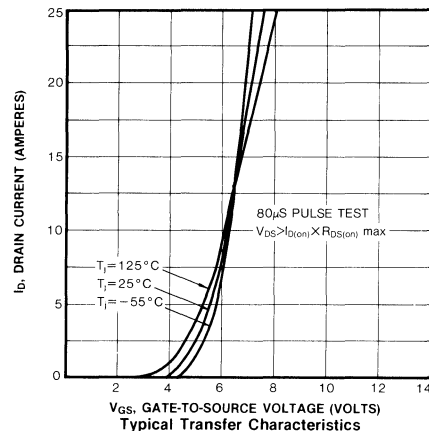
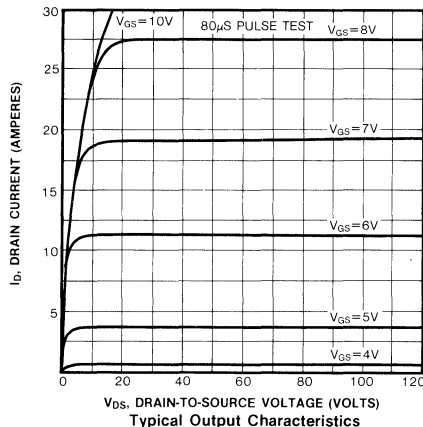
(2) Pulse test: Pulse width≤300μs, Duty Cycle≤2%

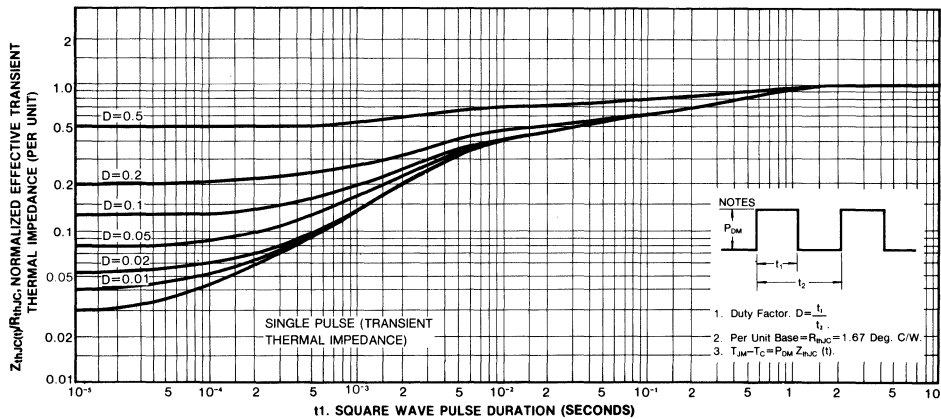
(3) Repetitive rating: Pulse width limited by max. junction temperature

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

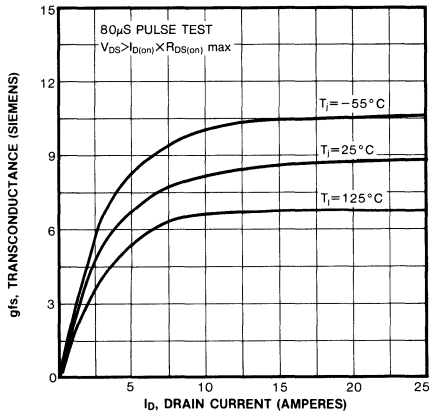
Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode) IRFS740/741 IRFS742/743	—	—	10 8	A	Modified MOSFET integral reverse P-N junction rectifier 
I_{SM}	Pulse Source Current (3) IRFS740/741 IRFS742/743	—	—	40 32	A	
V_{SD}	Diode Forward Voltage (2) IRFS740/741 IRFS742/743	—	—	2.0 1.9	V	$T_C = 25^\circ\text{C}$, $I_S = 10\text{A}$, $V_{GS} = 0\text{V}$ $T_C = 25^\circ\text{C}$, $I_S = 8\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	370	—	ns	$T_J = 25^\circ\text{C}$, $I_F = 10\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$

- Notes:** (1) $T_J = 25^\circ\text{C}$ to 150°C
(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature

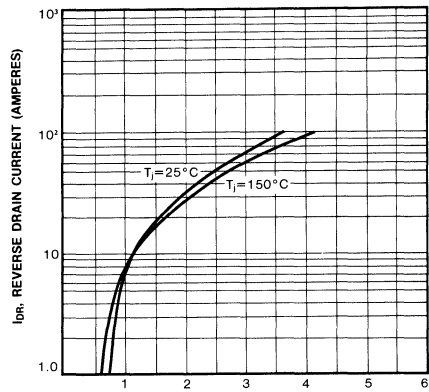




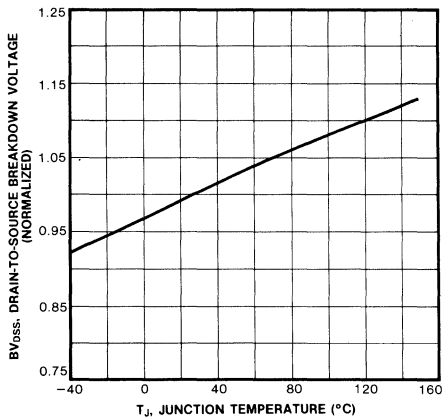
11. SQUARE WAVE PULSE DURATION (SECONDS)
Maximum Effective Transient Thermal Impedance Junction-to-Case Vs. Pulse Duration



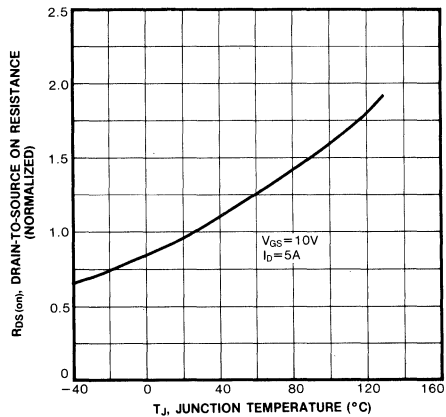
Typical Transconductance Vs. Drain Current



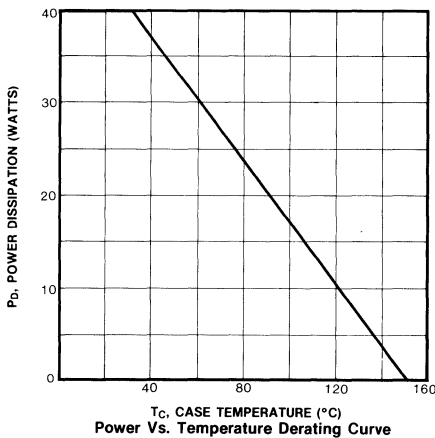
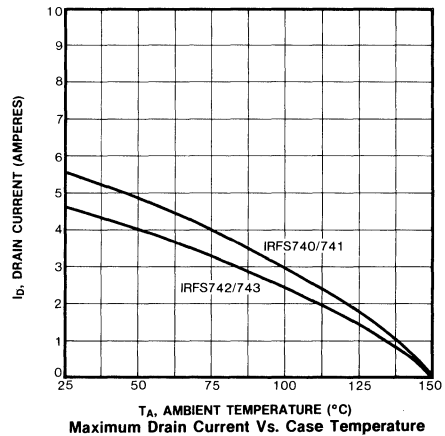
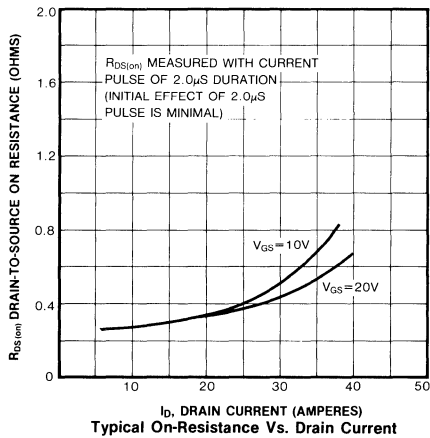
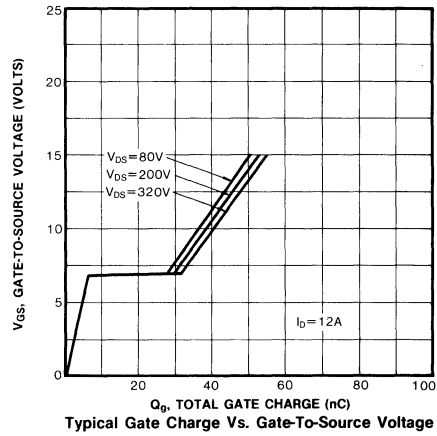
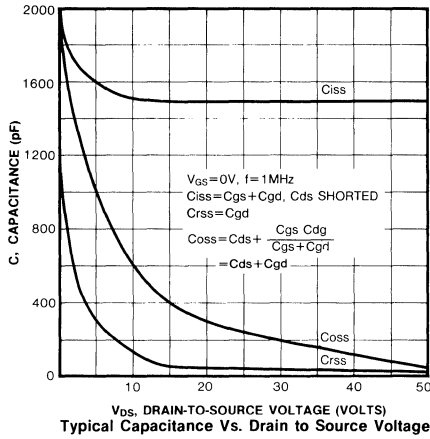
Typical Source-Drain Diode Forward Voltage



Breakdown Voltage Vs. Temperature



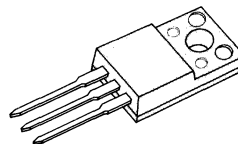
Normalized On-Resistance Vs. Temperature



FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

TO-220F



IRFS830/831/832/833

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFS830	500V	1.5 Ω	3.0A
IRFS831	450V	1.5 Ω	3.0A
IRFS832	500V	2.0 Ω	2.5A
IRFS833	450V	2.0 Ω	2.5A

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	IRFS830	IRFS831	IRFS832	IRFS833	Unit
Drain-Source Voltage (1)	V_{DSS}	500	450	500	450	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	500	450	500	450	Vdc
Gate-Source Voltage	V_{GS}	± 20				Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	3.0	3.0	2.5	2.5	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	1.8	1.8	1.5	1.5	Adc
Drain Current—Pulsed (3)	I_{DM}	18	18	16	16	Adc
Gate Current—Pulsed	I_{GM}	± 1.5				Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	124				mJ
Avalanche Current	I_{AS}	3.0				A
Total Power Dissipation at $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	35 0.28				Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150				$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300				$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=25mH$, $V_{dd}=50V$, $R_G=25\Omega$, starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-Source Breakdown Voltage IRFS830/832 IRFS831/833	500 450	— —	— —	V	V _{GS} =0V, I _D =250μA
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} =V _{GS} , I _D =250μA
I _{GSS}	Gate-Source Leakage Forward	—	—	100	nA	V _{GS} =20V
I _{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	V _{GS} =-20V
I _{DSS}	Zero Gate Voltage Drain Current	— —	— —	250 1000	μA	V _{DS} =Max. Rating, V _{GS} =0V V _{DS} =0.8Max. Rating, T _C =125°C
I _{D(on)}	On-State Drain-Source Current (2) IRFS830/831 IRFS832/833	4.5 4.0	— —	— —	A	V _{DS} ≥9.0V, V _{GS} =10V
R _{DS(on)}	Static Drain-Source On-State Resistance (2) IRFS830/831 IRFS832/833	— —	0.95 1.4	1.5 2.0	Ω	V _{GS} =10V, I _D =2.5A
g _{fs}	Forward Transconductance (2)	2.5	3.2	—	Ω	V _{DS} ≥50V, I _D =2.5A
C _{iss}	Input Capacitance	—	780	—	pF	V _{GS} =0V
C _{oss}	Output Capacitance	—	86	—	pF	V _{DS} =25V
C _{rss}	Reverse Transfer Capacitance	—	38	—	pF	f=1.0MHz
t _{d(on)}	Turn-On Delay Time	—	11	17	ns	V _{DD} =0.5 BV _{DSS} , I _D =4.5A, Z _O =12Ω (MOSFET switching times are essentially independent of operating temperature)
t _r	Rise Time	—	15	23	ns	
t _{d(off)}	Turn-Off Delay Time	—	35	53	ns	
t _f	Fall Time	—	15	23	ns	
Q _g	Total Gate Charge (Gate-Source Pulse Gate-Drain)	—	21	32	nC	V _{GS} =10V, I _D =4.5A, V _{DS} =0.8Max. Rating (Gate charge is essentially independent of operating temperature.)
Q _{gs}	Gate-Source Charge	—	3.2	4.8	nC	
Q _{gd}	Gate-Drain ("Miller") Charge	—	11	17	nC	

THERMAL RESISTANCE

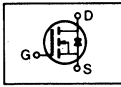
R _{thJC}	Junction-to-Case	MAX	3.57	K/W	
R _{thCS}	Case-to-Sink	TYP	0.5	K/W	Mounting surface flat, Smooth, and greased
R _{thJA}	Junction-to-Ambient	MAX	80	K/W	Free Air Operation

Notes: (1) T_J=25°C to 150°C

(2) Pulse test: Pulse width≤300μs, Duty Cycle≤2%

(3) Repetitive rating: Pulse width limited by max. junction temperature

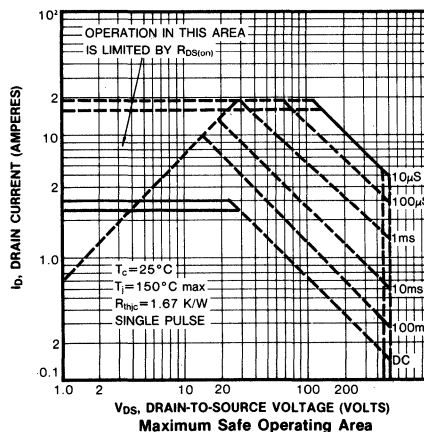
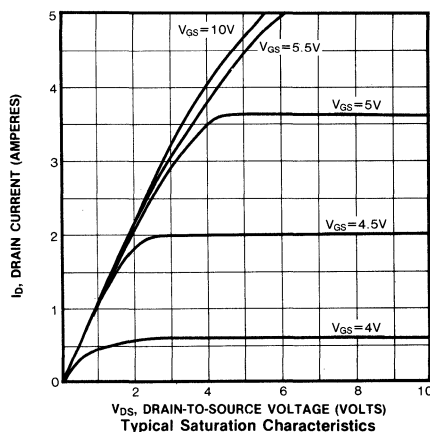
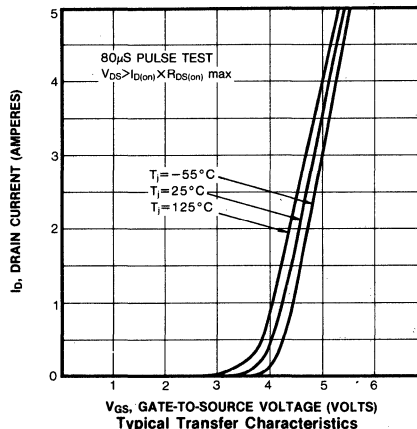
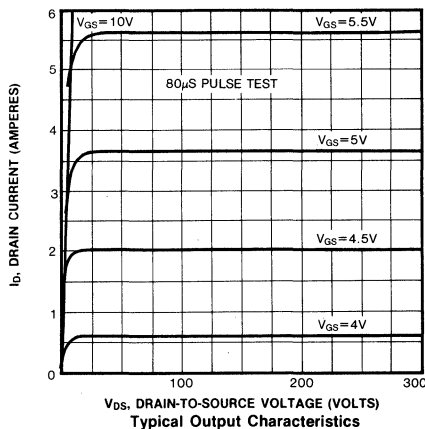
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

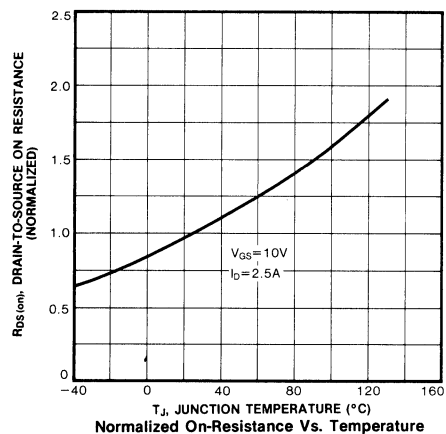
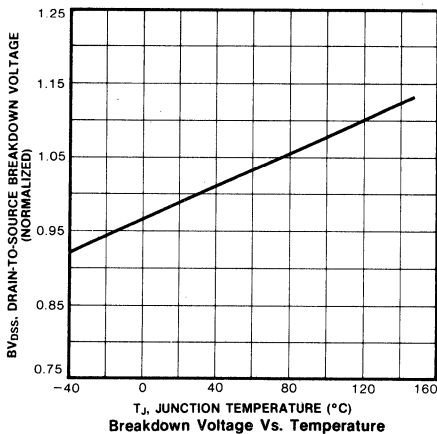
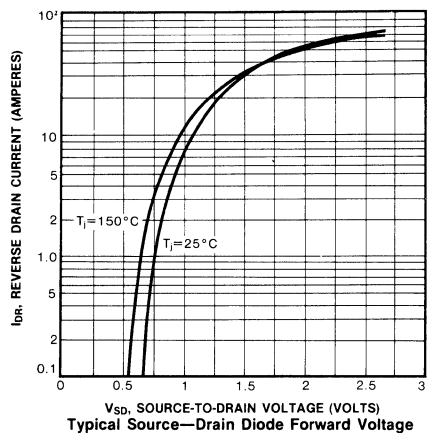
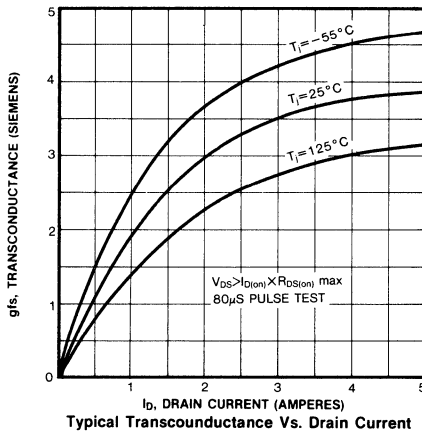
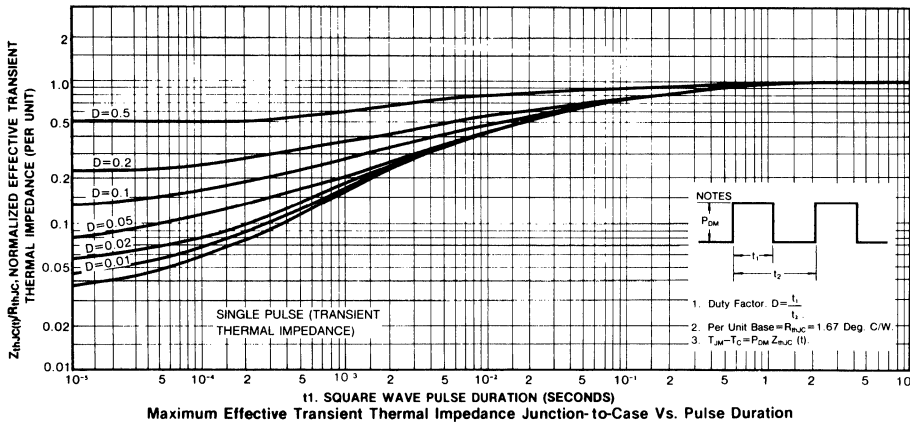
Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode) IRFS830/831 IRFS832/833	—	—	4.5 4.0	A	Modified MOSFET integral reverse P-N junction rectifier 
I_{SM}	Pulse Source Current (3) IRFS830/831 IRFS832/833	—	—	18 16	A	
V_{SD}	Diode Forward Voltage (2) IRFS830/831 IRFS832/833	—	—	1.6 1.5	V	$T_C = 25^\circ\text{C}$, $I_S = 4.5\text{A}$, $V_{GS} = 0\text{V}$ $T_C = 25^\circ\text{C}$, $I_S = 4.0\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	370	760	ns	$T_J = 25^\circ\text{C}$, $I_F = 4.5\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{s}$

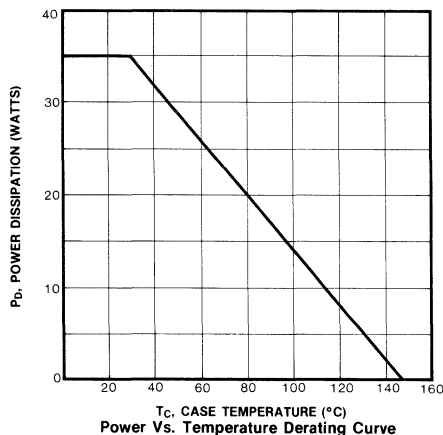
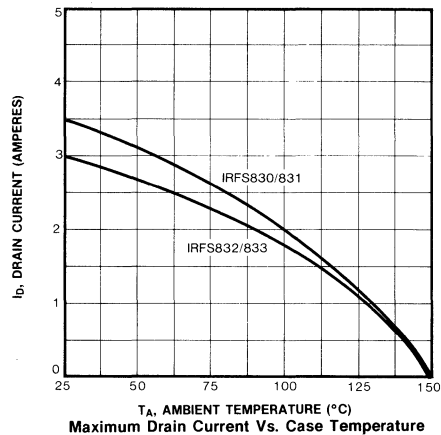
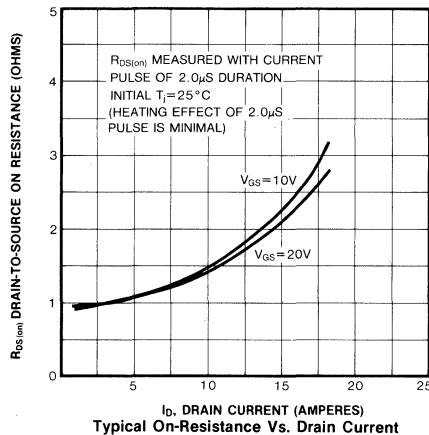
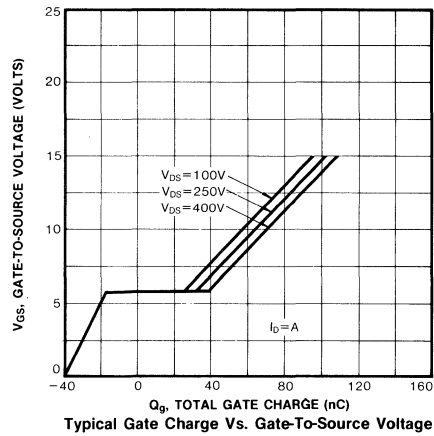
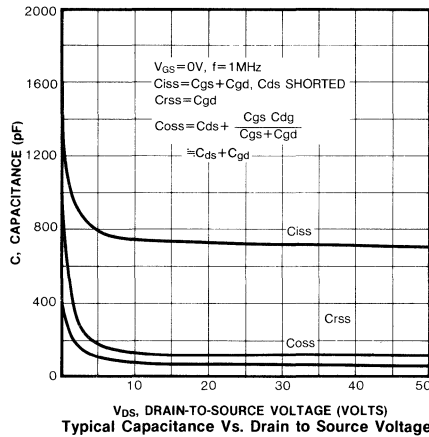
Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C

(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature



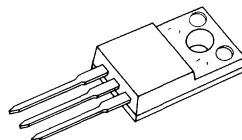




FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

TO-220F



IRFS840/841/842/843

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFS840	500V	$0.85\ \Omega$	4.5A
IRFS841	450V	$0.85\ \Omega$	4.5A
IRFS842	500V	$1.1\ \Omega$	4.0A
IRFS843	450V	$1.1\ \Omega$	4.0A

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	IRFS840	IRFS841	IRFS842	IRFS843	Unit
Drain-Source Voltage (1)	V_{DSS}	500	450	500	450	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	500	450	500	450	Vdc
Gate-Source Voltage	V_{GS}	± 20				Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	4.5	4.5	4.0	4.0	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	2.8	2.8	2.5	2.5	Adc
Drain Current—Pulsed (3)	I_{DM}	32	32	28	28	Adc
Gate Current—Pulsed	I_{GM}	± 1.5				Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	161				mJ
Avalanche Current	I_{AS}	4.5				A
Total Power Dissipation at $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	40 0.32				Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150				$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300				$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=14mH$, $V_{dd}=50V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-Source Breakdown Voltage IRFS840/842 IRFS841/843	500 450	— —	— —	V	V _{GS} =0V, I _D =250μA
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} =V _{GS} , I _D =250μA
I _{GSS}	Gate-Source Leakage Forward	—	—	100	nA	V _{GS} =20V
I _{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	V _{GS} =-20V
I _{DSS}	Zero Gate Voltage Drain Current	— —	— —	250 1000	μA	V _{DS} =Max. Rating, V _{GS} =0V V _{DS} =0.8Max. Rating, T _C =125°C
I _{D(on)}	On-State Drain-Source Current (2) IRFS840/841 IRFS842/843	8 7	— —	— —	A	V _{DS} ≥8.8V, V _{GS} =10V
R _{DS(on)}	Static Drain-Source On-State Resistance (2) IRFS840/841 IRFS842/843	— —	0.76 0.85	0.85 1.10	Ω	V _{GS} =10V, I _D =4A
g _{fs}	Forward Transconductance (2)	4.0	6.5	—	∩	V _{DS} ≥50V, I _D =4A
C _{iss}	Input Capacitance	—	1510	—	pF	V _{GS} =0V
C _{oss}	Output Capacitance	—	154	—	pF	V _{DS} =25V
C _{rss}	Reverse Transfer Capacitance	—	66	—	pF	f=1.0MHz
t _{d(on)}	Turn-On Delay Time	—	14	21	ns	V _{DD} =0.5 BV _{DSS} , I _D =8A, Z _O =19ohm (MOSFET switching times are essentially independent of operating temperature)
t _r	Rise Time	—	23	35	ns	
t _{d(off)}	Turn-Off Delay Time	—	49	74	ns	
t _f	Fall Time	—	20	30	ns	
Q _g	Total Gate Charge (Gate-Source Pulse Gate-Drain)	—	42	63	nC	V _{GS} =10V, I _D =8A, V _{DS} =0.8Max. Rating (Gate charge is essentially independent of operating temperature.)
Q _{gs}	Gate-Source Charge	—	6.2	9.3	nC	
Q _{gd}	Gate-Drain ("Miller") Charge	—	22	32	nC	

THERMAL RESISTANCE

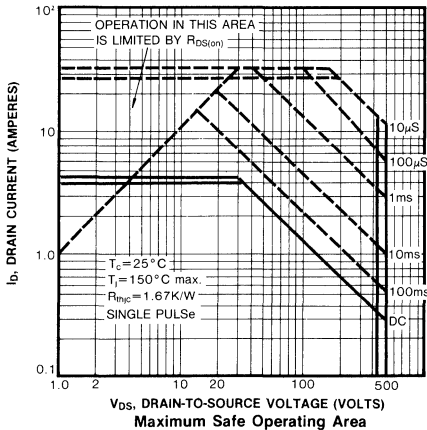
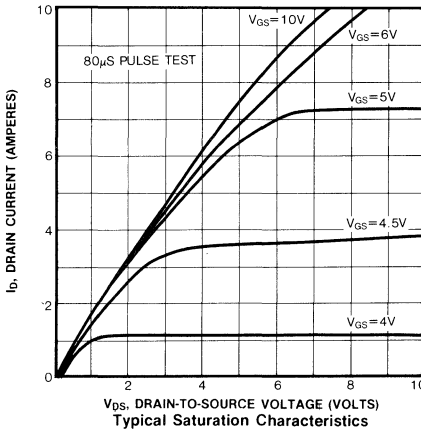
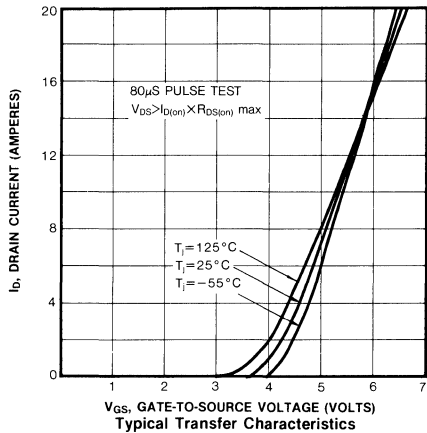
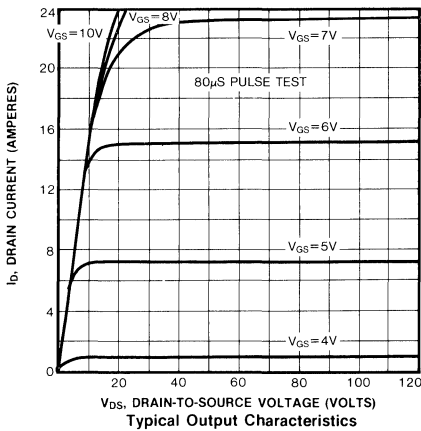
R _{thJC}	Junction-to-Case	MAX	3.12	K/W	
R _{thCS}	Case-to-Sink	TYP	0.5	K/W	Mounting surface flat, Smooth, and greased
R _{thJA}	Junction-to-Ambient	MAX	80	K/W	Free Air Operation

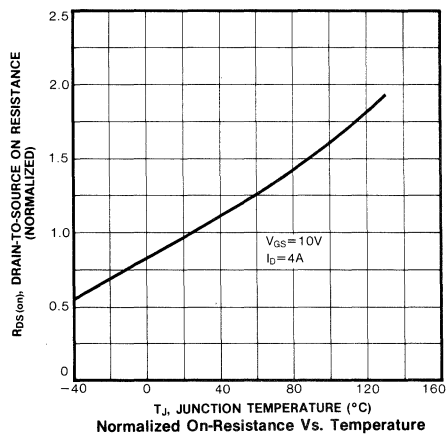
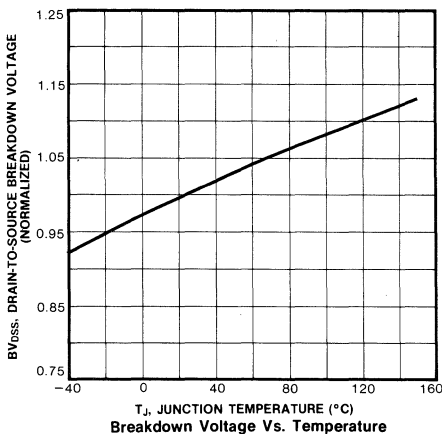
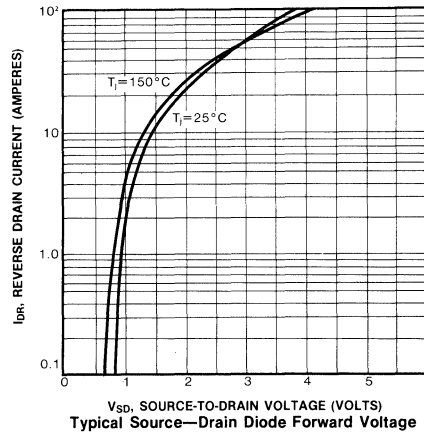
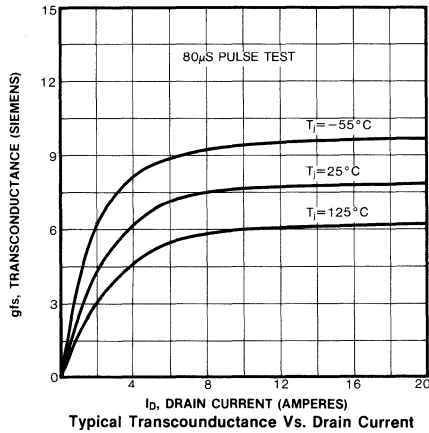
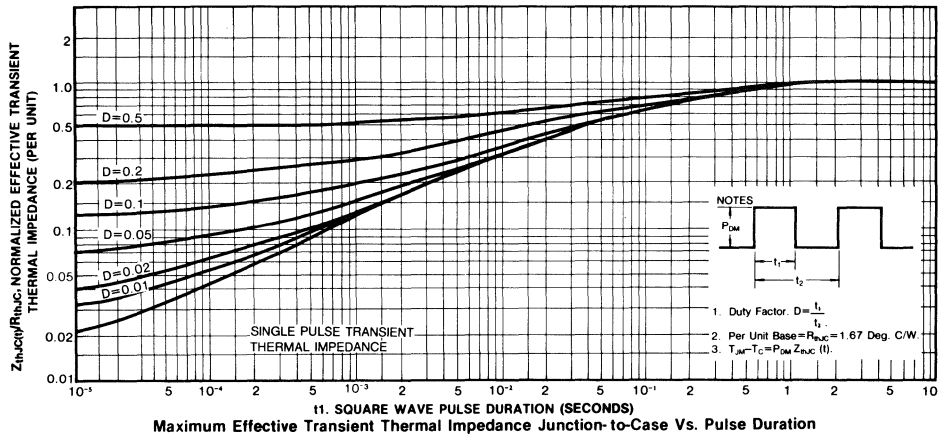
- Notes:** (1) T_J=25°C to 150°C
(2) Pulse test: Pulse width≤300μs, Duty Cycle≤2%
(3) Repetitive rating: Pulse width limited by max. junction temperature

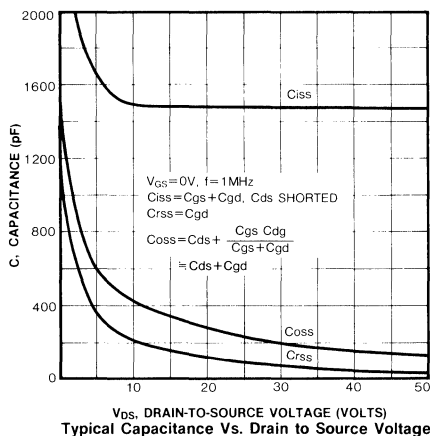
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode) IRFS840/841 IRFS842/843	—	—	8 7	A	Modified MOSFET integral reverse P-N junction rectifier
I_{SM}	Pulse Source Current (3) IRFS840/841 IRFS842/843	—	—	32 28	A	
V_{SD}	Diode Forward Voltage (2) IRFS840/841 IRFS842/843	—	—	2.0 1.9	V	$T_C = 25^\circ\text{C}$, $I_S = 8\text{A}$, $V_{GS} = 0\text{V}$ $T_C = 25^\circ\text{C}$, $I_S = 7\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	460	970	ns	$T_J = 25^\circ\text{C}$, $I_F = 10\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$

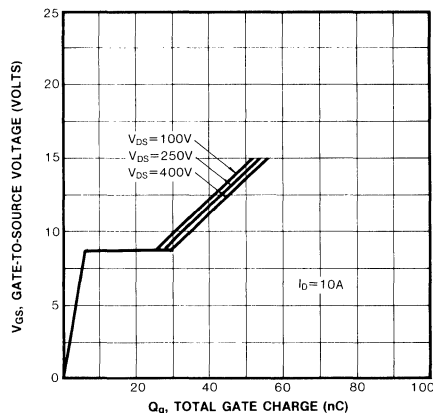
Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C
(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature



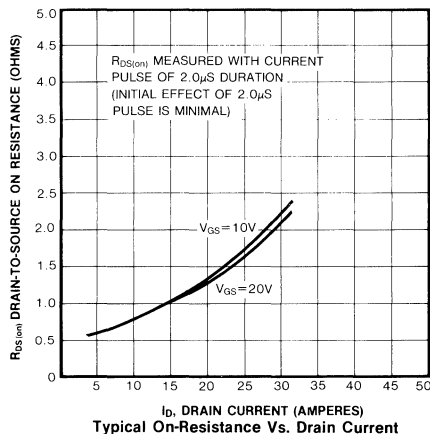




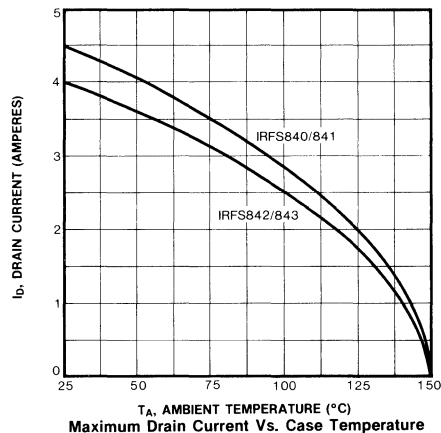
Typical Capacitance Vs. Drain to Source Voltage



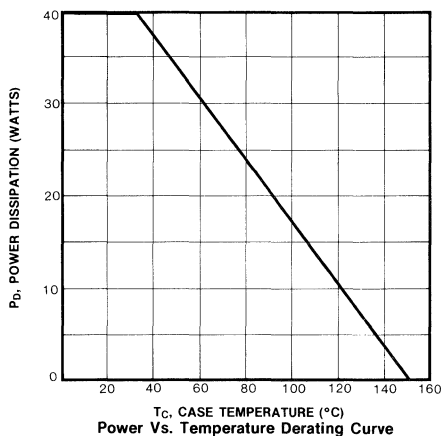
Typical Gate Charge Vs. Gate-To-Source Voltage



Typical On-Resistance Vs. Drain Current



Maximum Drain Current Vs. Case Temperature

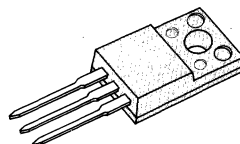


Power Vs. Temperature Derating Curve

FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

TO-220F



IRFS9540/9541/9542/9543

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFS9540	-100V	0.20 Ω	-10.7A
IRFS9541	-60V	0.20 Ω	-10.7A
IRFS9542	-100V	0.30 Ω	-8.4A
IRFS9543	-60V	0.30 Ω	-8.4A

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	IRFS9540	IRFS9541	IRFS9542	IRFS9543	Unit
Drain-Source Voltage (1)	V_{DS}	-100	-60	-100	-60	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	-100	-60	-100	-60	Vdc
Gate-Source Voltage	V_{GS}	± 20				Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	-10.7	-10.7	-8.4	-8.4	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	-8.1	-8.1	-6.4	-6.4	Adc
Drain Current—Pulsed (3)	I_{DM}	-76	-76	-60	-60	Adc
Gate Current—Pulsed	I_{GM}	± 1.5				Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	170				mJ
Avalanche Current	I_{AS}	-10.7				A
Total Power Dissipation at $T_C=25^\circ C$	P_D	40				Watts
Derate above $25^\circ C$		0.32				W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150				$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300				$^\circ C$

- Notes:** (1) $T_J=25^\circ C$ to $150^\circ C$
 (2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
 (3) Repetitive rating: Pulse with limited by max. junction temperature
 (4) $L=3.5mH$, $V_{dd}=-25V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage IRFS9540/9542 IRFS9541/9543	-100 -60	— —	— —	V	$V_{GS}=0V$, $I_D=-250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	$V_{DS}=V_{GS}$, $I_D=-250\mu A$
I_{GSS}	Gate-Source Leakage Forward	—	—	-100	nA	$V_{GS}=-20V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	100	nA	$V_{GS}=20V$
I_{DSS}	Zero Gate Voltage Drain Current	— —	— —	250 1000	μA	$V_{DS}=\text{Max. Rating}$, $V_{GS}=0V$ $V_{DS}=0.8\text{Max. Rating}$, $T_C=125^\circ\text{C}$, $V_{GS}=0V$
$I_{D(on)}$	On-State Drain-Source Current (2) IRFS9540/9541 IRFS9542/9543	-19 -15	— —	— —	A	$V_{DS}\leq-5.7V$, $V_{GS}=-10V$
$R_{DS(on)}$	Static Drain-Source On-State Resistance (2) IRFS9540/9541 IRFS9542/9543	— —	0.15 —	0.2 0.3	Ω	$V_{GS}=-10V$, $I_D=-10A$
g_{fs}	Forward Transconductance (2)	5.0	—	—	μ	$V_{DS}\leq-10V$, $I_D=-10A$
C_{iss}	Input Capacitance	—	1560	—	pF	$V_{GS}=0V$
C_{oss}	Output Capacitance	—	240	—	pF	$V_{DS}=-25V$
C_{rss}	Reverse Transfer Capacitance	—	120	—	pF	$f=1.0\text{MHz}$
$t_{d(on)}$	Turn-On Delay Time	—	10	30	ns	$V_{DD}=-50V$, $I_D=-10A$, $Z_O=4.7\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	15	15	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	20	20	ns	
t_f	Fall Time	—	12	12	ns	
Q_g	Total Gate Charge (Gate-Source Pulse Gate-Drain)	—	—	90	nC	$V_{GS}=-15V$, $I_D=-19A$, $V_{DS}=0.8\text{Max. Rating}$ (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	—	30	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	—	60	nC	

THERMAL RESISTANCE

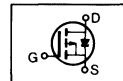
R_{thJC}	Junction-to-Case	MAX	3.12	K/W	
R_{thCS}	Case-to-Sink	TYP	0.5	K/W	Mounting surface flat, Smooth, and greased
R_{thJA}	Junction-to-Ambient	MAX	80	K/W	Free Air Operation

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse width limited by max. junction temperature

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

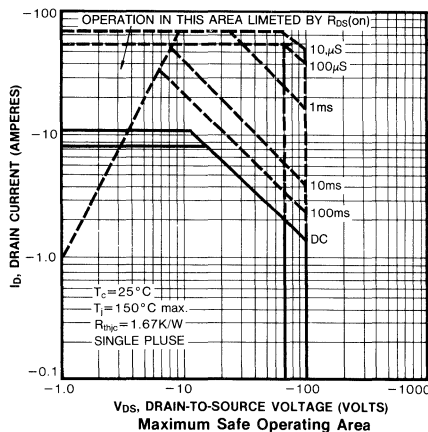
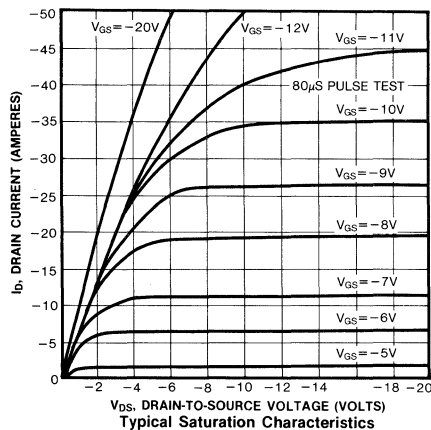
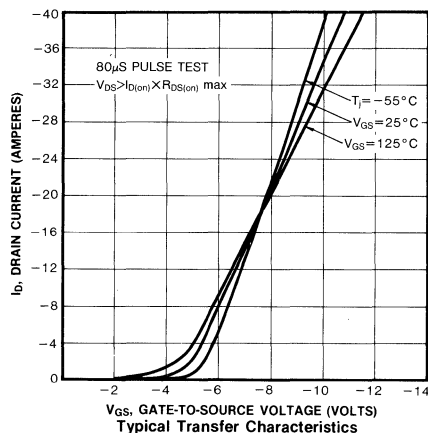
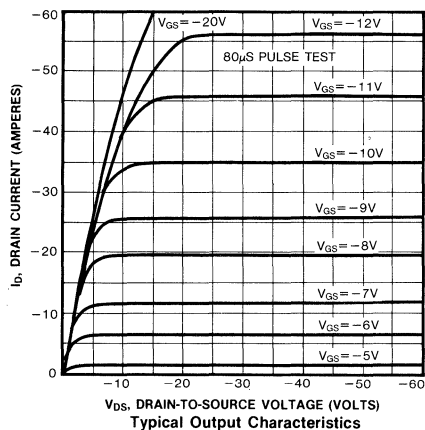
Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode) IRFS9540/9541 IRFS9542/9543	—	—	-19 -15	A	Modified MOSFET integral reverse P-N junction rectifier
I_{SM}	Pulse Source Current (3) IRFS9540/9541 IRFS9542/9543	—	—	-75 -60	A	
V_{SD}	Diode Forward Voltage (2) IRFS9540/9541 IRFS9542/9543	—	—	-4.2 -4.0	V	$T_C = 25^\circ\text{C}$, $I_S = -19\text{A}$, $V_{GS} = 0\text{V}$ $T_C = 25^\circ\text{C}$, $I_S = -15\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	170	—	ns	$T_J = 25^\circ\text{C}$, $I_F = -19\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$

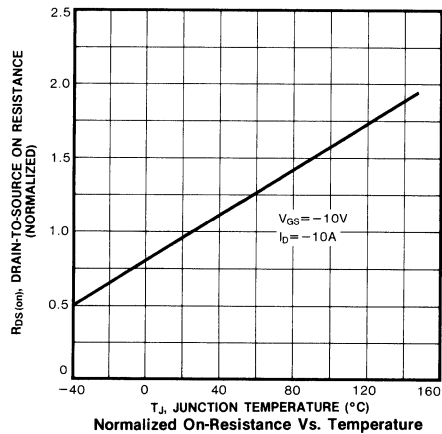
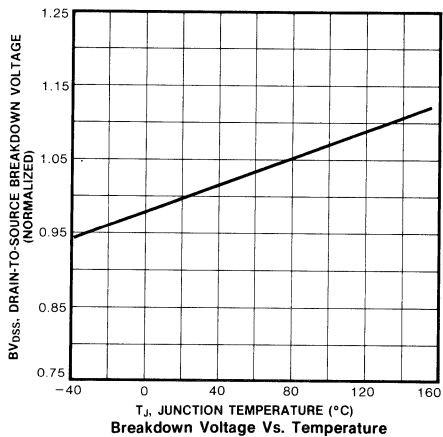
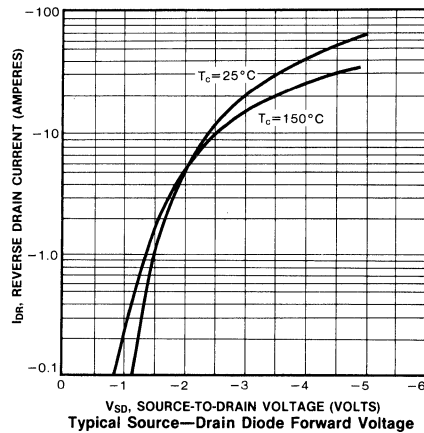
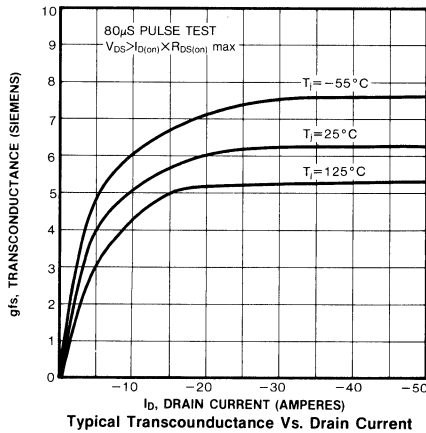
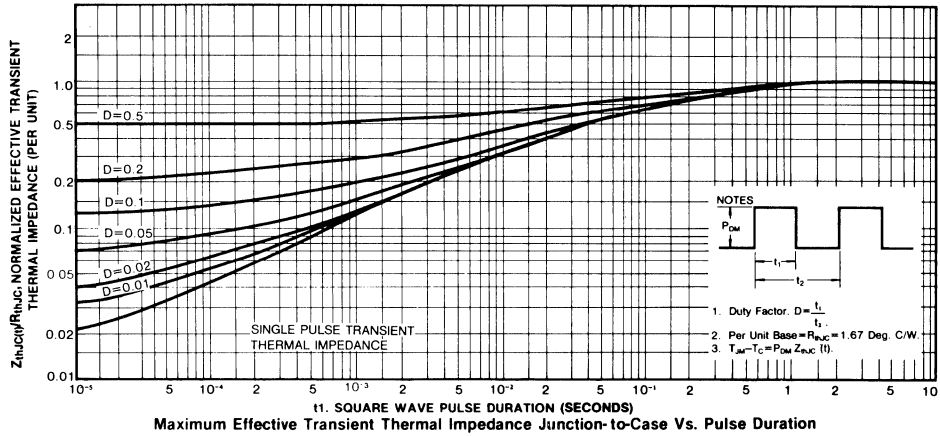


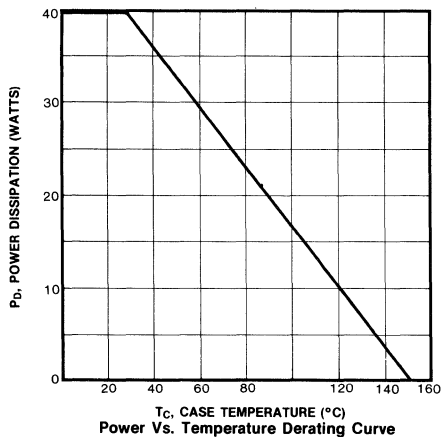
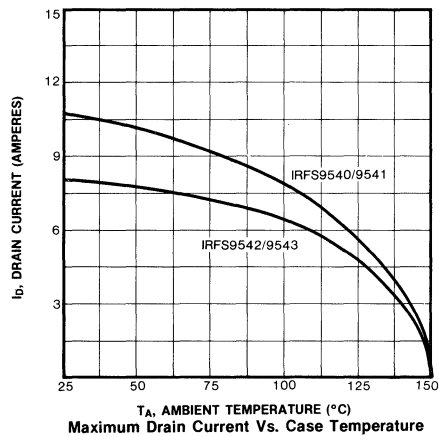
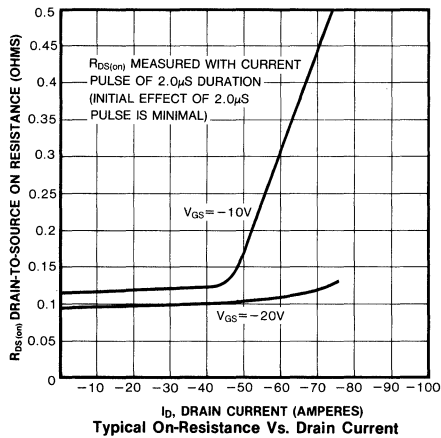
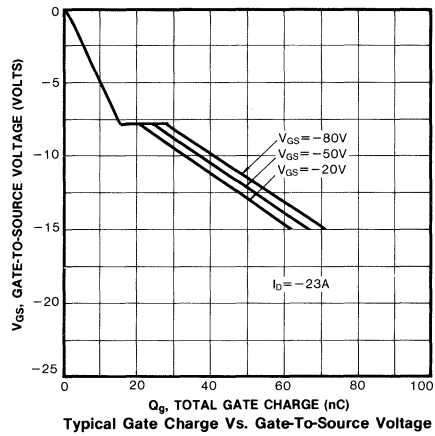
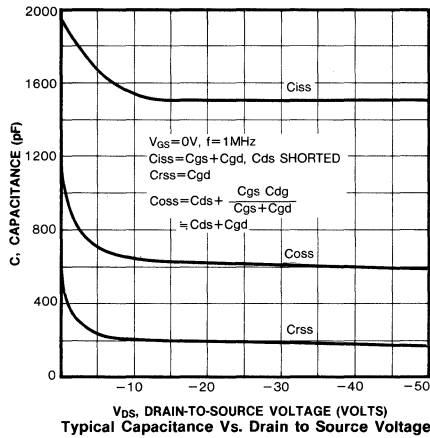
Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C

(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

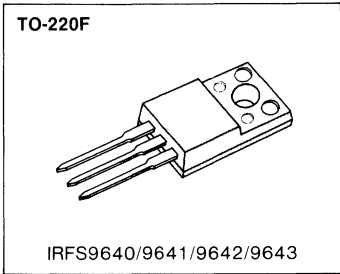






FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability



PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFS9640	-200V	0.50 Ω	-6.2A
IRFS9641	-150V	0.50 Ω	-6.2A
IRFS9642	-200V	0.70 Ω	-5.0A
IRFS9643	-150V	0.70 Ω	-5.0A

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	IRFS9640	IRFS9641	IRFS9642	IRFS9643	Unit
Drain-Source Voltage (1)	V_{DSS}	-100	-60	-100	-60	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	-100	-60	-100	-60	Vdc
Gate-Source Voltage	V_{GS}	± 20				Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	-6.2	-6.2	-5.0	-5.0	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	-4.7	-4.7	-3.8	-3.8	Adc
Drain Current—Pulsed (3)	I_{DM}	-44	-44	-36	-36	Adc
Gate Current—Pulsed	I_{GM}	± 1.5				Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	120				mJ
Avalanche Current	I_{AS}	-6.2				A
Total Power Dissipation at $T_C=25^\circ C$	P_D	40				Watts
Derate above $25^\circ C$		0.32				W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150				$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300				$^\circ C$

- Notes: (1) $T_J=25^\circ C$ to $150^\circ C$
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature
(4) $L=7mH$, $V_{dd}=-50V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage IRFS9640/9642 IRFS9641/9643	-200 -150	— —	— —	V	$V_{GS}=0V$, $I_D = -250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	$V_{DS}=V_{GS}$, $I_D = -250\mu A$
I_{GSS}	Gate-Source Leakage Forward	—	—	-100	nA	$V_{GS} = -20V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	100	nA	$V_{GS} = 20V$
I_{DSS}	Zero Gate Voltage Drain Current	— —	— —	250 1000	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS}=0V$ $V_{DS}=0.8\text{Max. Rating}$, $T_C=125^\circ\text{C}$, $V_{GS}=0V$
$I_{D(on)}$	On-State Drain-Source Current (2) IRFS9640/9641 IRFS9642/9643	-11 -9	— —	— —	A	$V_{DS} \leq -7.7V$, $V_{GS} = -10V$
$R_{DS(on)}$	Static Drain-Source On-State Resistance (2) IRFS9640/9641 IRFS9642/9643	— —	0.44 0.5	0.5 0.7	Ω	$V_{GS} = -10V$, $I_D = -6.0A$
g_{fs}	Forward Transconductance (2)	4.0	—	—	μ	$V_{DS} = -10V$, $I_D = -6.0A$
C_{iss}	Input Capacitance	—	1542	—	pF	$V_{GS}=0V$
C_{oss}	Output Capacitance	—	230	—	pF	$V_{DS} = -25V$
C_{rss}	Reverse Transfer Capacitance	—	115	—	pF	$f=1.0\text{MHz}$
$t_{d(on)}$	Turn-On Delay Time	—	—	30	ns	$V_{DD} = -100V$, $I_D = -6.0A$, $Z_O=4.7\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	—	15	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	—	18	ns	
t_f	Fall Time	—	—	12	ns	
Q_g	Total Gate Charge (Gate-Source Pulse Gate-Drain)	—	—	90	nC	$V_{GS} = -15V$, $I_D = -11A$, $V_{DS}=0.8\text{Max. Rating}$ (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	—	30	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	—	60	nC	

THERMAL RESISTANCE

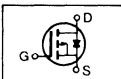
R_{thJC}	Junction-to-Case	MAX	3.12	K/W	
R_{thCS}	Case-to-Sink	TYP	0.5	K/W	Mounting surface flat smooth, and greased
R_{thJA}	Junction-to-Ambient	MAX	80	K/W	Free Air Operation

Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse width limited by max. junction temperature

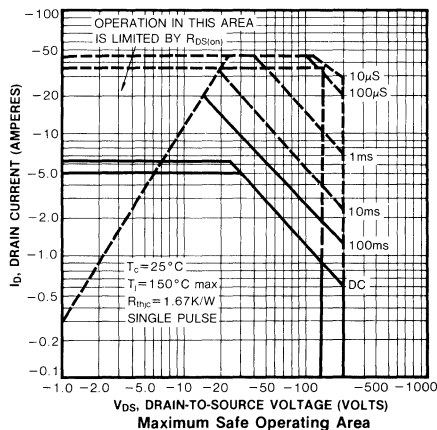
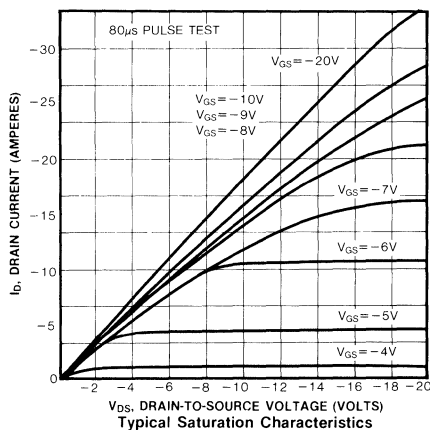
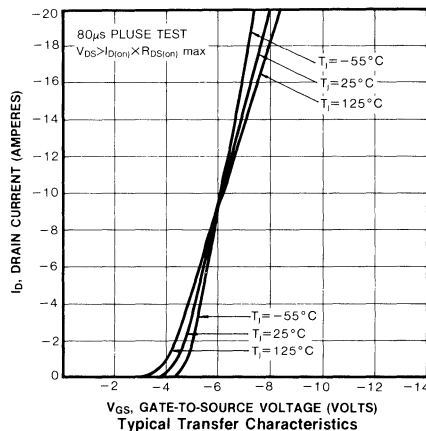
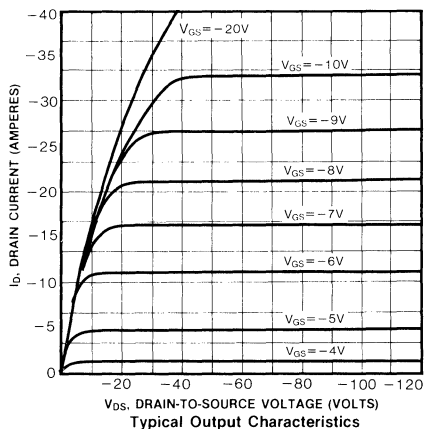
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

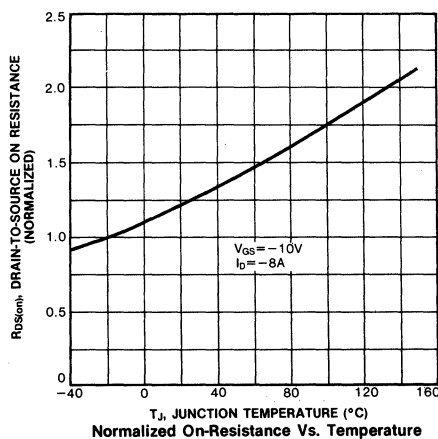
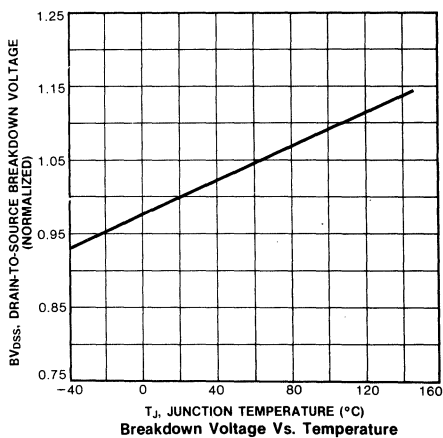
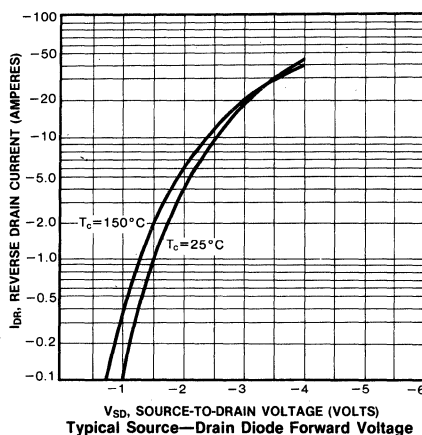
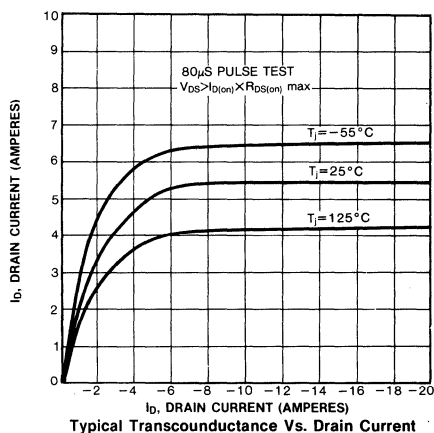
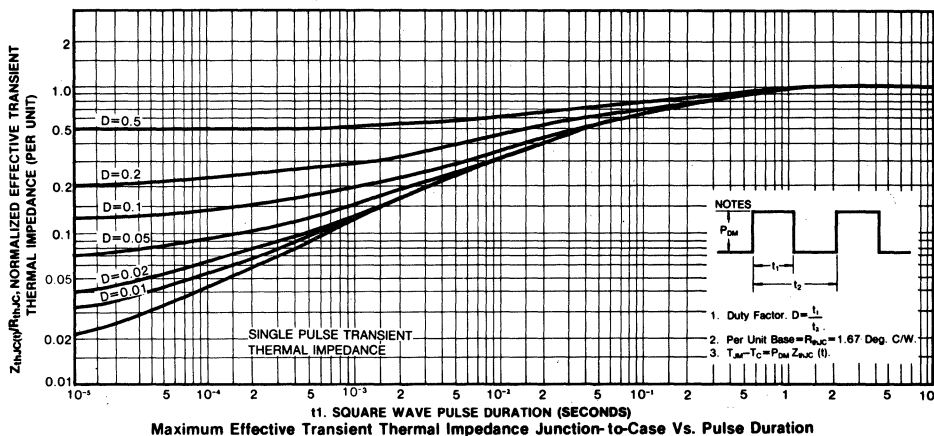
Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode) IRFS9640/9641 IRFS9642/9643	—	—	-11 -9	A	Modified MOSFET integral reverse P-N junction rectifier 
I_{SM}	Pulse Source Current (3) IRFS9640/9641 IRFS9642/9643	—	—	-44 -36	A	
V_{SD}	Diode Forward Voltage (2) IRFS9640/9641 IRFS9642/9643	—	—	-4.6 -4.4	V	$T_C = 25^\circ\text{C}$, $I_S = -11\text{A}$, $V_{GS} = 0\text{V}$ $T_C = 25^\circ\text{C}$, $I_S = -9\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	270	—	ns	$T_J = 25^\circ\text{C}$, $I_F = -11\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$

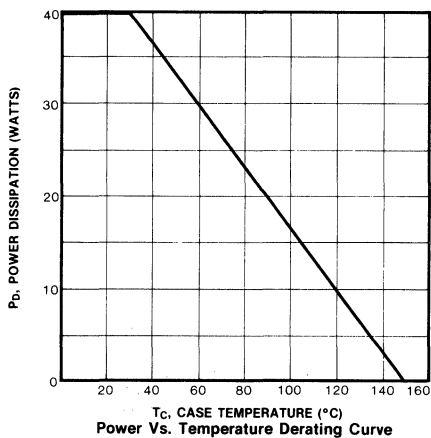
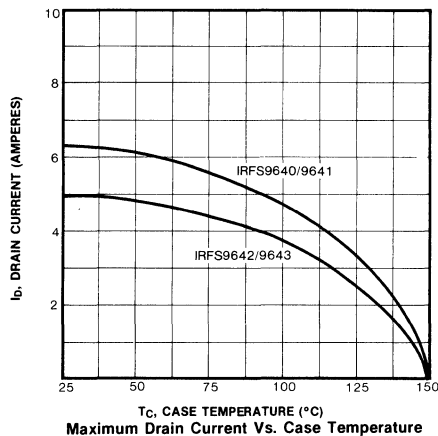
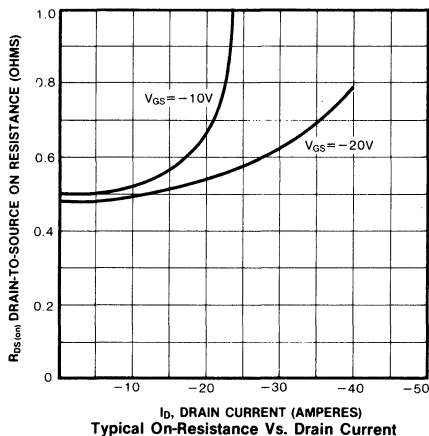
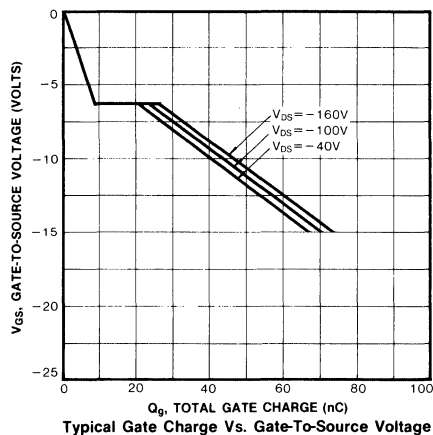
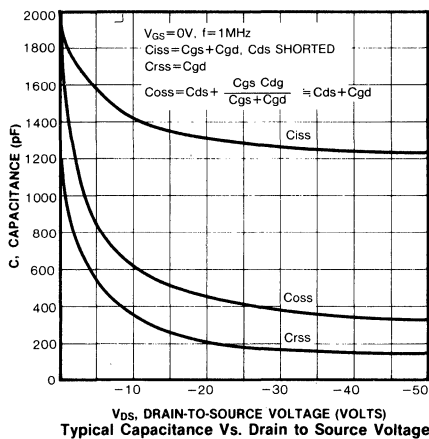
Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C

(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature







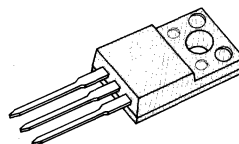
IRFSZ34/35 IRFSZ30/32

N-CHANNEL POWER MOSFETS

FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

TO-220F



IRFSZ34/35
IRFSZ30/32

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFSZ34	60V	0.05Ω	18.7A
IRFSZ35	60V	0.07Ω	15.6A
IRFSZ30	50V	0.05Ω	18.7A
IRFSZ32	50V	0.07Ω	15.6A

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	IRFSZ34	IRFSZ35	IRFSZ30	IRFSZ32	Unit
Drain-Source Voltage (1)	V_{DSS}	60		50		Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	60		50V		Vdc
Gate-Source Voltage	V_{GS}	± 20				Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	18.7	15.6	18.7	15.6	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	13.1	11.2	13.1	11.2	Adc
Drain Current—Pulsed (3)	I_{DM}	120	100	120	100	Adc
Gate Current—Pulsed	I_{GM}	± 1.5				Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	8				mJ
Avalanche Current	I_{AS}	18.7				A
Total Power Dissipation at $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	35 0.28				Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150				$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300				$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=50\mu H$, $V_{dd}=25V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage IRFSZ34/35	60	—	—	V	$V_{GS}=0V, I_D=250\mu A$
	IRFSZ30/32	50	—	—	V	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}, I_D=250\mu A$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS}=+20V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	100	nA	$V_{GS}=-20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS}=\text{Max. Rating}, V_{GS}=0V$
		—	—	1000		$V_{DS}=0.8\text{Max. Rating}, V_{GS}=0V, T_C=125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2) IRFSZ34/30	30	—	—	A	$V_{DS}\geq 2.1V$
	IRFSZ35/32	25	—	—	A	$V_{GS}=10V$
$R_{DS(on)}$	Static Drain-Source On-State Resistance IRFSZ34/30	—	—	0.05	Ω	$V_{GS}=10V, I_D=18A$
	IRFSZ35/32	—	—	0.07	Ω	
g_{ts}	Forward Transconductance (2)	9.3	—	—	Ω	$V_{DS}\geq 50V, I_D=18A$
C_{iss}	Input Capacitance	—	1300	—	pF	$V_{GS}=0V$
C_{oss}	Output Capacitance	—	650	—	pF	$V_{DS}=25V$
C_{rss}	Reverse Transfer Capacitance	—	100	—	pF	$f=1.0\text{MHz}$
$t_{d(on)}$	Turn-On Delay Time	—	—	21	ns	$V_{DD}=0.5 BV_{DSS}, I_D=18.7A, Z_O=12\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	—	110	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	—	21	ns	
t_f	Fall Time	—	—	80	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	—	47	nC	$V_{GS}=10V, I_D=18.7A, V_{DS}=0.8, \text{Max. Rating}$ (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	—	10	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	—	22	nC	

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	MAX	3.6	K/W	
R_{thCS}	Case-to-Sink	TYP	0.5	K/W	Mounting surface flat smooth, and greased
R_{thJA}	Junction-to-Ambient	MAX	80	K/W	Free Air Operation

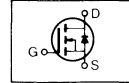
Notes: (1) $T_J=25^\circ\text{C}$ to 150°C

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

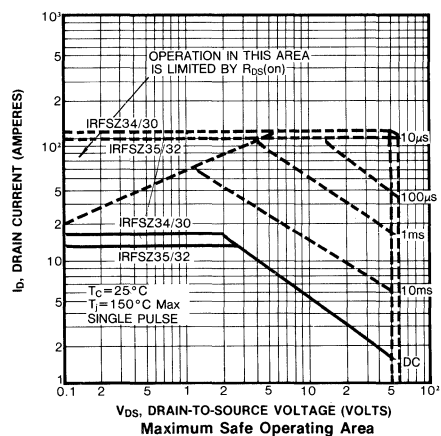
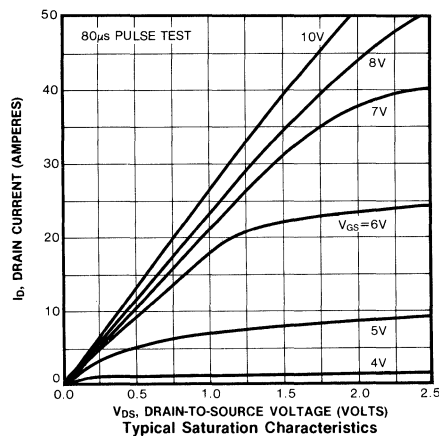
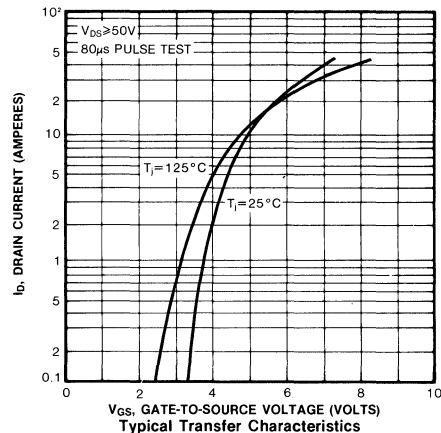
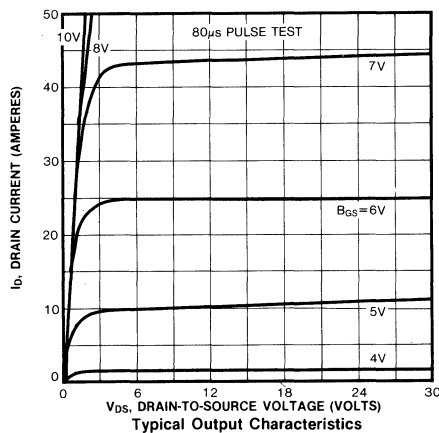
(3) Repetitive rating: Pulse width limited by max. junction temperature

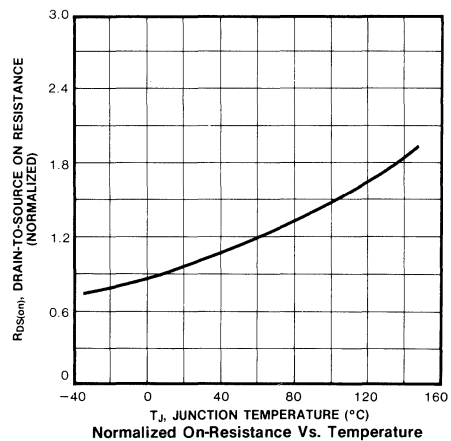
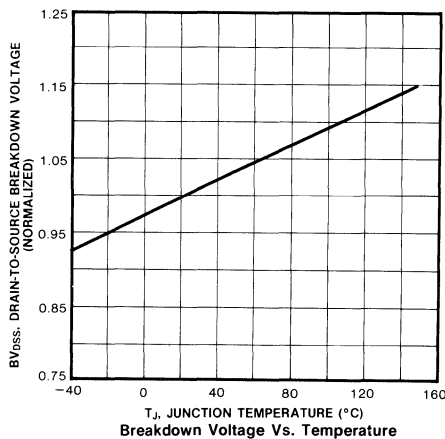
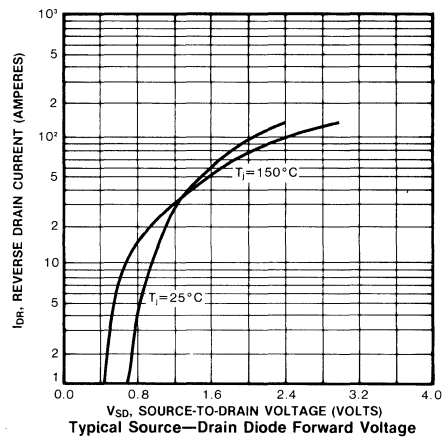
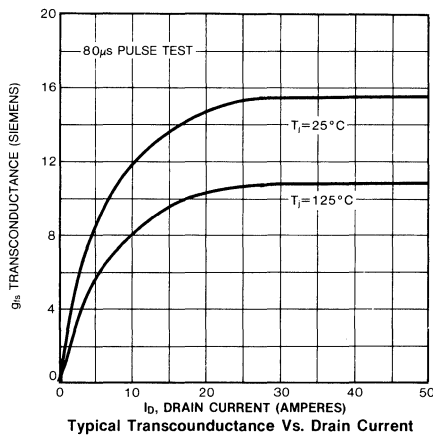
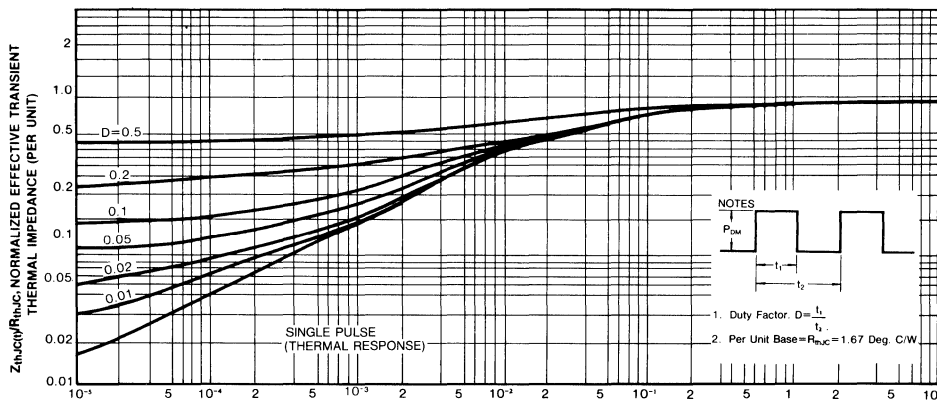
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

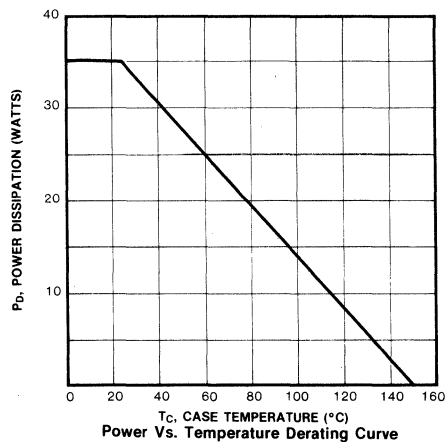
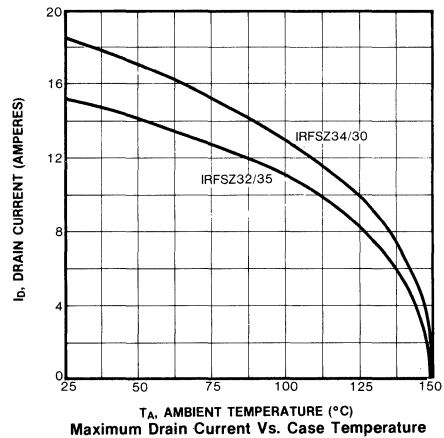
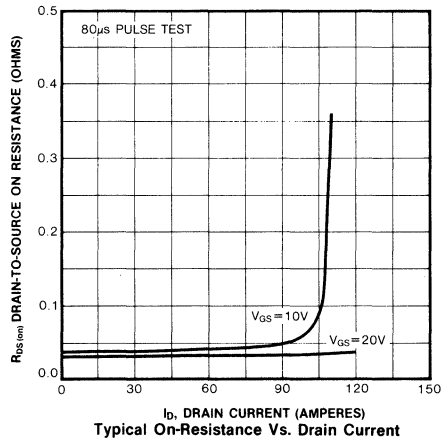
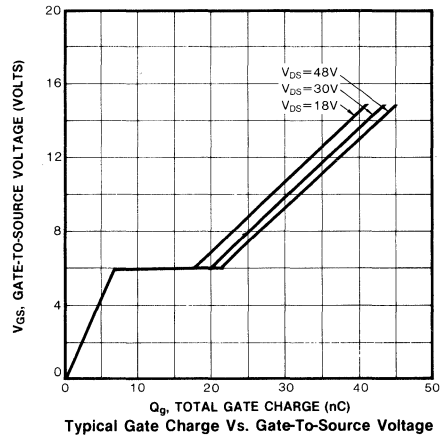
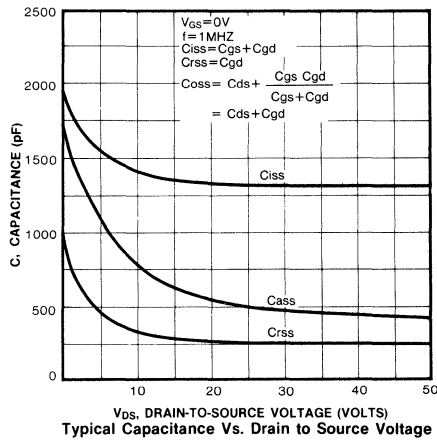
Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	18.7	A	Modified MOSFET integral reverse P-N junction rectifier
I_{SM}	Pulse-Source Current (3)	—	—	120	A	
		—	—	100	A	
V_{SD}	Diode Forward Voltage (2)	—	—	1.6	V	$T_C = 25^\circ\text{C}$, $I_S = 30\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	—	220	ns	$T_J = 25^\circ\text{C}$, $I_F = 30\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$



- Notes:** (1) $T_J = 25^\circ\text{C}$ to 150°C
(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature

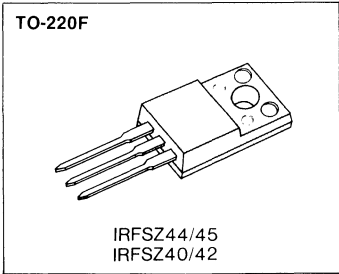






FEATURES

- Lower $R_{DS(ON)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability



PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFSZ44	60V	0.028 Ω	34.0A
IRFSZ45	60V	0.035 Ω	30.0A
IRFSZ40	50V	0.028 Ω	34.0A
IRFSZ42	50V	0.035 Ω	30.0A

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	IRFSZ44	IRFSZ45	IRFSZ40	IRFSZ42	Unit
Drain-Source Voltage (1)	V _{DSS}	60		50		V _{dc}
Drain-Gate Voltage (R _{GS} =1.0MΩ)(1)	V _{DGR}	60		50		V _{dc}
Gate-Source Voltage	V _{GS}	± 20				V _{dc}
Continuous Drain Current T _C =25°C	I _D	34.0	30.0	34.0	30.0	A _{dc}
Continuous Drain Current T _C =100°C	I _D	24.0	21.0	24.0	21.0	A _{dc}
Drain Current—Pulsed (3)	I _{DM}	120	100	120	100	A _{dc}
Gate Current—Pulsed	I _{GM}	± 1.5				A _{dc}
Single Pulsed Avalanche Energy (4)	E _{AS}	48				mJ
Avalanche Current	I _{AS}	34				A
Total Power Dissipation at T _C =25°C Derate above 25°C	P _D	65 0.52				Watts W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	−55 to 150				°C
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T _L	300				°C

- Notes: (1) $T_J=25^\circ C$ to $150^\circ C$
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature
(4) $L=50\mu H$, $V_{dd}=25V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-Source Breakdown Voltage IRFSZ44/45	60	—	—	V	V _{GS} =0V, I _D =250 μ A
	IRFSZ40/42	50	—	—	V	
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} =V _{GS} , I _D =250 μ A
I _{GSS}	Gate-Source Leakage Forward	—	—	100	nA	V _{GS} =20V
I _{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	V _{GS} =-20V
I _{DSS}	Zero Gate Voltage Drain Current	—	—	250	μ A	V _{DS} =Max. Rating, V _{GS} =0V
		—	—	1000		V _{DS} =0.8 $\times$ Max. Rating, V _{GS} =0V, T _C =125 $^\circ\text{C}$
I _{D(on)}	On-State Drain-Source Current (2)	35	—	—	A	V _{DS} $\geq$ 1.2V
		35	—	—	A	V _{GS} =10V
R _{DS(on)}	Static Drain-Source IRFSZ44/40	—	—	0.028	Ω	V _{GS} =10V, I _D =23A
	On-State Resistance IRFSZ45/42	—	—	0.035	Ω	
g _{fs}	Forward Transconductance (2)	15	—	—	U	V _{DS} $\geq$ 50V, I _D =23A
C _{iss}	Input Capacitance	—	2450	—	pF	V _{GS} =0V
C _{oss}	Output Capacitance	—	740	—	pF	V _{DS} =25V
C _{rss}	Reverse Transfer Capacitance	—	360	—	pF	f=1.0MHz
t _{d(on)}	Turn-On Delay Time	—	—	32	ns	V _{DD} =0.5 BV _{DSS} , I _D =52A Z _O =9.1 Ω (MOSFET switching times are essentially independent of operating temperature)
t _r	Rise Time	—	—	210	ns	
t _{d(off)}	Turn-Off Delay Time	—	—	75	ns	
t _f	Fall Time	—	—	130	ns	
Q _g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	—	100	nC	V _{GS} =10V, I _D =52A, V _{DS} =0.8, Max. Rating (Gate charge is essentially independent of operating temperature.)
Q _{gs}	Gate-Source Charge	—	—	21	nC	
Q _{gd}	Gate-Drain ("Miller") Charge	—	—	58	nC	

THERMAL RESISTANCE

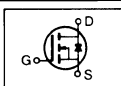
R _{thJC}	Junction-to-Case	MAX	1.92	K/W	
R _{thCS}	Case-to-Sink	TYP	0.5	K/W	Mounting surface flat smooth, and greased
R _{thJA}	Junction-to-Ambient	MAX	80	K/W	Free Air Operation

Notes: (1) T_J=25 $^\circ\text{C}$ to 150 $^\circ\text{C}$

(2) Pulse test: Pulse width<300 μ s, Duty Cycle $\leq$ 2%

(3) Repetitive rating: Pulse width limited by max. junction temperature

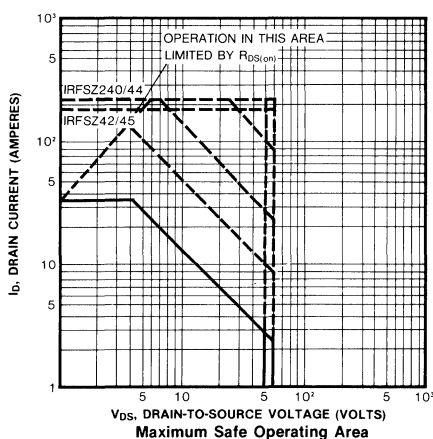
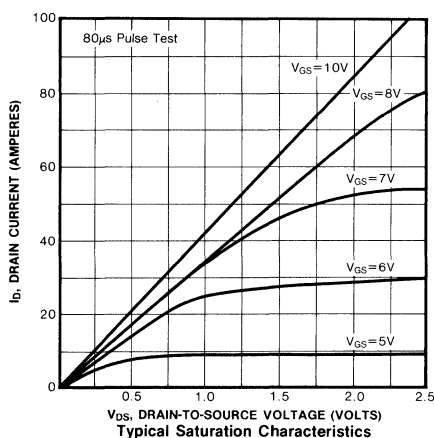
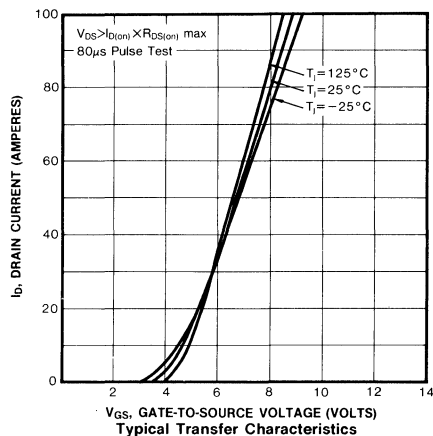
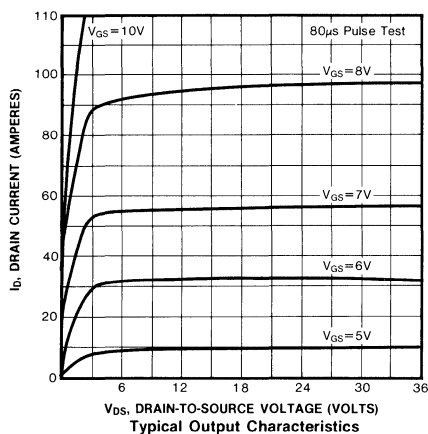
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

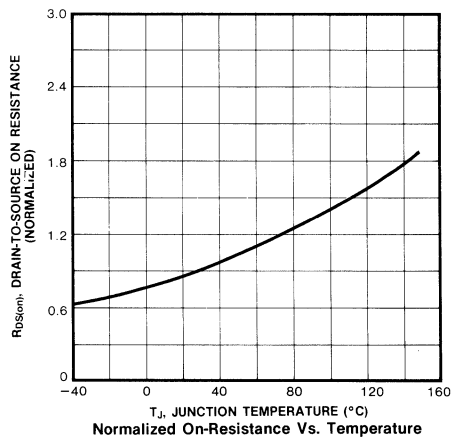
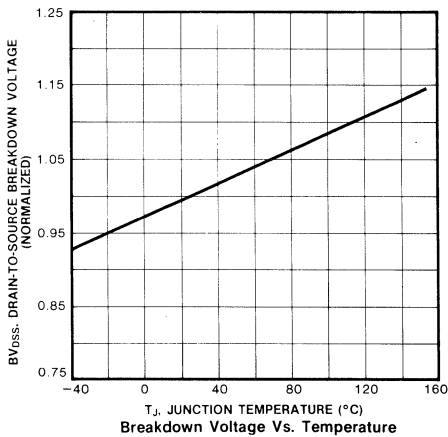
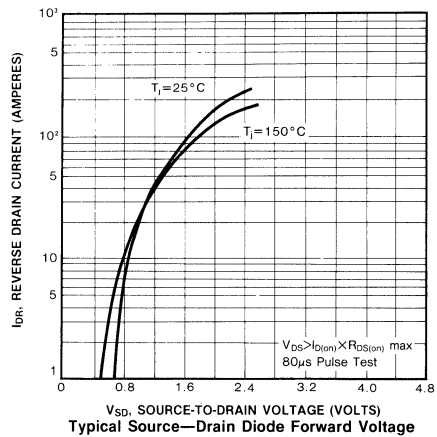
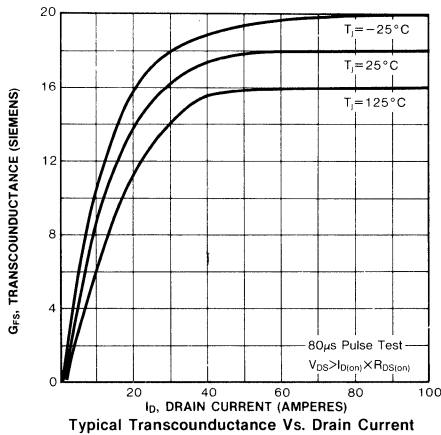
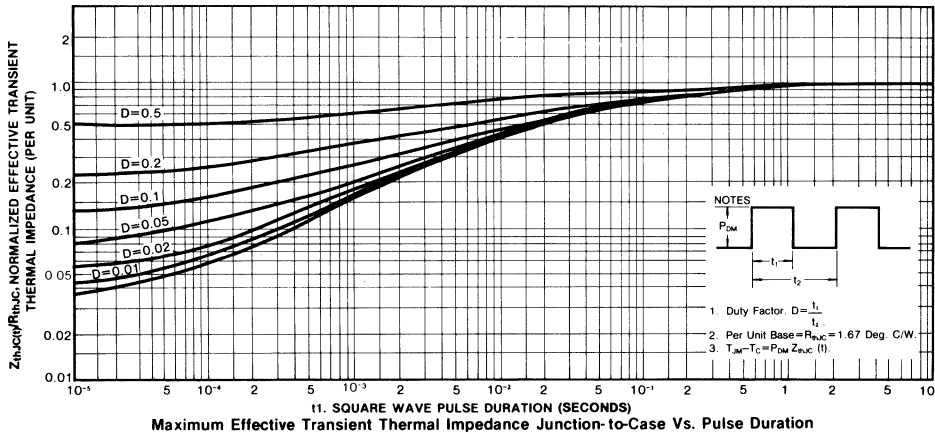
Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	23.0	A	Modified MOSFET integral reverse P-N junction rectifier 
I_{SM}	Pulse-Source Current (3)	—	—	210	A	
V_{SD}	Diode Forward Voltage (2)	—	—	2.5	V	$T_C = 25^\circ\text{C}$, $I_S = 35\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	—	250	ns	$T_J = 25^\circ\text{C}$, $I_F = 35\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$

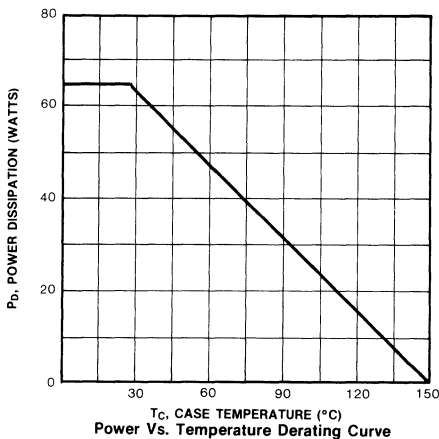
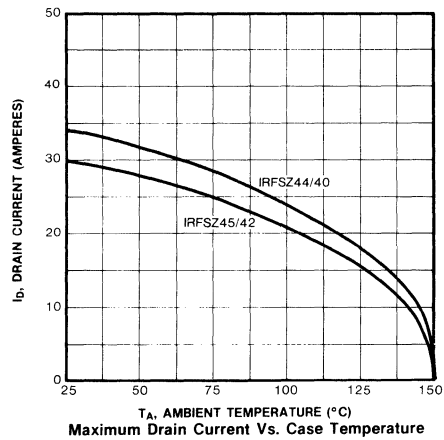
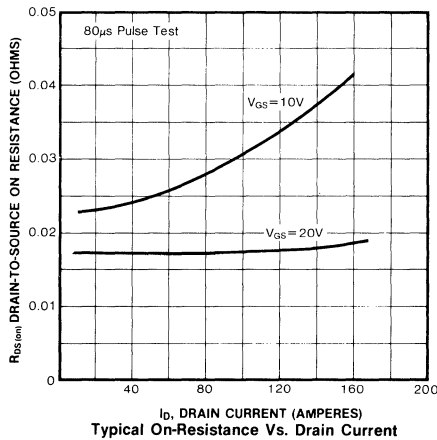
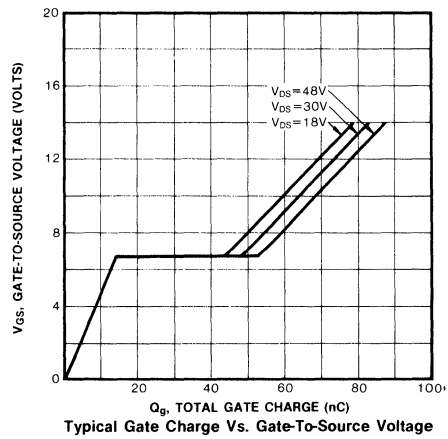
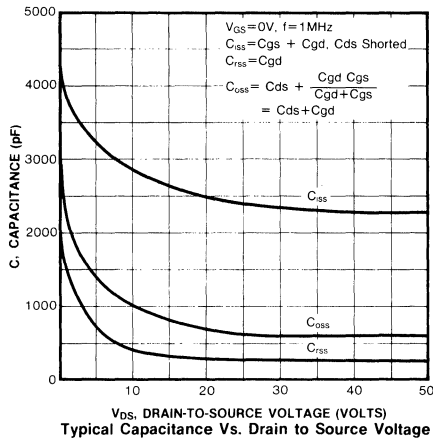
Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C

(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature



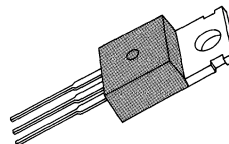




FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

TO-220



IRFZ10/12
IRFZ14/15

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFZ10	50V	0.20 Ω	10A
IRFZ12	50V	0.30 Ω	8.3A
IRFZ14	60V	0.20 Ω	10A
IRFZ15	60V	0.32 Ω	8.3A

MAXIMUM RATINGS

Characteristic	Symbol	IRFZ10	IRFZ14	IRFZ12	IRFZ15	Unit
Drain-Source Voltage (1)	V_{DS}	50	60	50	60	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	50	60	50	60	Vdc
Gate-Source Voltage	V_{GS}	± 20				Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	10		8.3		Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	7.2		5.8		Adc
Drain Current—Pulsed (3)	I_{DM}	40		33		Adc
Gate Current—Pulsed	I_{GM}	± 1.5				Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	2.2				mJ
Avalanche Current	I_{AS}	10				A
Total Power Dissipation at $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	42 0.29				Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 175				$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300				$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $175^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=50\mu H$, $V_{dd}=25V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-Source Breakdown Voltage					$V_{GS}=0V, I_D=-250\mu A$
	IRFZ10/12	50	—	—	V	
	IRFZ14/15	60	—	—		
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}, I_D=250\mu A$
I _{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS}=20V$
I _{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	$V_{GS}=-20V$
I _{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS}=\text{Max. Rating}, V_{GS}=0V$
		—	—	1000		$V_{DS}=0.8 \times \text{Max. Rating}, V_{GS}=0V, T_C=150^\circ\text{C}$
I _{D(on)}	On-State Drain-Source Current (2)					$V_{DS} \geq 3V, V_{GS}=10V$
	IRFZ10	10	—	—	A	
	IRFZ14					
	IRFZ12/IRFZ15	8.3	—	—	A	
R _{DS(on)}	Static Drain-Source	IRFZ10	—	0.15	0.20	$V_{GS}=10V, I_D=5.8A$
	On-State Resistance	IRFZ14				
	IRFZ12/IRFZ15	—	—	0.30	Ω	
g _{fs}	Forward Transconductance (2)	2.4	—	—	Ω	$V_{DS} \geq 50V, I_D=5.8A$
C _{iss}	Input Capacitance	—	358	—	pF	$V_{GS}=0V$
C _{oss}	Output Capacitance	—	134	—	pF	$V_{DS}=25V$
C _{rss}	Reverse Transfer Capacitance	—	55	—	pF	$f=1.0\text{MHz}$
t _{d(on)}	Turn-On Delay Time	—	—	15	ns	$V_{DD}=0.5 \text{ BV}_{DSS}, I_D=10A, Z_O=24\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t _r	Rise Time	—	—	75	ns	
t _{d(off)}	Turn-Off Delay Time	—	—	20	ns	
t _f	Fall Time	—	—	29	ns	
Q _g	Total Gate Charge (Gate-Source Pulse Gate-Drain)	—	—	12	nC	$V_{GS}=10V, I_D=10A, V_{DS}=0.8\text{Max. Rating}$ (Gate charge is essentially independent of operating temperature.)
Q _{gs}	Gate-Source Charge	—	—	3.1	nC	
Q _{gd}	Gate-Drain ("Miller") Charge	—	—	5.8	nC	

THERMAL RESISTANCE

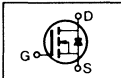
R _{thJC}	Junction-to-Case	MAX	3.5	K/W	
R _{thCS}	Case-to-Sink	TYP	0.5	K/W	Mounting surface flat smooth, and greased
R _{thJA}	Junction-to-Ambient	MAX	80	K/W	Free Air Operation

Notes: (1) $T_J=25^\circ\text{C}$ to 175°C

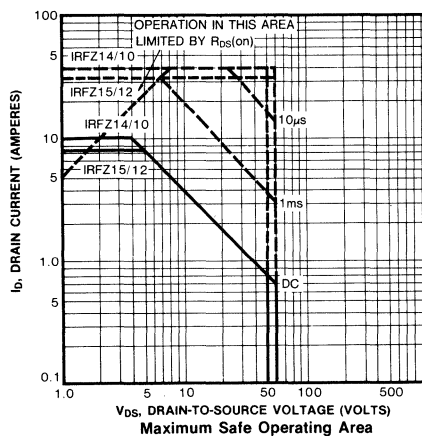
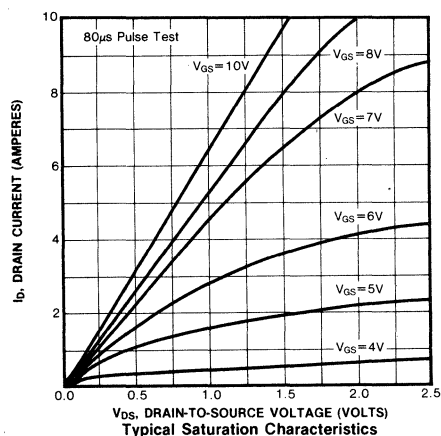
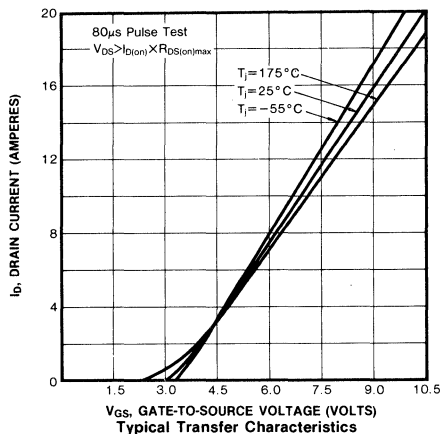
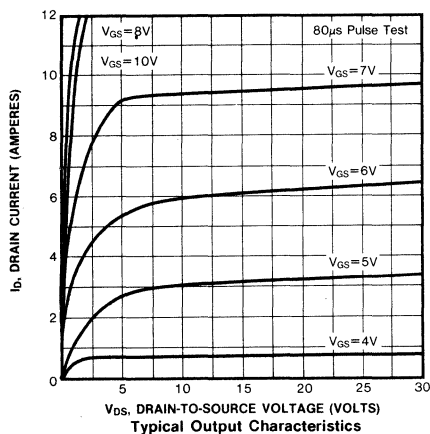
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

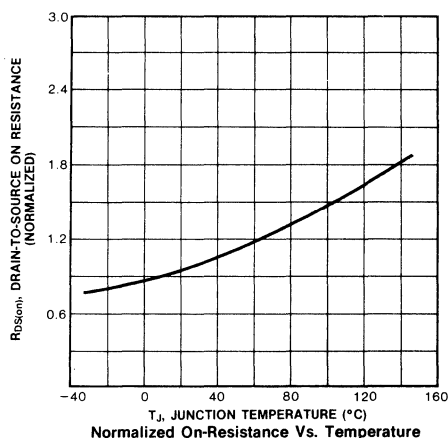
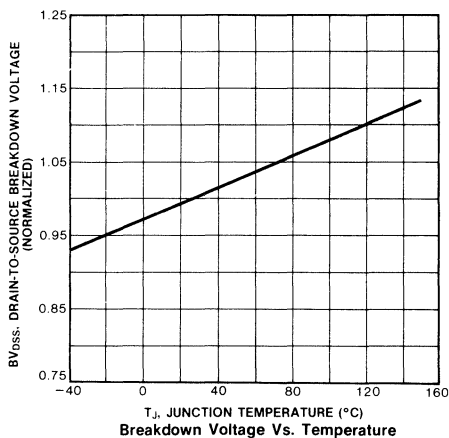
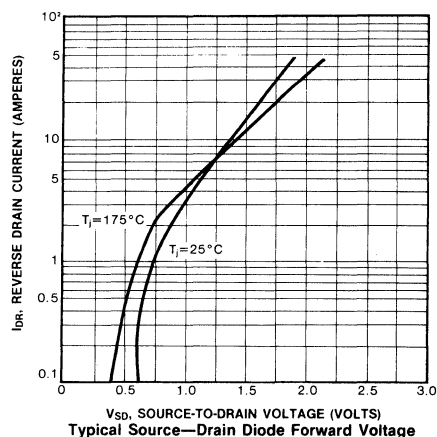
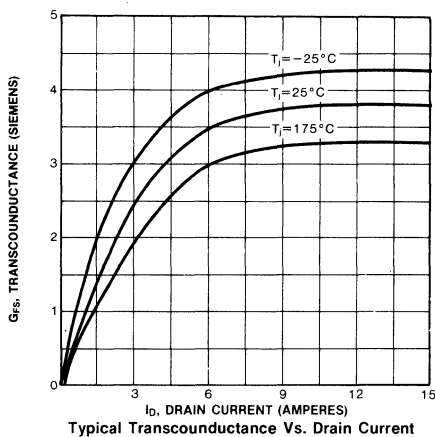
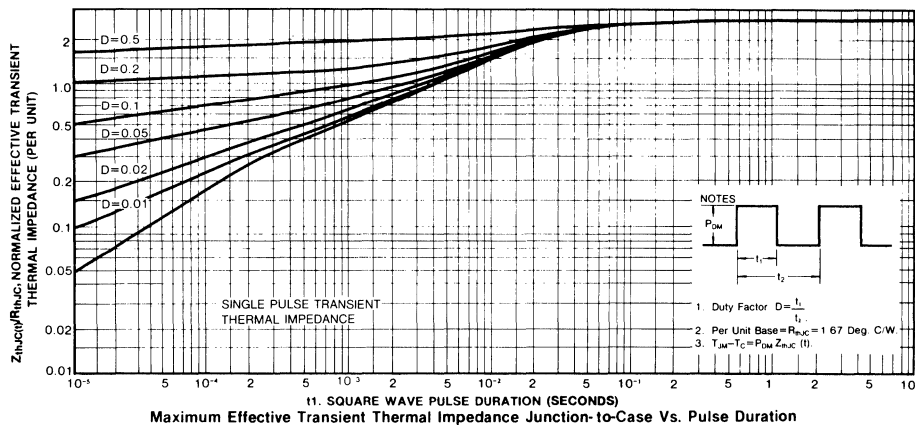
(3) Repetitive rating: Pulse width limited by max. junction temperature

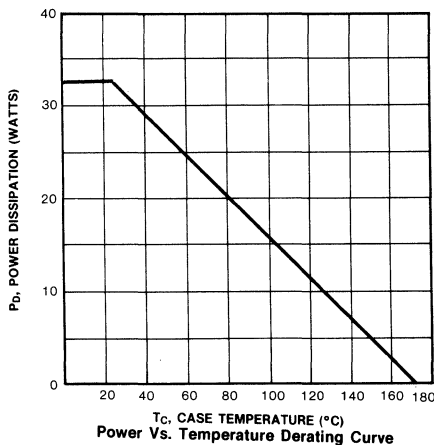
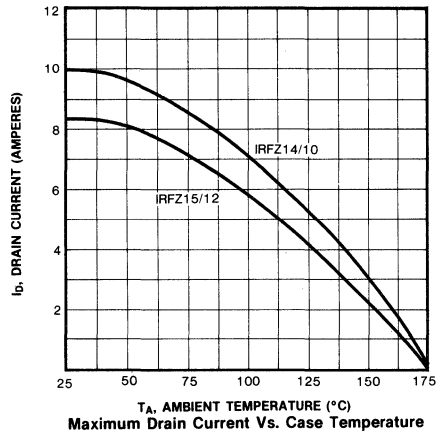
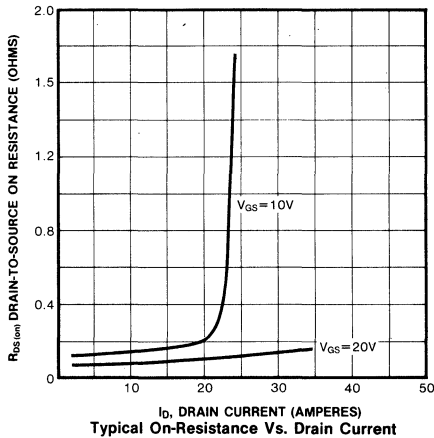
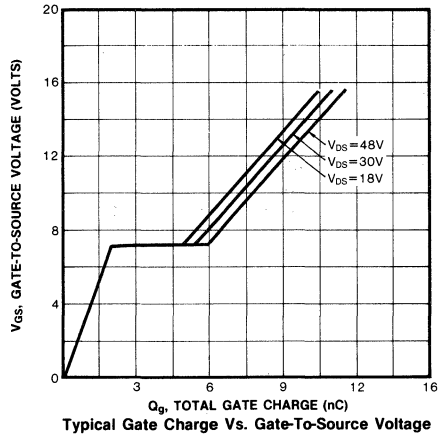
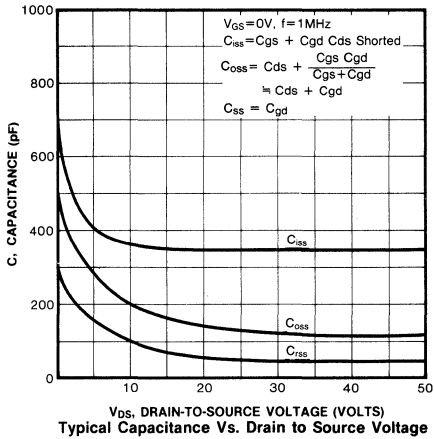
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	10	A	Modified MOSFET integral reverse P-N junction rectifier 
I_{SM}	Pulse-Source Current (3)	—	—	40	A	
V_{SD}	Diode Forward Voltage (2)	—	—	1.6	V	$T_C = 25^\circ\text{C}$, $I_S = 10\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	—	140	ns	$T_J = 25^\circ\text{C}$, $I_F = 35\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$

- Notes:** (1) $T_J = 25^\circ\text{C}$ to 175°C
 (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
 (3) Repetitive rating: Pulse with limited by max. junction temperature



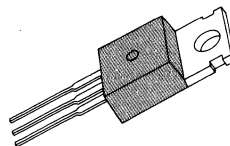




FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

TO-220



IRFZ24/Z25
IRFZ20/Z22

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFZ20	50V	$0.10\ \Omega$	15A
IRFZ22	50V	$0.12\ \Omega$	14A
IRFZ24	60V	$0.10\ \Omega$	15A
IRFZ25	60V	$0.12\ \Omega$	14A

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	IRFZ20	IRFZ22	IRFZ24	IRFZ25	Unit
Drain-Source Voltage (1)	V _{DSS}	50		60		V _{dc}
Drain-Gate Voltage (R _{GS} =1.0MΩ)(1)	V _{DGR}	50		60		V _{dc}
Gate-Source Voltage	V _{GS}	±20				V _{dc}
Continuous Drain Current T _C =25°C	I _D	15	14	15	14	A _{dc}
Continuous Drain Current T _C =100°C	I _D	10	9	10	9	A _{dc}
Drain Current—Pulsed (3)	I _{DM}	60	56	60	56	A _{dc}
Gate Current—Pulsed	I _{GM}	±1.5				A _{dc}
Single Pulsed Avalanche Energy (4)	E _{AS}	9.5				mJ
Avalanche Current	I _{AS}	15				A
Total Power Dissipation at T _C =25°C Derate above 25°C	P _D	40 0.32				Watts W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	−55 to 175				°C
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T _L	300				°C

Notes: (1) $T_J=25^\circ C$ to $175^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=100\mu H$, $V_{dd}=25V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage	60	—	—	V	$V_{GS}=0V$, $I_D=250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}$, $I_D=250\mu A$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS}=20V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	$V_{GS}=-20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS}=\text{Max. Rating}$, $V_{GS}=0V$
		—	—	1000		$V_{DS}=0.8\text{Max. Rating}$, $V_{GS}=0V$, $T_C=150^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2)	15	—	—	A	$V_{DS}\geq 1.8V$
		14	—	—	A	$V_{GS}=10V$
$R_{DS(on)}$	Static Drain-Source On-State Resistance	—	0.08	0.10	Ω	$V_{GS}=10V$, $I_D=9.0A$
g_{fs}	Forward Transconductance (2)	5.6	6.1	—	Ω	$V_{DS}>R_{DS}\times I_{D(on)}$, $I_D=9.0A$
C_{iss}	Input Capacitance	—	635	—	pF	$V_{GS}=0V$
C_{oss}	Output Capacitance	—	218	—	pF	$V_{DS}=25V$
C_{rss}	Reverse Transfer Capacitance	—	105	—	pF	$f=1.0\text{MHz}$
$t_{d(on)}$	Turn-On Delay Time	—	—	30	ns	$V_{DD}=0.5 BV_{DSS}$, $I_D=9.0A$ $Z_O=50\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	—	90	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	—	40	ns	
t_f	Fall Time	—	—	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	—	17	nC	$V_{GS}=10V$, $I_D=9.0A$, $V_{DS}=0.8$, Max. Rating (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	—	7.5	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	—	18	nC	

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	MAX	3.12	K/W	
R_{thCS}	Case-to-Sink	TYP	1.0	K/W	Mounting surface flat, Smooth, and greased
R_{thJA}	Junction-to-Ambient	MAX	80	K/W	Free Air Operation

Notes: (1) $T_J=25^\circ\text{C}$ to 175°C

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

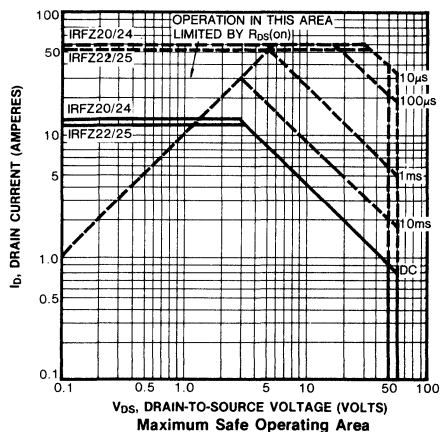
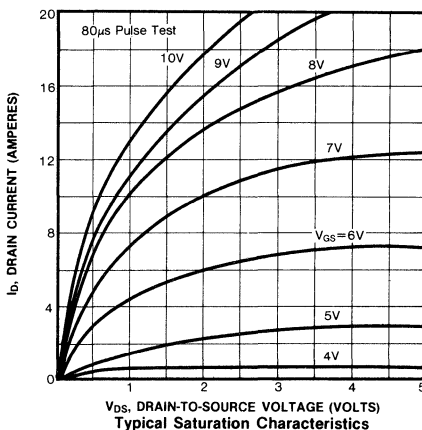
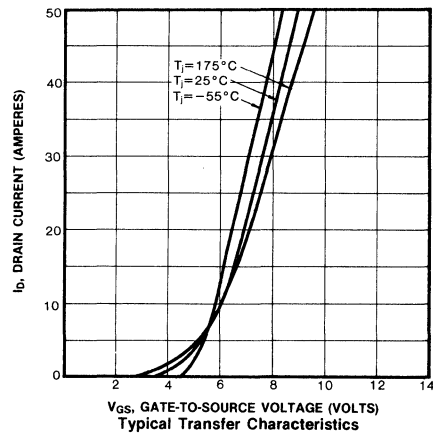
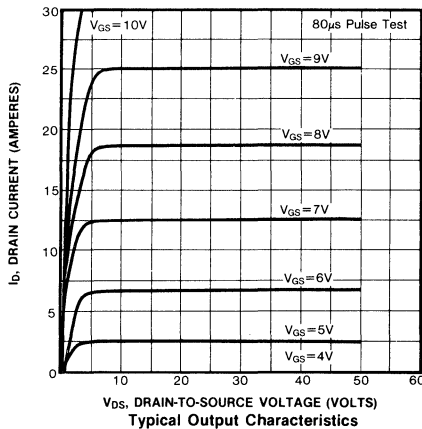
(3) Repetitive rating: Pulse width limited by max. junction temperature

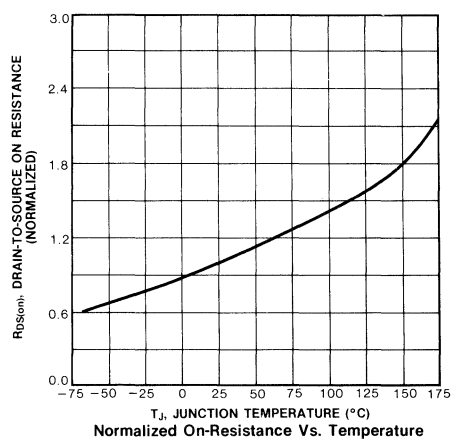
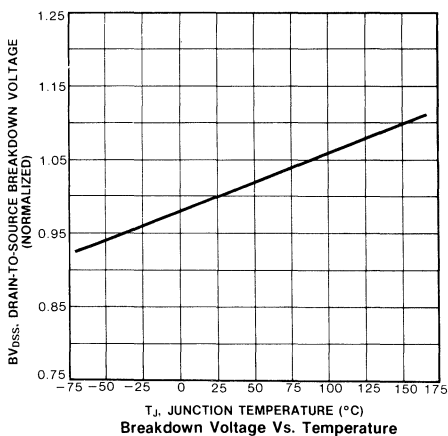
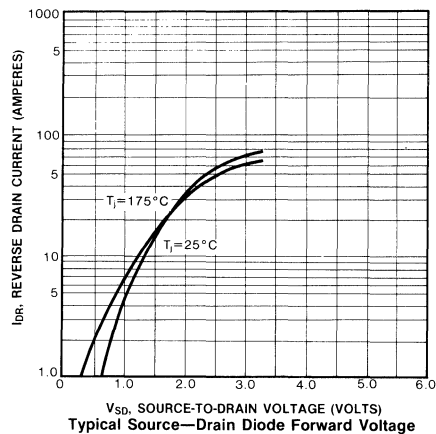
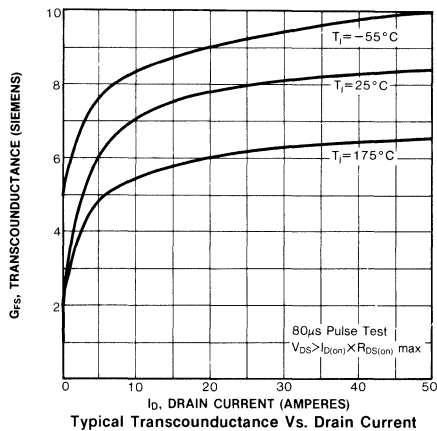
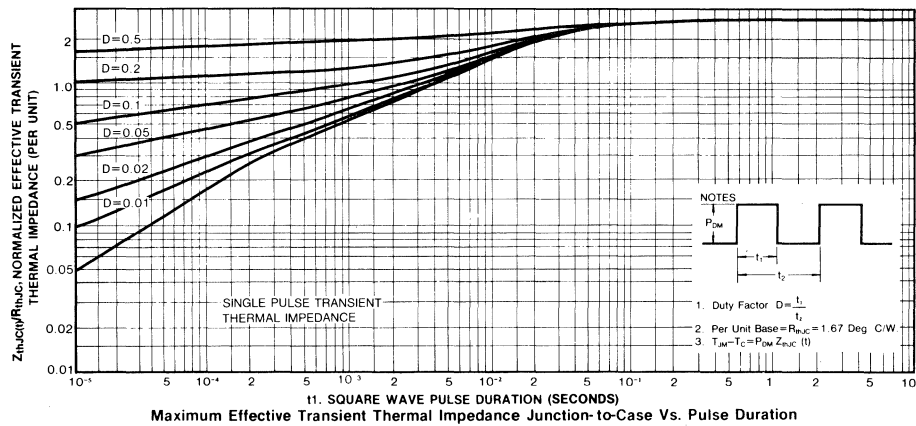
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

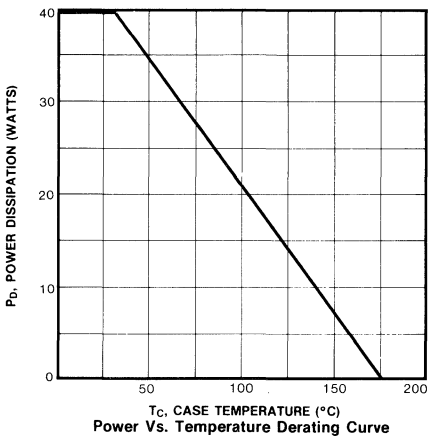
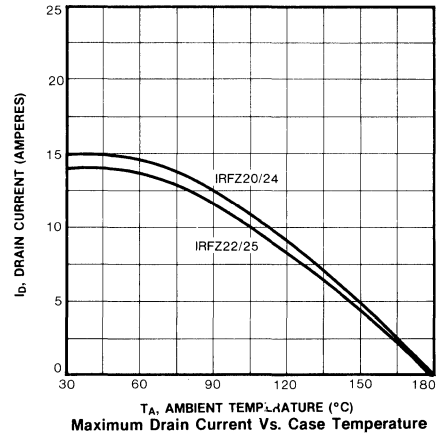
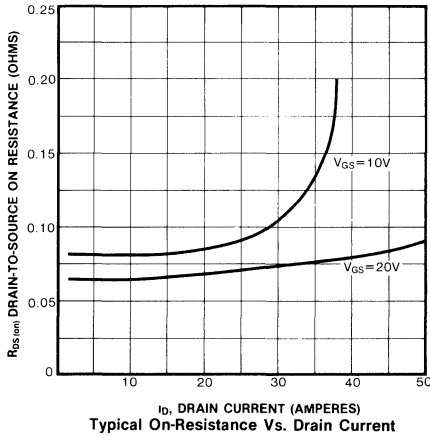
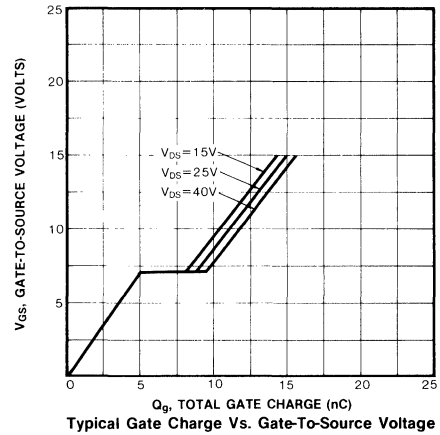
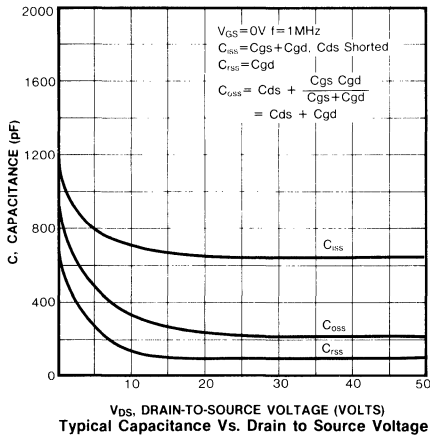
Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	15	A	Modified MOSFET integral reverse P-N junction rectifier
I_{SM}	Pulse-Source Current	—	—	60	A	
V_{SD}	Diode Forward Voltage	—	—	1.5	V	$T_C=25^\circ\text{C}$, $I_S=15\text{A}$, $V_{GS}=0\text{V}$
t_{rr}	Reverse Recovery Time	—	—	310	ns	$T_J=25^\circ\text{C}$, $I_F=15\text{A}$, $dI_F/dt=100\text{A}/\mu\text{S}$



- Notes:** (1) $T_J=25^\circ\text{C}$ to 175°C
 (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
 (3) Repetitive rating: Pulse with limited by max. junction temperature

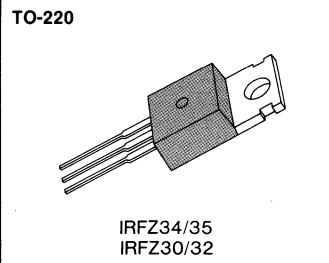






FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability



PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFZ34	60V	0.05Ω	30A
IRFZ35	60V	0.07Ω	25A
IRFZ30	50V	0.05Ω	30A
IRFZ32	50V	0.07Ω	25A

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	IRFZ34	IRFZ35	IRFZ30	IRFZ32	Unit
Drain-Source Voltage (1)	V_{DSS}	60		50		Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	60		50		Vdc
Gate-Source Voltage	V_{GS}	± 20				Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	30	25	30	25	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	21	18	21	18	Adc
Drain Current—Pulsed (3)	I_{DM}	120	100	120	100	Adc
Gate Current—Pulsed	I_{GM}	± 1.5				Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	19				mJ
Avalanche Current	I_{AS}	30				A
Total Power Dissipation at $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	90 0.60				Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to $175^\circ C$				$^\circ C$
Maximum Lead Temp. for Soldering Purposes, $1/8"$ from case for 5 seconds	T_L	300				$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $175^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=50\mu H$, $V_{dd}=25V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage IRFZ34/35	60	—	—	V	$V_{GS}=0V, I_D=250\mu A$
	IRFZ30/32	50	—	—	V	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}, I_D=250\mu A$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS}=+20V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	100	nA	$V_{GS}=-20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS}=\text{Max. Rating}, V_{GS}=0V$
		—	—	1000		$V_{DS}=0.8 \times \text{Max. Rating}, V_{GS}=0V, T_C=150^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2) IRFZ34/30	30	—	—	A	$V_{DS} \geq 2.1V$
	IRFZ35/32	25	—	—	A	$V_{GS}=10V$
$R_{DS(on)}$	Static Drain-Source On-State Resistance IRFZ34/30	—	—	0.05	Ω	$V_{GS}=10V, I_D=18A$
	IRFZ35/32	—	—	0.07	Ω	
g_{fs}	Forward Transconductance (2)	9.3	—	—	S	$V_{DS} \geq 50V, I_D=18A$
C_{iss}	Input Capacitance	—	1300	—	pF	$V_{GS}=0V$
C_{oss}	Output Capacitance	—	650	—	pF	$V_{DS}=25V$
C_{rss}	Reverse Transfer Capacitance	—	100	—	pF	$f=1.0\text{MHz}$
$t_{d(on)}$	Turn-On Delay Time	—	—	21	ns	$V_{DD}=0.5 BV_{DSS}, I_D=30A, Z_O=12\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	—	110	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	—	53	ns	
t_f	Fall Time	—	—	80	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	—	47	nC	$V_{GS}=10V, I_D=30A, V_{DS}=0.8, \text{Max. Rating}$ (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	—	10	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	—	22	nC	

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	MAX	1.7	K/W	
R_{thCS}	Case-to-Sink	TYP	0.5	K/W	Mounting surface flat
R_{thJA}	Junction-to-Ambient	MAX	80	K/W	Free Air Operation

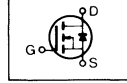
Notes: (1) $T_J = 25^\circ\text{C}$ to 175°C

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse width limited by max. junction temperature

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

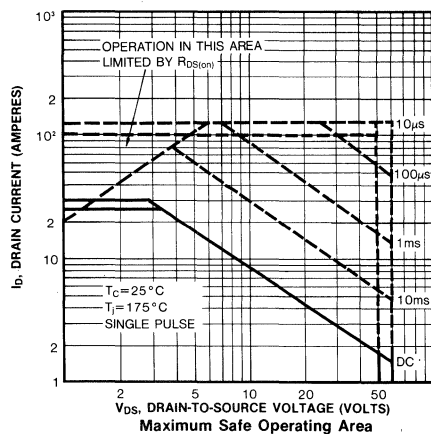
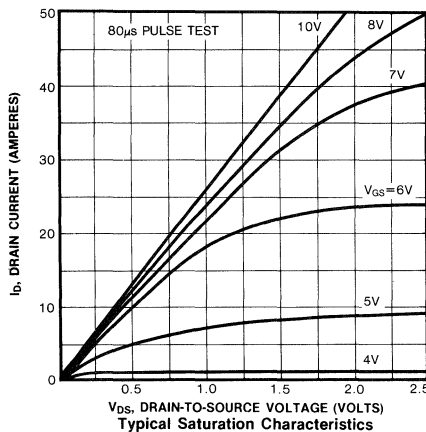
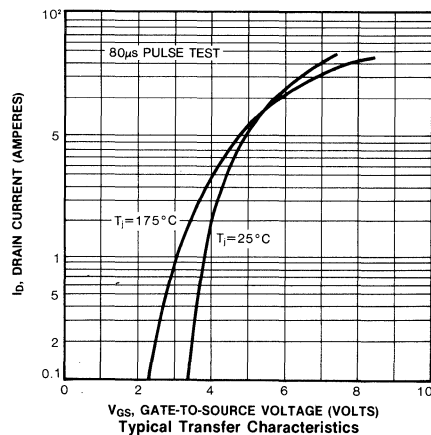
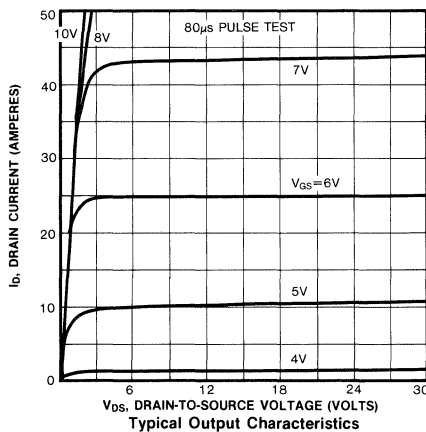
Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	30	A	Modified MOSFET integral reverse P-N junction rectifier
I_{SM}	Pulse-Source Current (3)	—	—	120	A	
		—	—	100	A	
V_{SD}	Diode Forward Voltage (2)	—	—	1.6	V	$T_C = 25^\circ\text{C}$, $I_S = 30\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	—	220	ns	$T_J = 25^\circ\text{C}$, $I_F = 30\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$

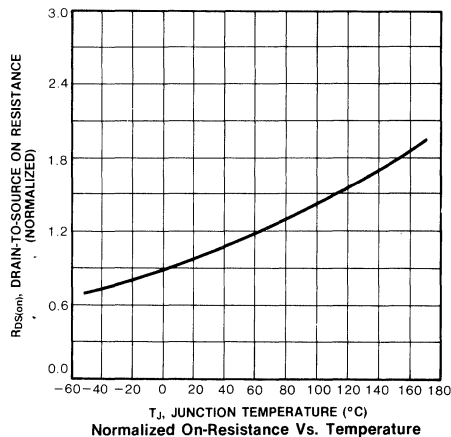
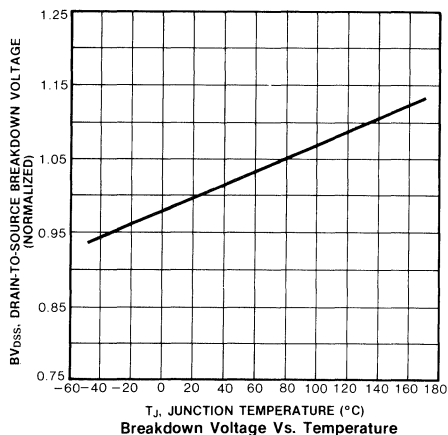
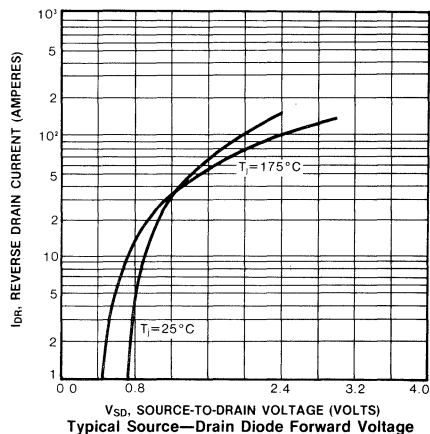
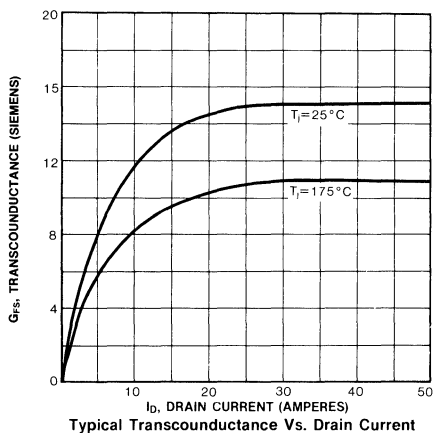
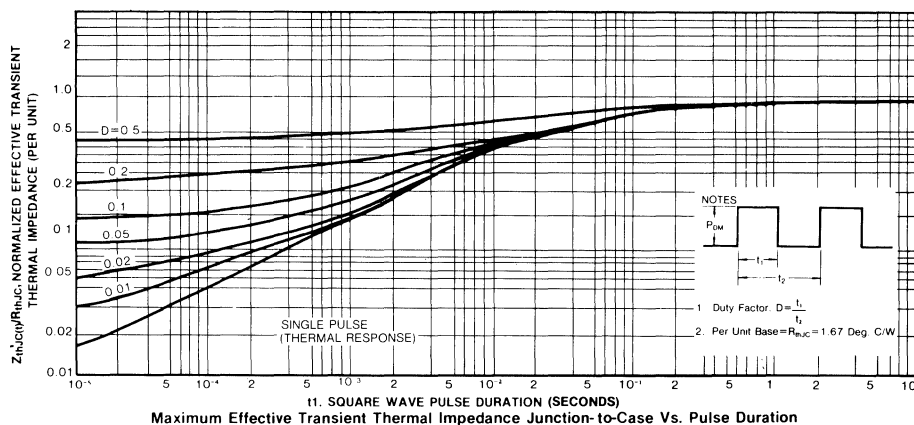


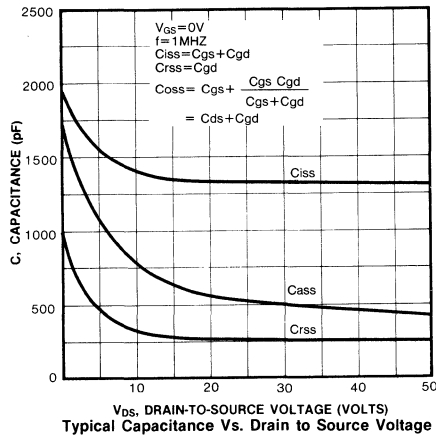
Notes: (1) $T_J = 25^\circ\text{C}$ to 175°C

(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 3\%$

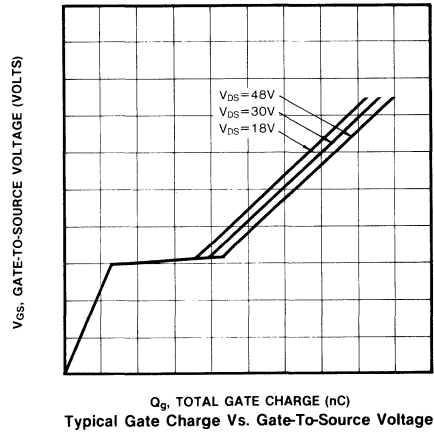
(3) Repetitive rating: Pulse with limited by max. junction temperature



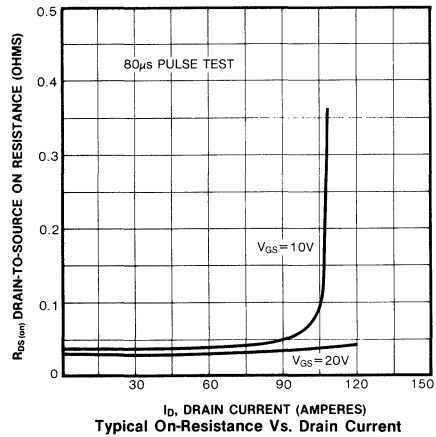




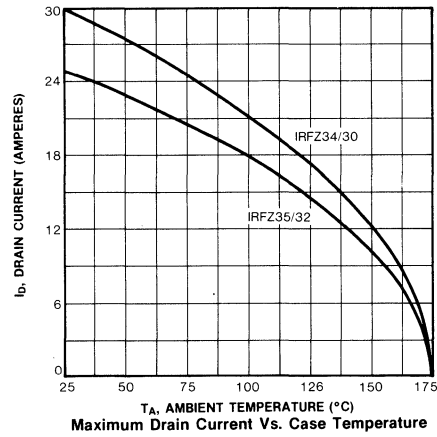
Typical Capacitance Vs. Drain to Source Voltage



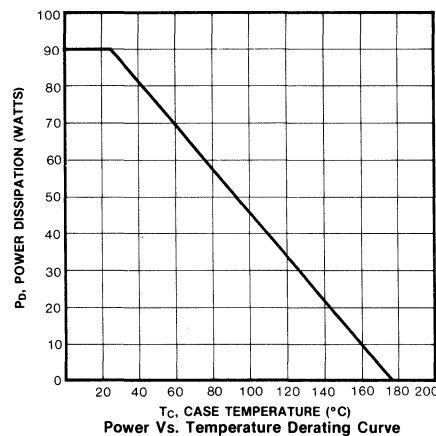
Typical Gate Charge Vs. Gate-To-Source Voltage



Typical On-Resistance Vs. Drain Current



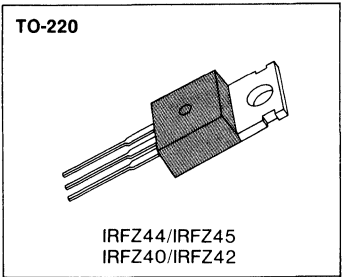
Maximum Drain Current Vs. Case Temperature



Power Vs. Temperature Derating Curve

FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability



PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFZ44	60V	0.028Ω	35A
IRFZ45	60V	0.035Ω	35A
IRFZ40	50V	0.028Ω	35A
IRFZ42	50V	0.035Ω	35A

* Current limited by wire & pin diameter

MAXIMUM RATINGS

Characteristic	Symbol	IRFZ44	IRFZ45	IRFZ40	IRFZ42	Unit
Drain-Source Voltage (1)	V _{DSS}	60		50		V _{dc}
Drain-Gate Voltage (R _{GS} =1.0MΩ)(1)	V _{DGR}	60		50		V _{dc}
Gate-Source Voltage	V _{GS}	± 20				V _{dc}
Continuous Drain Current T _C =25 °C	I _D	35	35	35	35	A _{dc}
Continuous Drain Current T _C =100 °C	I _D	35	33	35	33	A _{dc}
Drain Current—Pulsed (3)	I _{DM}	210	190	210	190	A _{dc}
Gate Current—Pulsed	I _{GM}	± 1.5				A _{dc}
Single Pulsed Avalanche Energy (4)	E _{AS}	53				mJ
Avalanche Current	I _{AS}	35				A
Total Power Dissipation at T _C =25 °C Derate above 25 °C	P _D	150 1.2				Watts W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-55 to 175 °				°C
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T _L	300				°C

- Notes: (1) $T_J=25^\circ C$ to $175^\circ C$
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature
(4) $L=50\mu H$, $V_{dd}=25V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage IRFZ44/45 IRFZ40/42	60 50	— —	— —	V	$V_{GS}=0V$, $I_D=250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}$, $I_D=250\mu A$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS}=20V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	$V_{GS}=-20V$
I_{DSS}	Zero Gate Voltage Drain Current	— —	— —	250 1000	μA μA	$V_{DS}=\text{Max. Rating}$, $V_{GS}=0V$ $V_{DS}=0.8\text{Max. Rating}$, $V_{GS}=0V$, $T_C=150^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2)	35	—	—	A	$V_{DS}\geq 1.2V$, $V_{GS}=10V$
$R_{DS(on)}$	Static Drain-Source On-State Resistance	— —	— —	0.028 0.035	Ω	IRFZ44/40 IRFZ45/42 $V_{GS}=10V$, $I_D=33A$
g_{fs}	Forward Transconductance (2)	15	—	—	S	$V_{DS}\geq 50V$, $I_D=33A$
C_{iss}	Input Capacitance	—	2450	—	pF	$V_{GS}=0V$
C_{oss}	Output Capacitance	—	740	—	pF	$V_{DS}=25V$
C_{rss}	Reverse Transfer Capacitance	—	360	—	pF	$f=1.0\text{MHz}$
$t_{d(on)}$	Turn-On Delay Time	—	—	32	ns	$V_{DD}=0.5 BV_{DSS}$, $I_D=52A$, $Z_O=9.1\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	—	210	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	—	75	ns	
t_f	Fall Time	—	—	130	ns	
Q_g	Total Gate Charge (Gate-Source Pulse Gate-Drain)	—	—	100	nC	$V_{GS}=10V$, $I_D=52A$, $V_{DS}=0.8\text{Max. Rating}$ (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	—	21	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	—	58	nC	

THERMAL RESISTANCE

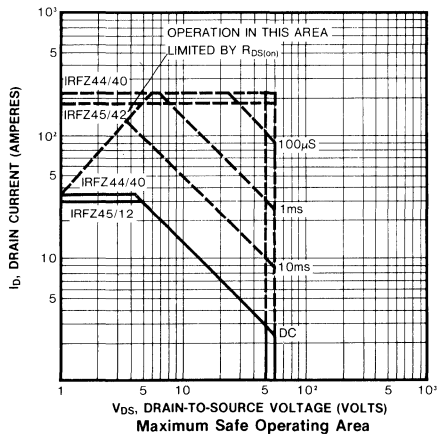
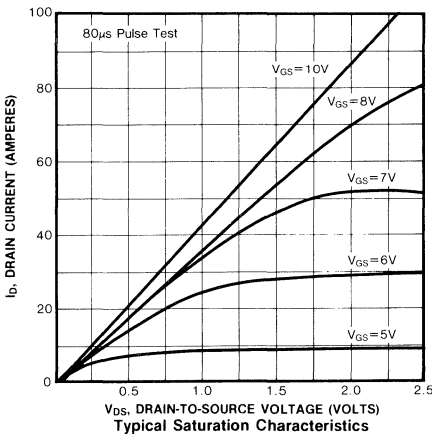
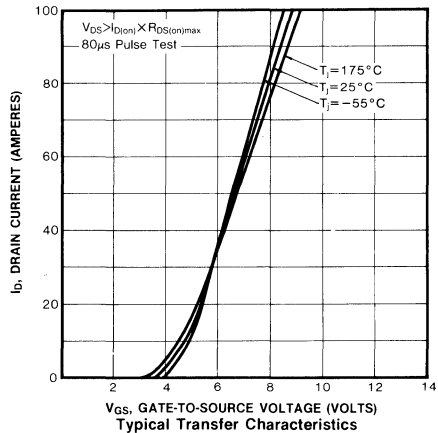
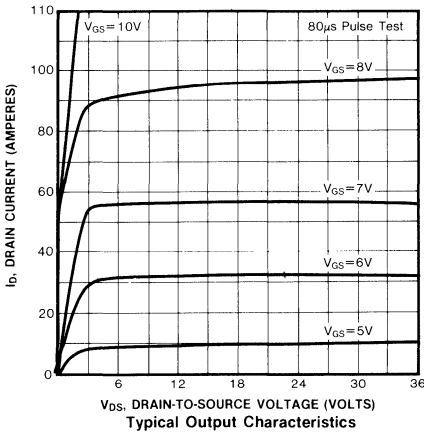
R_{thJC}	Junction-to-Case	MAX	1.0	K/W	
R_{thCS}	Case-to-Sink	TYP	0.5	K/W	Mounting surface flat smooth, and greased
R_{thJA}	Junction-to-Ambient	MAX	80	K/W	Free Air Operation

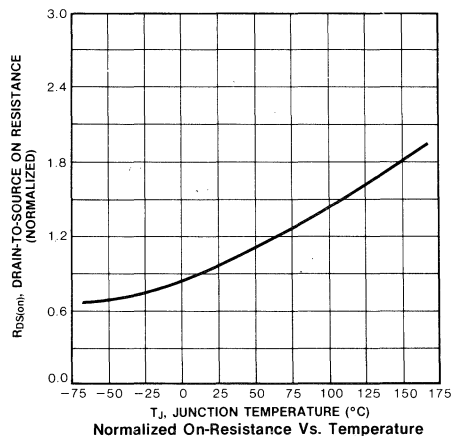
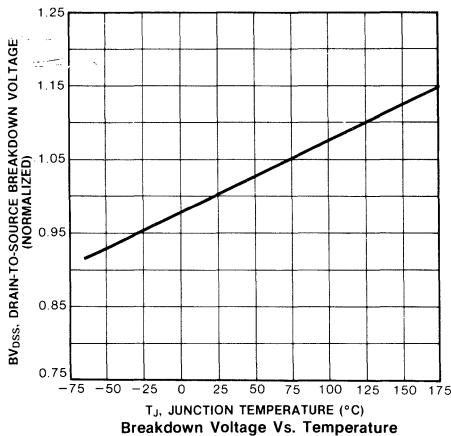
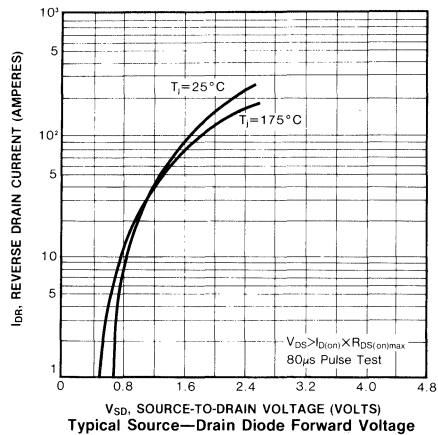
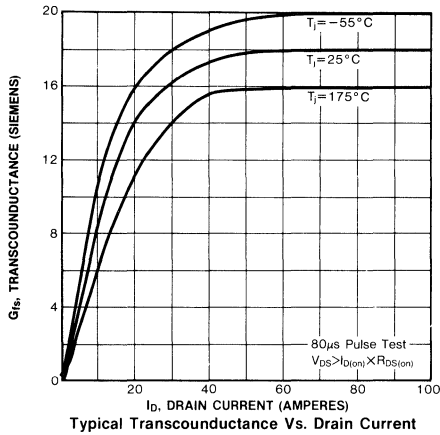
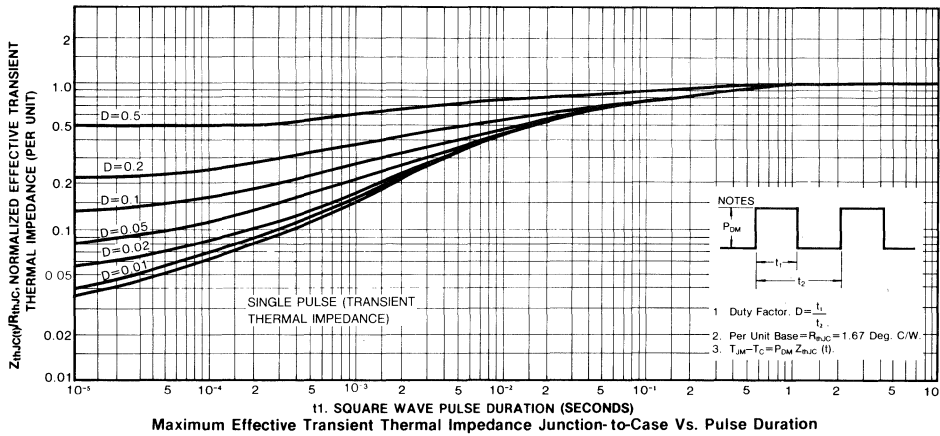
- Notes:** (1) $T_J=25^\circ\text{C}$ to 175°C
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse width limited by max. junction temperature

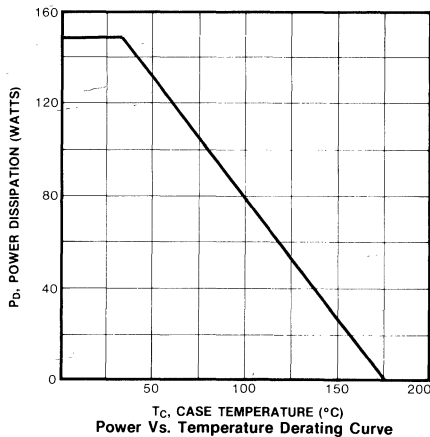
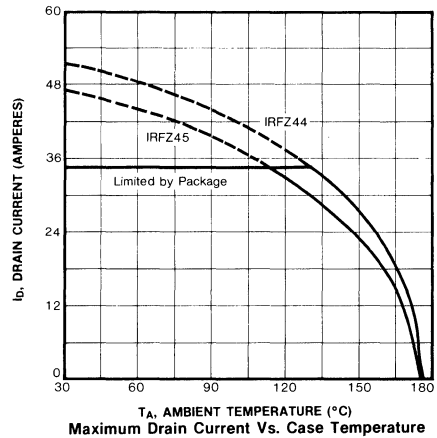
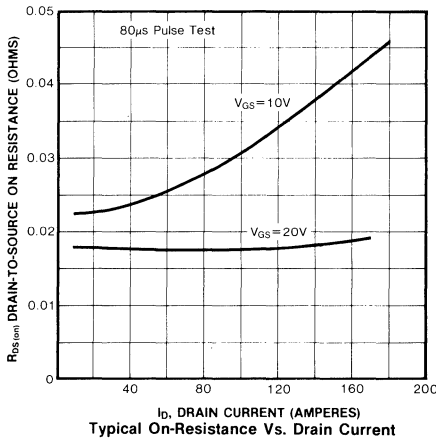
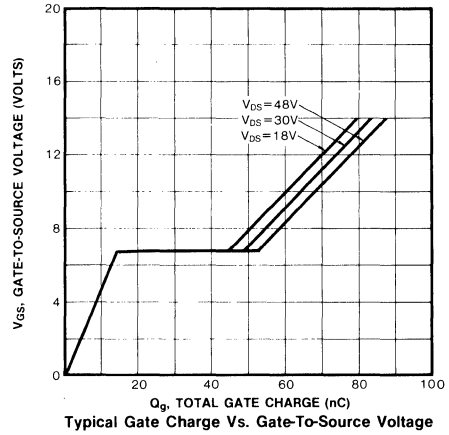
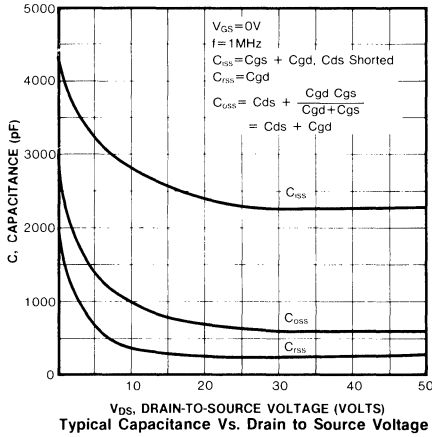
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current IRFZ44/40	—	—	35	A	Modified MOSFET integral reverse P-N junction rectifier
	Current (Body Diode) IRFZ45/42	—	—	35	A	
I_{SM}	Pulse-Source Current IRFZ44/40	—	—	210	A	
	(3) IRFZ45/42	—	—	190	A	
V_{SD}	Diode Forward Voltage All	—	—	2.5	V	$T_C = 25^\circ\text{C}$, $I_S = 35\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	—	250	ns	$T_J = 25^\circ\text{C}$, $I_F = 35\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$

- Notes: (1) $T_J = 25^\circ\text{C}$ to 175°C
(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature



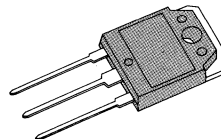




FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

TO-3P



SSH10N70

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$		I_D
		A	STD	
SSH10N70	700V	0.9Ω	1.2Ω	10A

MAXIMUM RATINGS

Characteristic	Symbol	SSH10N70	Unit
Drain-Source Voltage (1)	V_{DSS}	700	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	700	Vdc
Gate-Source Voltage	V_{GS}	± 20	Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	10	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	6.5	Adc
Drain Current—Pulsed (3)	I_{DM}	40	Adc
Gate Current—Pulsed	I_{GM}	± 1.5	Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	795	mJ
Avalanche Current	I_{AS}	10	A
Total Power Dissipation @ $T_C=25^\circ C$	P_D	150	Watts
Derate above $25^\circ C$		1.2	W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300	$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$ (2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=15mH$, $V_{dd}=50V$, $R_G=25\Omega$, starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage	700	—	—	V	$V_{GS}=0V$ $I_D=250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.5	V	$V_{DS}=V_{GS}$, $I_D=1mA$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS}=20V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	$V_{GS}=-20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS}=\text{Max. Rating}$, $V_{GS}=0V$
		—	—	1000	μA	$V_{DS}=\text{Max. Rating} \times 0.8$, $V_{GS}=0V$, $T_C=125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2)	10.0	—	—	A	$V_{DS}>I_{D(on)} \times R_{DS(on)max}$, $V_{GS}=10V$
$R_{DS(on)}$	Static Drain-Source On-State Resistance (2) A (4)	—	—	0.9	Ω	$V_{GS}=10V$, $I_D=5.0A$
	STD	—	—	1.2	Ω	
g_{fs}	Forward Transconductance (2)	7.0	—	—	S	$V_{DS} \geq 50V$, $I_D=5.0A$
C_{iss}	Input Capacitance	—	3678	—	pF	$V_{GS}=0V$, $V_{DS}=25V$, $f=1MHz$
C_{oss}	Output Capacitance	—	293	—	pF	
C_{rss}	Reverse Transfer Capacitance	—	816	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	—	130	ns	$V_{DD}=0.5BV_{DSS}$, $I_D=5.0A$, $Z_O=4.7\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	—	280	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	—	630	ns	
t_f	Fall Time	—	—	210	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	—	240	nC	$V_{GS}=10V$, $I_D=13A$, $V_{DS}=0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	—	80	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	—	160	nC	

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse width limited by max. junction temperature

(4) For ultra low "A" $R_{DS(on)}$, device add "A" suffix to part number

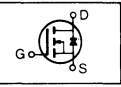
THERMAL RESISTANCE

Symbol	Characteristic		SSH10N70	Unit	
R_{thJC}	Junction-to-Case	MAX	0.83	K/W	
R_{thCS}	Case-to-Sink	TYP	0.24	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	MAX	40	K/W	Free Air Operation

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

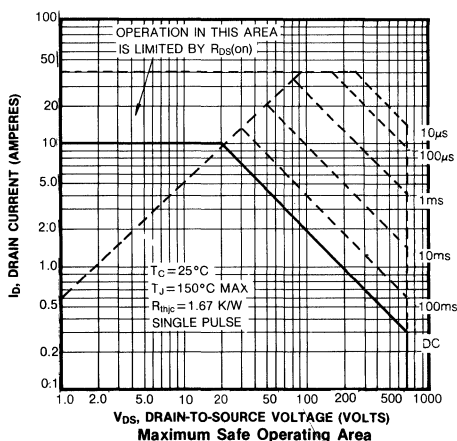
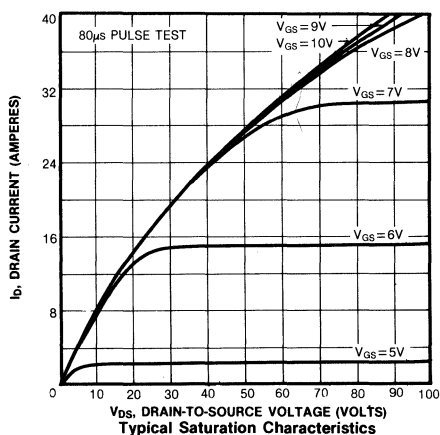
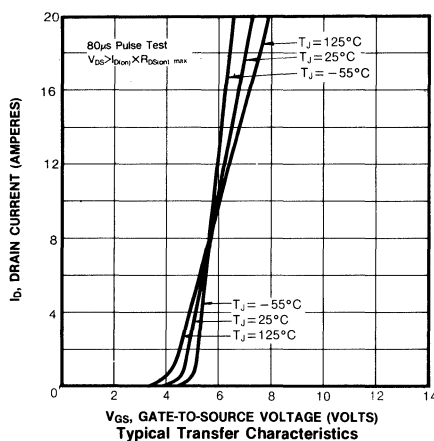
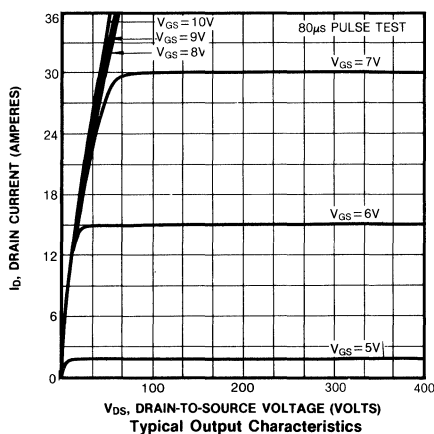
(3) Repetitive rating: Pulse with limited by max. junction temperature

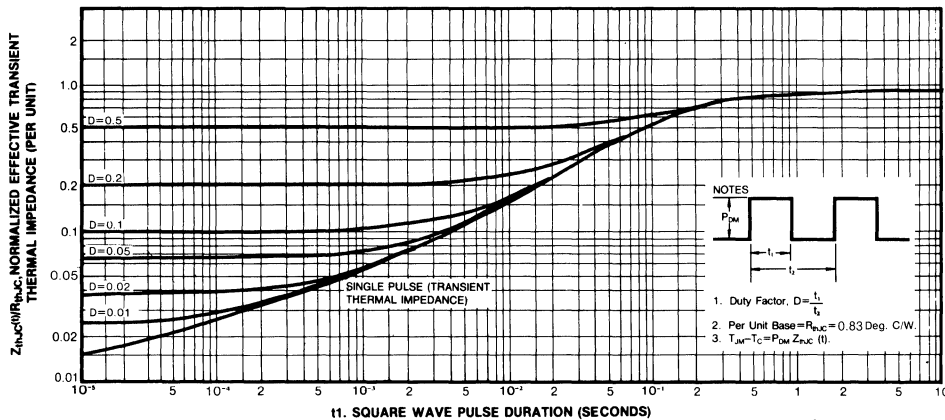
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	10	A	Modified MOSFET showing the integral reverse P-N junction rectifier 
I_{SM}	Pulse Source Current(Body Diode)(3)	—	—	40	A	
V_{SD}	Diode Forward Voltage (2)	—	—	2.5	V	$T_C = 25^\circ\text{C}$, $I_S = 10\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	900	—	ns	$T_J = 150^\circ\text{C}$, $I_F = 10\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{s}$

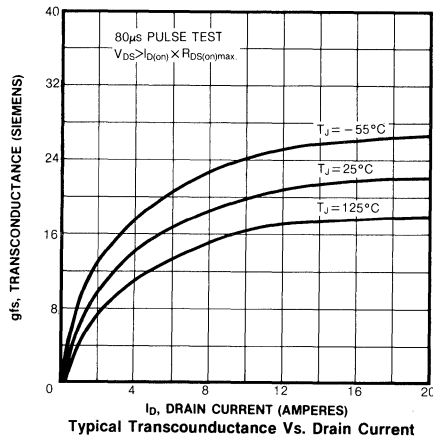
Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

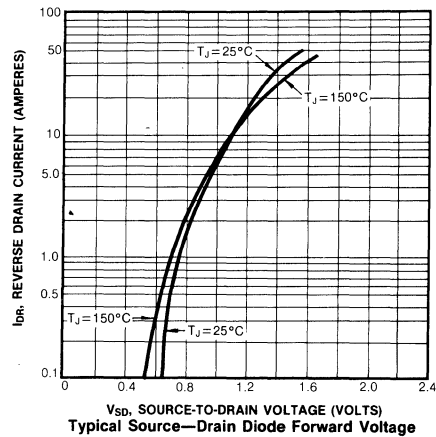




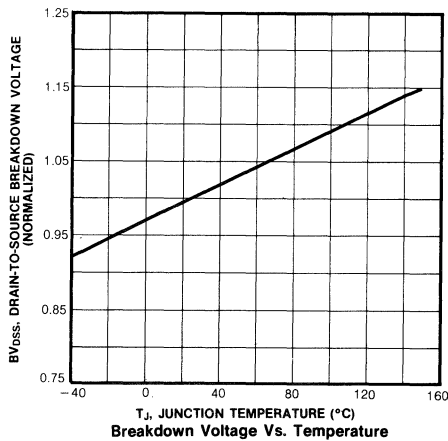
11. SQUARE WAVE PULSE DURATION (SECONDS)
Maximum Effective Transient Thermal Impedance Junction-to-Case Vs. Pulse Duration



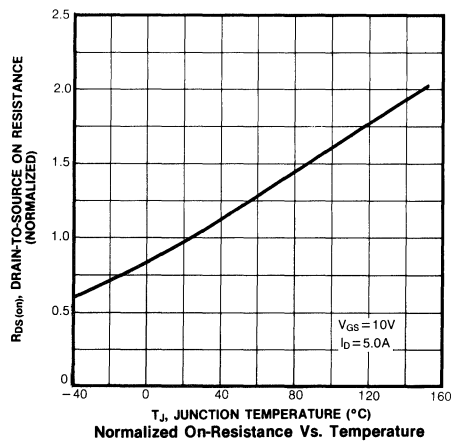
Typical Transconductance Vs. Drain Current



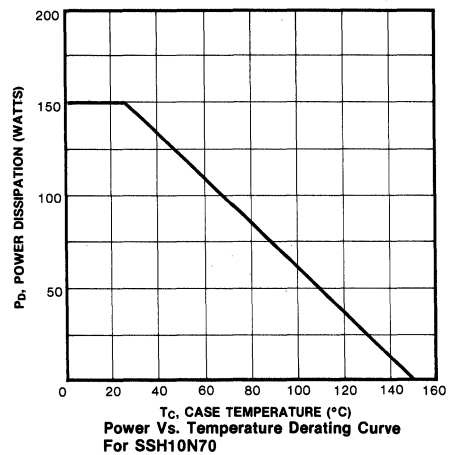
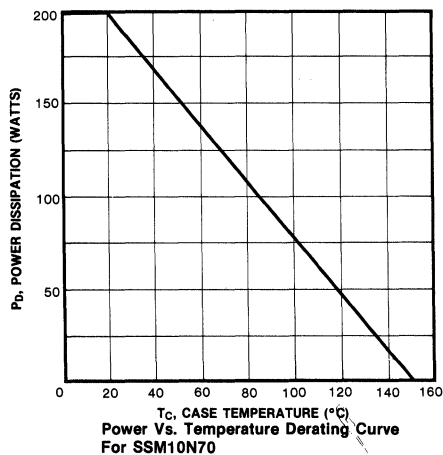
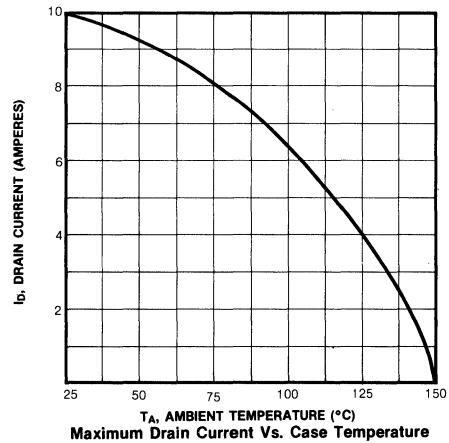
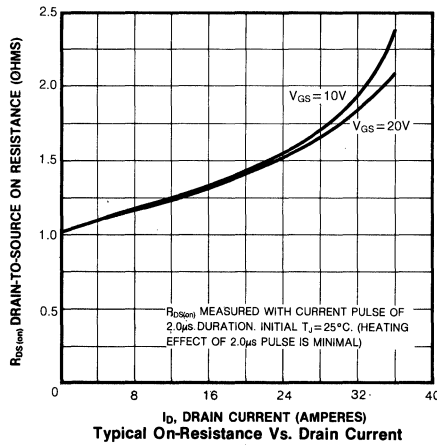
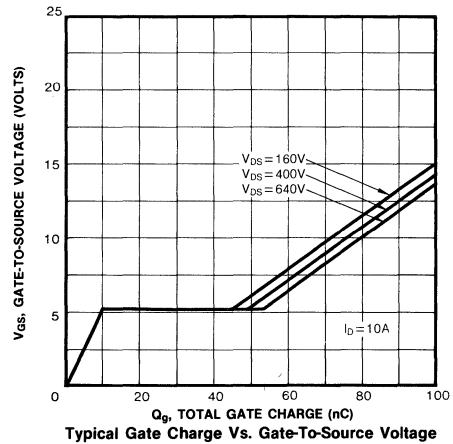
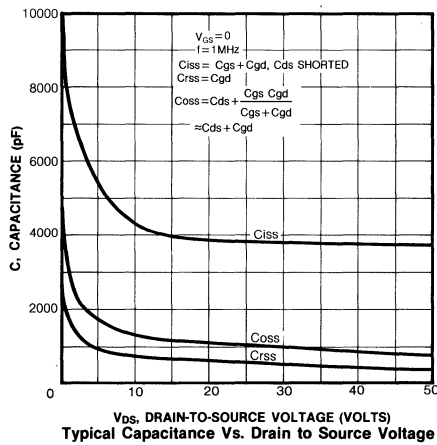
Typical Source-Drain Diode Forward Voltage



Breakdown Voltage Vs. Temperature



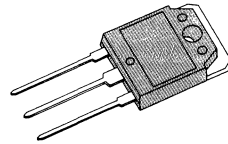
Normalized On-Resistance Vs. Temperature



FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

TO-3P



SSH20N45/20N50

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$		I_D
		A	STD	
SSH20N45	450V	0.25Ω	0.35Ω	20A
SSH20N50	500V	0.25Ω	0.35Ω	20A

MAXIMUM RATINGS

Characteristic	Symbol	SSH20N45	SSH20N50	Unit
Drain-Source Voltage (1)	V_{DSS}	450	500	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	450	500	Vdc
Gate-Source Voltage	V_{GS}	± 20		Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	20		Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	13		Adc
Drain Current—Pulsed (3)	I_{DM}	80		Adc
Gate Current—Pulsed	I_{GM}	± 1.5		Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	960		mJ
Avalanche Current	I_{AS}	20		A
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	150 1.2		Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300		$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$ (2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=4.3mH$, $V_{dd}=50V$, $R_G=25\Omega$, starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-Source Breakdown Voltage SSH20N45	450	—	—	V	$V_{GS}=0V$
	SSH20N50	500	—	—	V	$I_D=250\mu A$
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.5	V	$V_{DS}=V_{GS}$, $I_D=1mA$
I _{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS}=20V$
I _{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	$V_{GS}=-20V$
I _{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS}=\text{Max. Rating}$, $V_{GS}=0V$
		—	—	1000	μA	$V_{DS}=\text{Max. Rating}\times 0.8$, $V_{GS}=0V$, $T_C=125^\circ\text{C}$
I _{D(on)}	On-State Drain-Source Current (2)	20	—	—	A	$V_{DS}\geq 7V$, $V_{GS}=10V$
R _{DS(on)}	Static Drain-Source On-State Resistance (2) A (4)	—	—	0.25	Ω	$V_{GS}=10V$, $I_D=13A$
	STD	—	—	0.35	Ω	
g _{fs}	Forward Transconductance (2)	7.0	—	—	Ω	$V_{DS}\geq 50V$, $I_D=13A$
C _{iss}	Input Capacitance	—	4260	—	pF	$V_{GS}=0V$, $V_{DS}=25V$, $f=1.0MHz$
C _{oss}	Output Capacitance	—	438	—	pF	
C _{rss}	Reverse Transfer Capacitance	—	125	—	pF	
t _{d(on)}	Turn-On Delay Time	—	—	130	ns	$V_{DD}=0.5BV_{DSS}$, $I_D=10A$, $Z_O=4.7\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t _r	Rise Time	—	—	280	ns	
t _{d(off)}	Turn-Off Delay Time	—	—	630	ns	
t _f	Fall Time	—	—	210	ns	
Q _g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	—	240	nC	$V_{GS}=10V$, $I_D=25A$, $V_{DS}=0.8\text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature.)
Q _{gs}	Gate-Source Charge	—	—	80	nC	
Q _{gd}	Gate-Drain ("Miller") Charge	—	—	160	nC	

THERMAL RESISTANCE

Symbol	Characteristic		SSH20N45/50	Unit	
R _{thJC}	Junction-to-Case	MAX	0.83	K/W	
R _{thCS}	Case-to-Sink	TYP	0.24	K/W	Mounting surface flat, smooth, and greased
R _{thJA}	Junction-to-Ambient	MAX	40	K/W	Free Air Operation

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

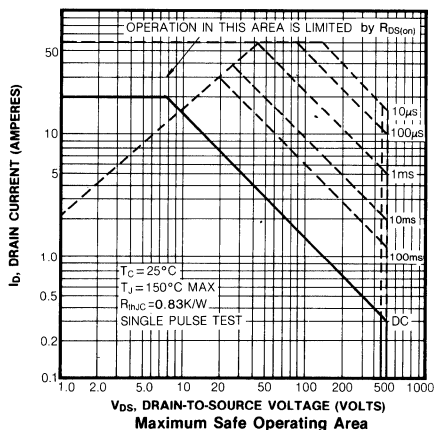
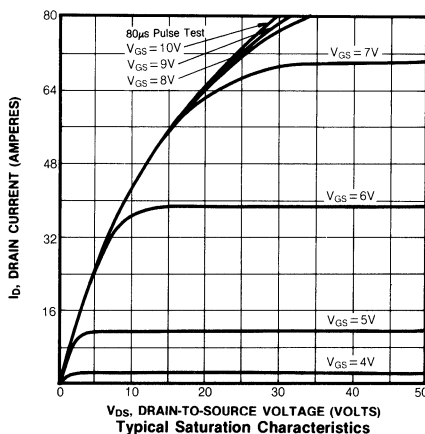
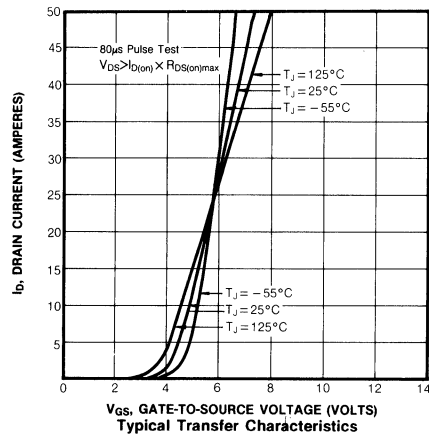
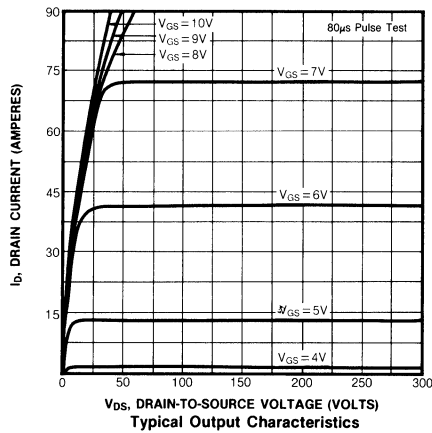
(3) Repetitive rating: Pulse width limited by max. junction temperature

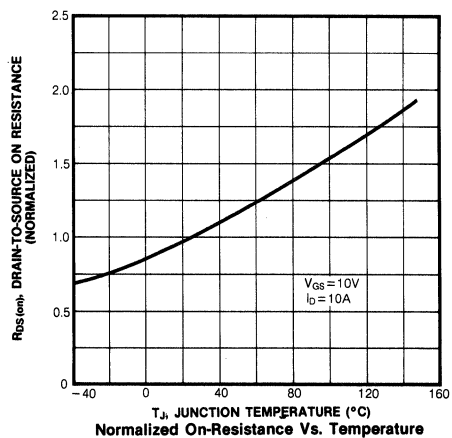
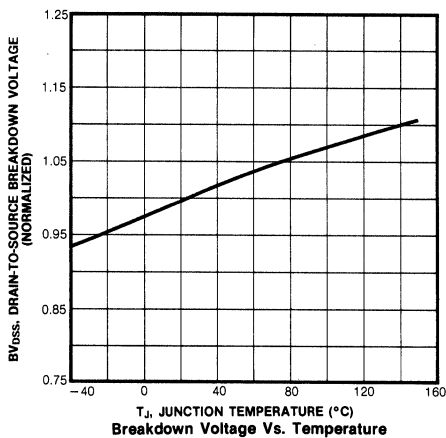
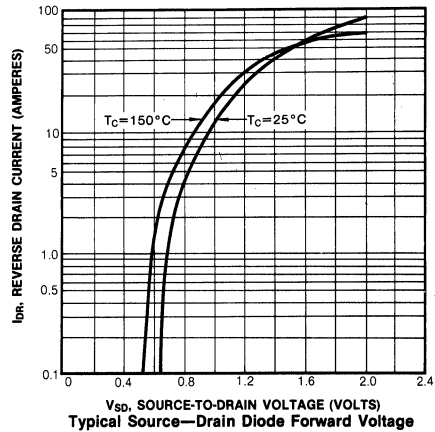
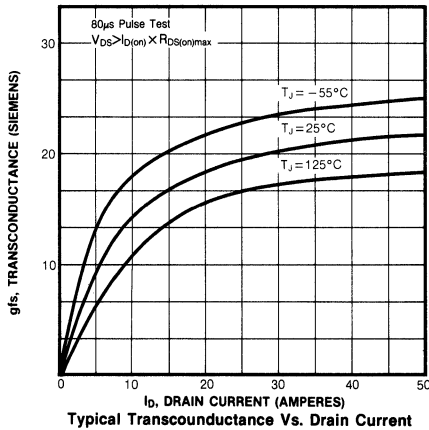
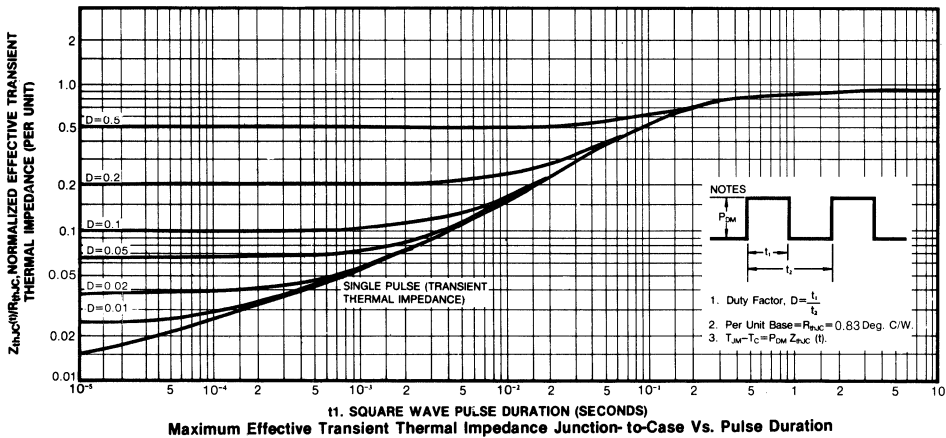
(4) For Ultra low "A" R_{DS(on)}, device add "A" suffix to part number

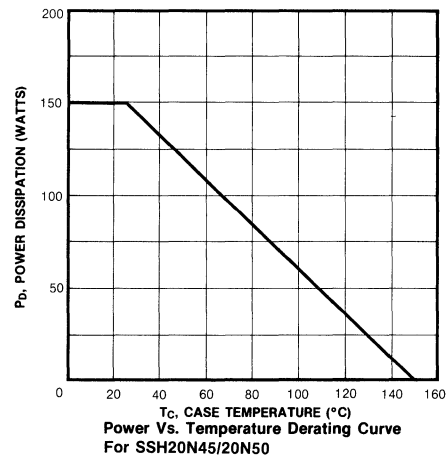
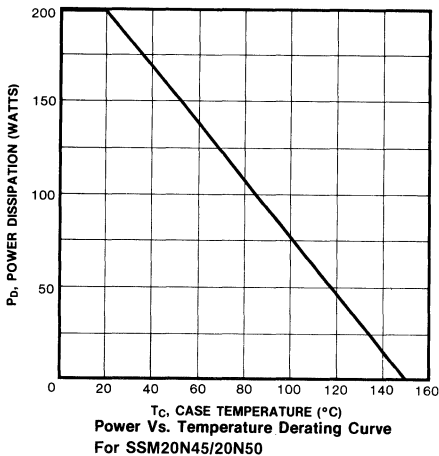
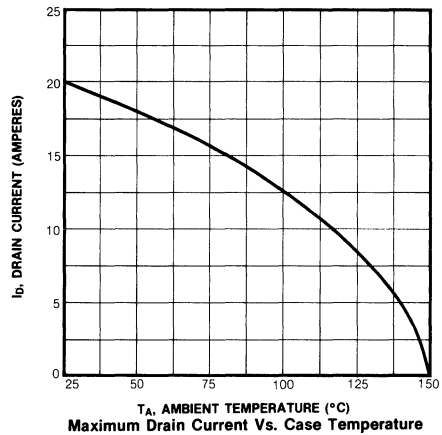
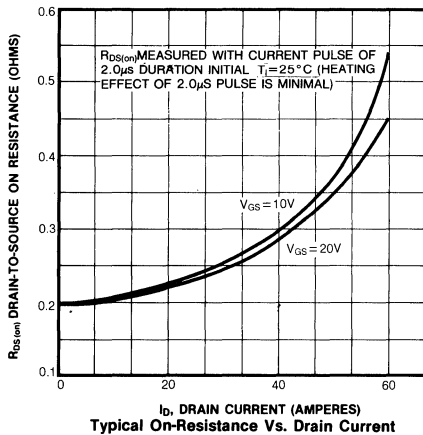
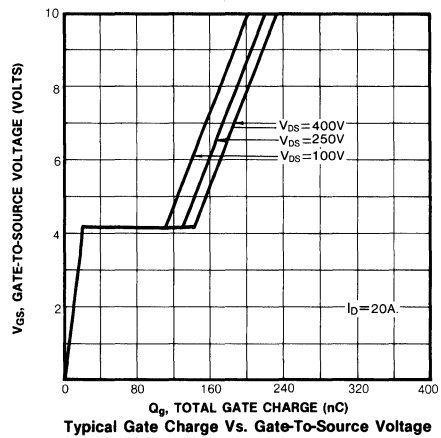
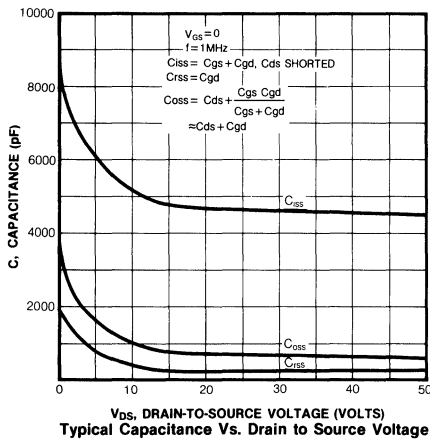
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	20	A	Modified MOSFET showing the integral reverse P-N junction rectifier
I_{SM}	Pulse Source Current(Body Diode)(3)	—	—	80	A	
V_{SD}	Diode Forward Voltage (2)	—	—	2.5	V	$T_C = 25^\circ\text{C}$, $I_S = 20\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	900	—	ns	$T_J = 150^\circ\text{C}$, $I_F = 20\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$

Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
 (3) Repetitive rating: Pulse with limited by max. junction temperature



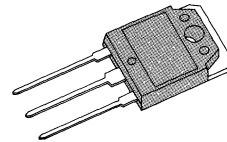




FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability
- TO-220 package

TO-3P



SSH60N06/60N10

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$		I_D
		A	STD	
SSH60N06	60V	0.025Ω	0.03Ω	60A
SSH60N10	100V	0.025Ω	0.03Ω	60A

MAXIMUM RATINGS

Characteristic	Symbol	SSH60N06	SSH60N10	Unit
Drain-Source Voltage (1)	V_{DSS}	60	100	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	60	100	Vdc
Gate-Source Voltage	V_{GS}	± 20		Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	60		Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	40		Adc
Drain Current—Pulsed (3)	I_{DM}	180		Adc
Gate Current—Pulsed	I_{GM}	± 1.5		Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	790		mJ
Avalanche Current	I_{AS}	60.0		A
Total Power Dissipation @ $T_C=25^\circ C$	P_D	150		Watts
Derate above $25^\circ C$		1.2		W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300		$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=0.33mH$, $V_{dd}=25V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-Source Breakdown Voltage SSH60N06	60	—	—	V	V _{GS} =0V
	SSH60N10	100	—	—	V	I _D =250μA
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.5	V	V _{DS} =V _{GS} , I _D =1mA
I _{GSS}	Gate-Source Leakage Forward	—	—	100	nA	V _{GS} =20V
I _{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	V _{GS} =-20V
I _{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	V _{DS} =Max. Rating, V _{GS} =0V
		—	—	1000	μA	V _{DS} =Max. Rating×0.8, V _{GS} =0V, T _C =125°C
I _{D(on)}	On-State Drain-Source Current (2)	60	—	—	A	V _{DS} ≥1.8V, V _{GS} =10V
R _{DS(on)}	Static Drain-Source On-State Resistance (2) "A" (4)	—	—	0.025	Ω	V _{GS} =10V, I _D =30A
	STD	—	—	0.03	Ω	
g _{fs}	Forward Transconductance (2)	7.0	—	—	Ω	V _{DS} ≥50V, I _D =30A
C _{iss}	Input Capacitance	—	4800	—	pF	V _{GS} =0V, V _{DS} =25V, f=1MHz
C _{oss}	Output Capacitance	—	950	—	pF	
C _{rss}	Reverse Transfer Capacitance	—	395	—	pF	
t _{d(on)}	Turn-On Delay Time	—	—	126	ns	V _{DD} =0.5BV _{DSS} , I _D =30A, Z _O =50Ω (MOSFET switching times are essentially independent of operating temperature)
t _r	Rise Time	—	—	280	ns	
t _{d(off)}	Turn-Off Delay Time	—	—	630	ns	
t _f	Fall Time	—	—	210	ns	
Q _g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	—	80	nC	V _{GS} =10V, I _D =60A, V _{DS} =0.8 Max. Rating (Gate charge is essentially independent of operating temperature.)
Q _{gs}	Gate-Source Charge	—	—	28	nC	
Q _{gd}	Gate-Drain ("Miller") Charge	—	—	14	nC	

Notes: (1) T_J=25°C to 150°C

(2) Pulse test: Pulse width≤300μs, Duty Cycle≤2%

(3) Repetitive rating: Pulse width limited by max. junction temperature

(4) For ultra low "A" R_{DS(on)}, device add "A" suffix to part number

THERMAL RESISTANCE

Symbol	Characteristic		SSH60N06/10	Unit	
R _{thJC}	Junction-to-Case	MAX	0.83	K/W	
R _{thCS}	Case-to-Sink	TYP	0.24	K/W	Mounting surface flat, smooth, and greased
R _{thJA}	Junction-to-Ambient	MAX	40	K/W	Free Air Operation

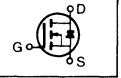
Notes: (1) T_J=25°C to 150°C

(2) Pulse test: Pulse width≤300μs, Duty Cycle≤2%

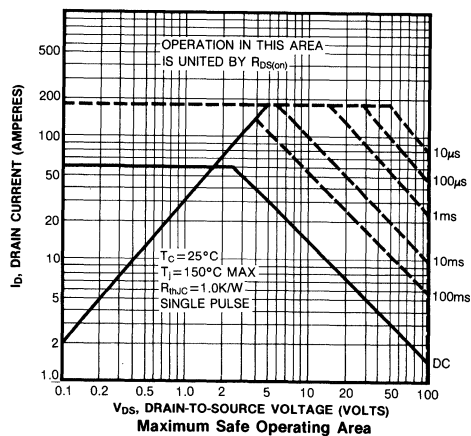
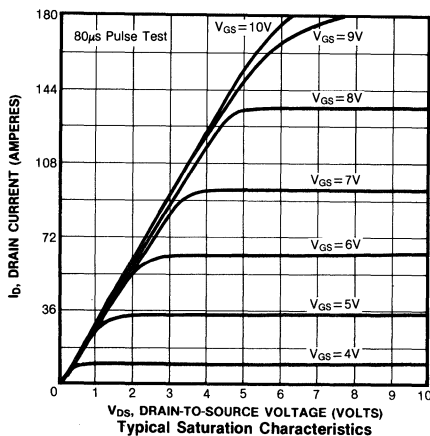
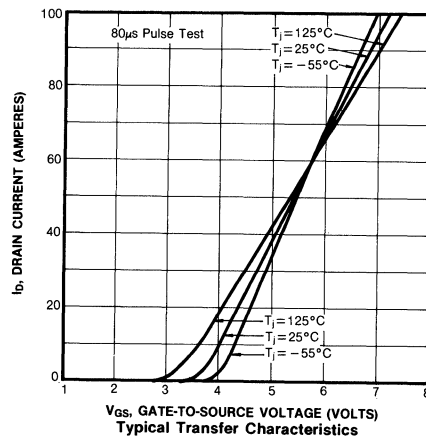
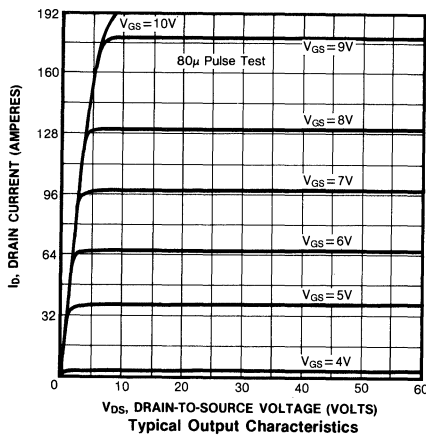
(3) Repetitive rating: Pulse with limited by max. junction temperature

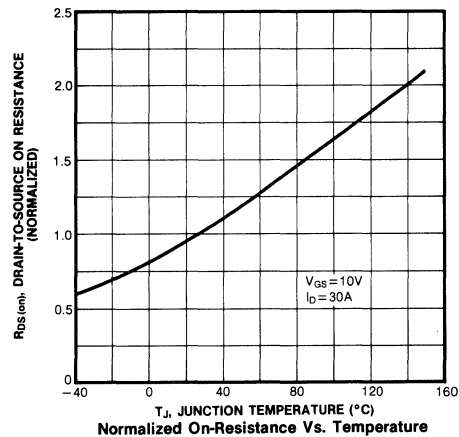
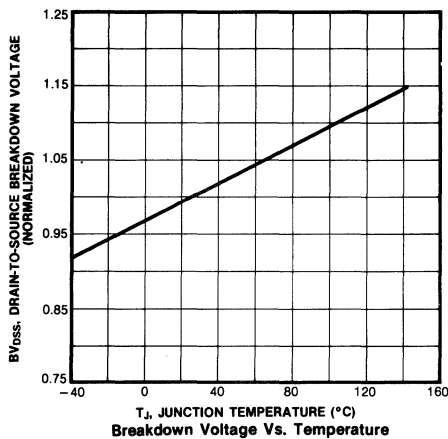
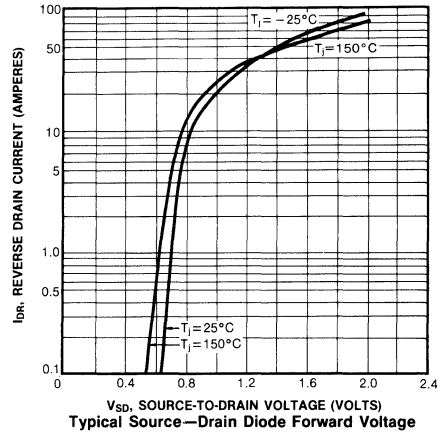
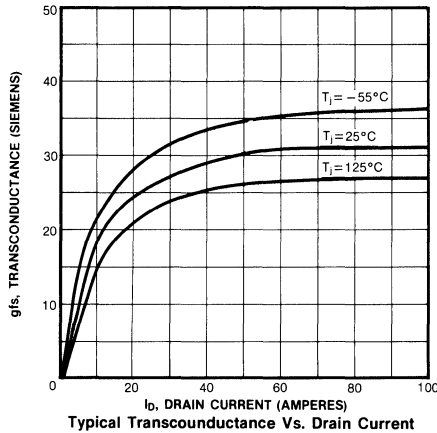
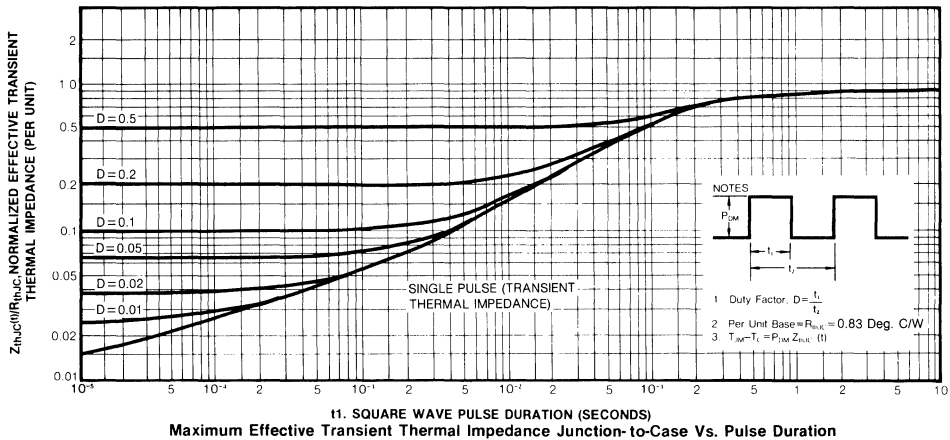
(4) For ultra low "A" R_{DS(on)}, device and "A" suffix to part number

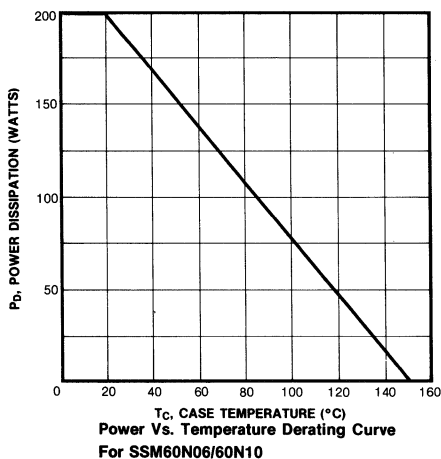
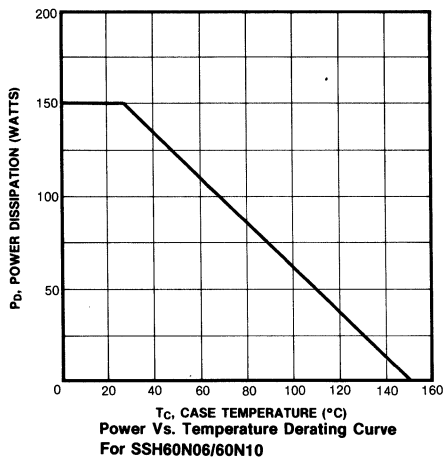
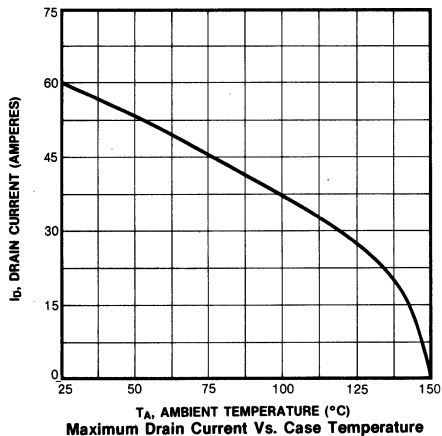
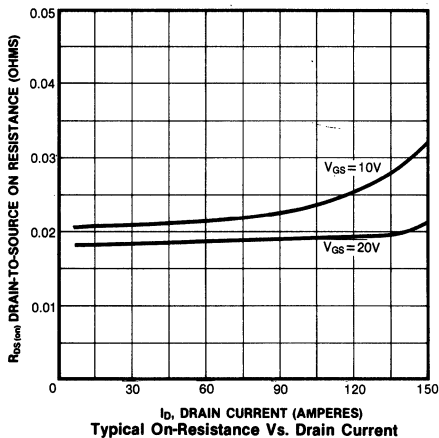
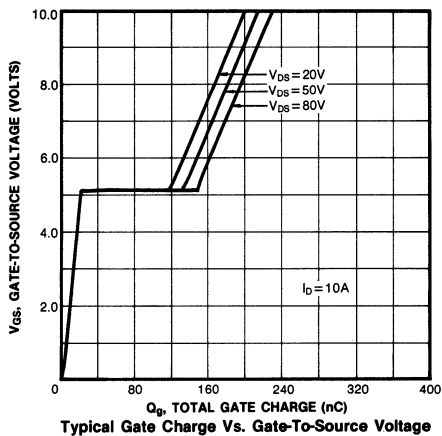
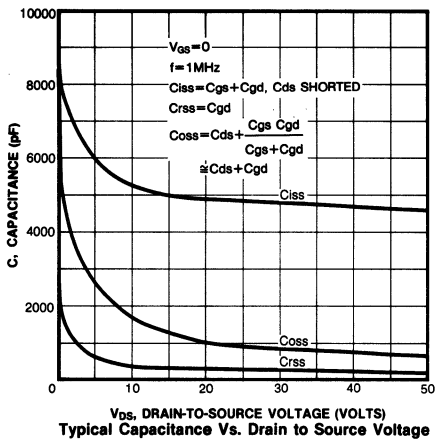
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	60	A	Modified MOSFET showing the integral reverse P-N junction rectifier 
I_{SM}	Pulse Source Current(Body Diode)(3)	—	—	180	A	
V_{SD}	Diode Forward Voltage (2)	—	—	2.5	V	$T_C=25^\circ\text{C}$, $I_S=60\text{A}$, $V_{GS}=0\text{V}$
t_{rr}	Reverse Recovery Time	—	1200	—	ns	$T_J=150^\circ\text{C}$, $I_F=60\text{A}$, $dI_F/dt=100\text{A}/\mu\text{S}$

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
 (3) Repetitive rating: Pulse with limited by max. junction temperature



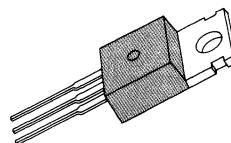




FEATURES

- Lower $R_{DS(ON)}$
- Excellent voltage stability
- Fast switching time
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Improved high temperature reliability

TO-220



1. Gate 2. Drain 3. Source

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
SSP1N60	600V	12Ω	1.0A
SSP1N55	550V	12Ω	1.0A

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	SSP1N60	SSP1N55	Units
Drain-Source Voltage (1)	V_{DSS}	600	550	Vdc
Drain-Gate Voltage ($R_{GS} = 1.0M\Omega$) (1)	V_{DGR}	600	550	Vdc
Gate-Source Voltage	V_{GS}	± 20		Vdc
Continuous Drain Current $T_C = 25^\circ C$	I_D	1.0		Adc
Drain Current — Pulsed (3)	I_{DM}	3.0		Adc
Total Power Dissipation at $T_C = 25^\circ C$ Derate above $25^\circ C$	P_D	50 0.4		Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ C$
Maximum Lead Temp, for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300		$^\circ C$

Notes: (1) $T_J = 25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse width limited by max. junction temperature

ELECTRICAL CHARACTERISTIC (T_C = 25°C unless otherwise specified)

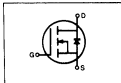
Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
BV _{DSS}	Drain-Source Breakdown Voltage SSP1N60 SSP1N55	600 550	— —	— —	V V	V _{GS} = 0V, I _D = 250μA
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
I _{GSS}	Gate-Source Leakage Forward	—	—	100	nA	V _{GS} = 20V
I _{GSS}	Gate-Source Leakage Reverse	—	—	- 100	nA	V _{GS} = - 20V
I _{DSS}	Zero Gate Voltage Drain Current	— —	— —	250 1000	μA	V _{DS} = Max. Rating V _{GS} = 0V, V _{DS} = 0.8 Max. Rating, T _C = 125°C
I _{D(on)}	On-State Drain-Source Current (2)	1			A	V _{DS} ≥ 12V, V _{GS} = 10V
R _{DS(on)}	Static Drain-Source On-State Resistance (2)	— —	— —	12	Ω	V _{GS} = 10V, I _D = 0.5A
g _{fs}	Forward Transconductance (2)	0.5	—	—	Ω	V _{DS} > 15V, I _D = 0.5A
C _{iss}	Input Capacitance	—	250	300	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0MHz
C _{oss}	Output Capacitance	—	25	50	pF	
C _{rss}	Reverse Transfer Capacitance	—	10	20	pF	
t _{d(on)}	Turn-On Delay Time	—	12	20	ns	V _{DD} = 0.5 BV _{DSS} , I _D = 0.5A, Z _O = 50Ω (MOSFET switching times are essentially independent of operating temperature)
t _r	Rise Time	—	4	15	ns	
t _{d(off)}	Turn-Off Delay Time	—	30	60	ns	
t _f	Fall Time	—	10	30	ns	
Q _g	Total Gate Charge (Gate-Source Pulse Gate-Drain)	—	20	—	nC	V _{GS} = 10V, I _D = 1.0A V _{DS} = 0.8 Max. Rating (Gate charge is essentially independent of operating temperature)
Q _{gs}	Gate-Source Charge	—	3	—	nC	
Q _{gd}	Gate-Drain ("Miller") Charge	—	9	—	nC	

THERMAL RESISTANCE

R _{thJC}	Junction-to-Case	MAX	2.5	K/W	
R _{thJA}	Junction-to-Ambient	MAX	80	K/W	Free Air Opration

Notes: (1) T_J = 25°C to 150°C
(2) Pulse test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
(3) Repetitive rating: Pulse width limited by max. junction temperature

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
I_S	Continuous Source Current (Body Diode) SSP1N60 SSP1N55	—	—	1.0	A	Modified MOSFET integral reverse P-N junction rectifier 
I_{SM}	Pulse-Source Current (3) SSP1N60 SSP1N55	—	—	3.0	A	
V_{SD}	Diode Forward Voltage (2)	—	—	1.15	V	$T_c=25^\circ\text{C}$, $I_S=1.0\text{A}$, $V_{GS}=0\text{V}$
T_{rr}	Reverse Recovery Time	—	350	—	ns	$T_J=25^\circ\text{C}$, $I_F=1.0\text{A}$, $dI_F/dt=100\text{A}/\mu\text{s}$

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C

(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$

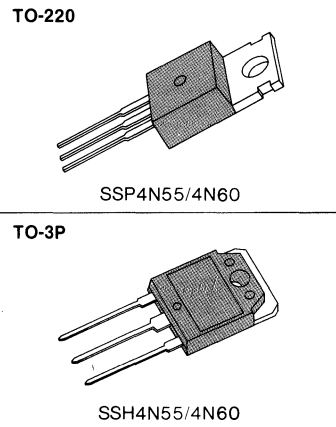
(3) Repetitive rating: Pulse width limited by max. junction temperature

FEATURES

- Lower $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$		I_D
		A	STD	
SSP4N55/SSH4N55	550V	2.5Ω	3.0Ω	4A
SSP4N60/SSH4N60	600V	2.5Ω	3.0Ω	4A



MAXIMUM RATINGS

Characteristic	Symbol	SSP4N55 SSH4N55	SSP4N60 SSH4N60	Unit
Drain-Source Voltage (1)	V_{DSS}	550	600	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	550	600	Vdc
Gate-Source Voltage	V_{GS}	± 20		Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	4	4	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	2.5	2.5	Adc
Drain Current—Pulsed (3)	I_{DM}	16	16	Adc
Gate Current—Pulsed	I_{GM}	± 1.5		Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	358		mJ
Avalanche Current	I_{AS}	4		A
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	75 0.6		Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300		$^\circ C$

- Notes:** (1) $T_J=25^\circ C$ to $150^\circ C$
 (2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
 (3) Repetitive rating: Pulse with limited by max. junction temperature
 (4) $L=42 mH$, $V_{dd}=50V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage SSP4N60/SSH4N60	600	—	—	V	$V_{GS}=0V$ $I_D=250\mu A$
	SSP4N55/SSH4N55	550	—	—	V	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.5	V	$V_{DS}=V_{GS}$, $I_D=1mA$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS}=20V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	$V_{GS}=-20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS}=\text{Max. Rating}$, $V_{GS}=0V$
		—	—	1000	μA	$V_{DS}=\text{Max. Rating} \times 0.8$, $V_{GS}=0V$, $T_C=125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2)	4	—	—	A	$V_{DS} \geq 12V$, $V_{GS}=10V$
$R_{DS(on)}$	Static Drain-Source On-State A (4) Resistance (2) STD	—	—	2.5	Ω	$V_{GS}=10V$, $I_D=2.0A$
		—	—	3.0	Ω	
g_{fs}	Forward Transconductance (2)	2.0	3.1	—	Ω	$V_{DS} \geq 50V$, $I_D=2.0A$
C_{iss}	Input Capacitance	—	720	—	pF	$V_{GS}=0V$, $V_{DS}=25V$, $f=1.0MHz$
C_{oss}	Output Capacitance	—	40	—	pF	
C_{rss}	Reverse Transfer Capacitance	—	—	40	pF	
$t_{d(on)}$	Turn-On Delay Time	—	—	40	ns	$V_{DD}=0.5BV_{DSS}$, $I_D=2.0A$, $Z_O=15\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	—	150	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	—	100	ns	
t_f	Fall Time	—	—	60	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	25	—	nC	$V_{I0}=10V$, $I_D=8.0A$, $V_{DS}=0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	—	15	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	6.0	—	nC	

THERMAL RESISTANCE

Symbol	Characteristic		SSP4N50/60	SSH4N55/60		
R_{thJC}	Junction-to-Case	MAX	1.67	1.67	K/W	
R_{thCS}	Case-to-Sink	TYP	0.5	0.24	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	MAX	80	40	K/W	Free Air Operation

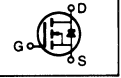
Notes: (1) $T_J=25^\circ\text{C}$ to 150°C

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

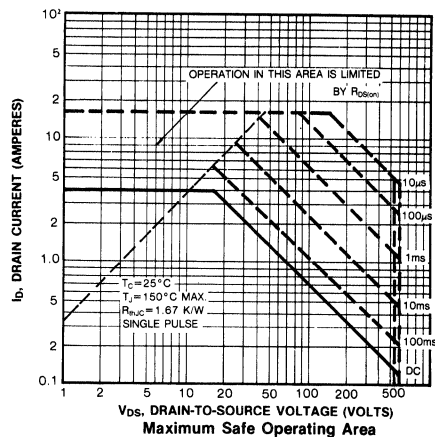
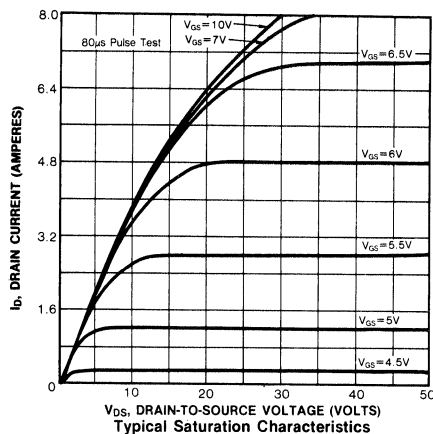
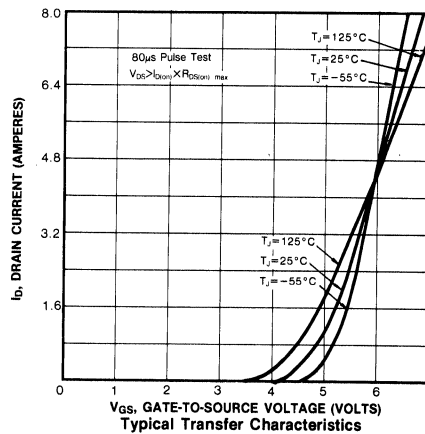
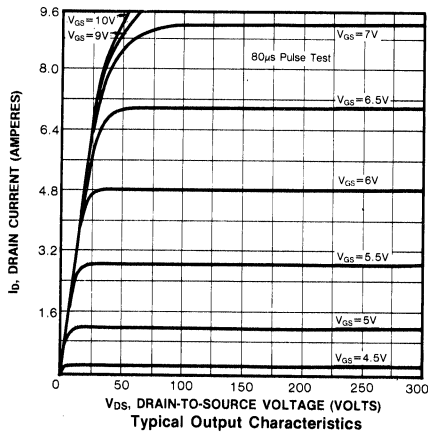
(3) Repetitive rating: Pulse width limited by max. junction temperature

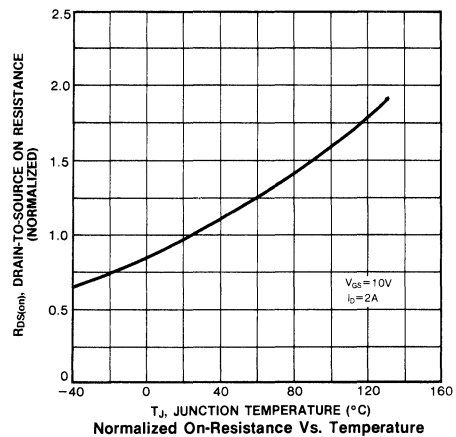
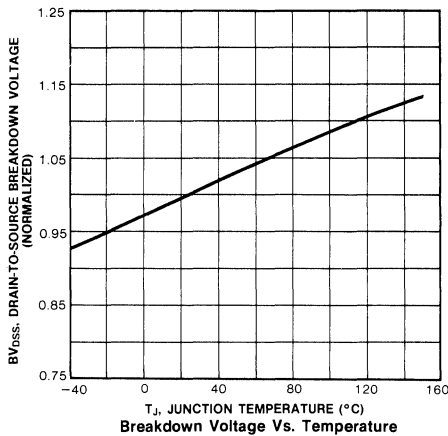
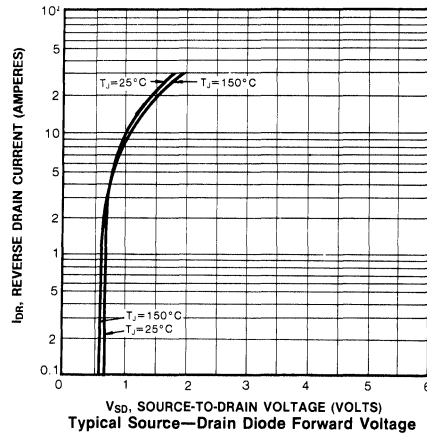
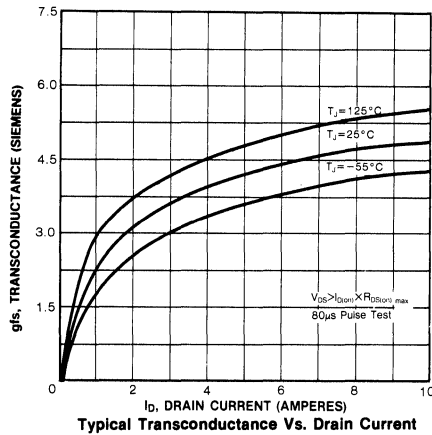
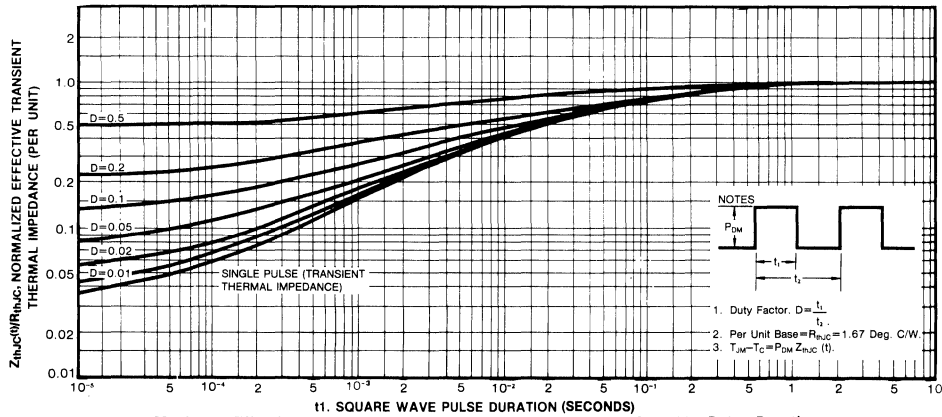
(4) For Ultra low "A" $R_{DS(on)}$, device add "A" suffix to part number

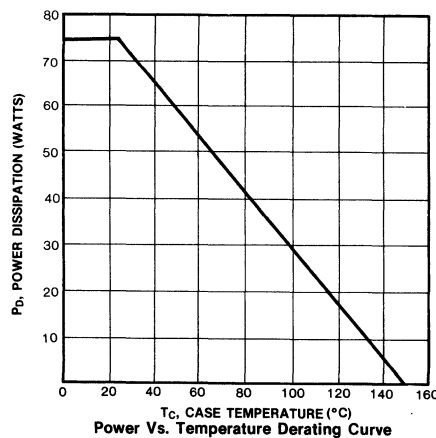
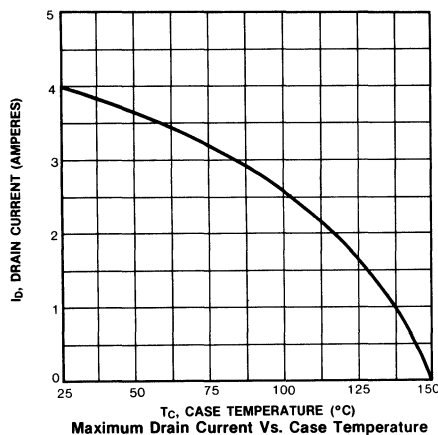
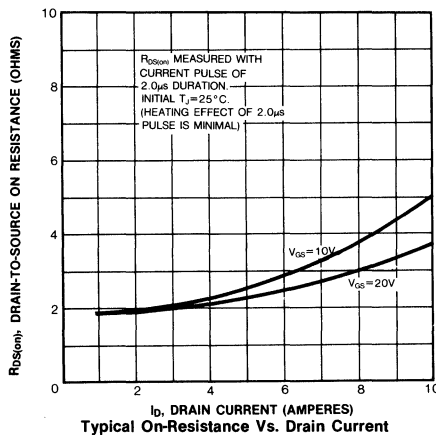
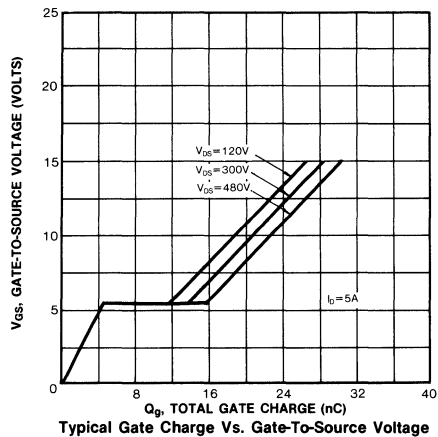
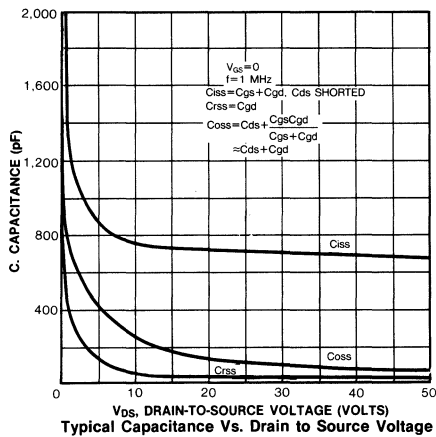
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	4.0	A	Modified MOSFET showing the integral reverse P-N junction rectifier 
I_{SM}	Pulse Source Current(Body Diode)(3)	—	—	16.0	A	
V_{SD}	Diode Forward Voltage (2)	—	—	1.5	V	$T_C=25^\circ\text{C}$, $I_S=4.0\text{A}$, $V_{GS}=0\text{V}$
t_{rr}	Reverse Recovery Time	—	600	—	μs	$T_J=150^\circ\text{C}$, $I_F=8.0\text{A}$, $dI_F/dt=100\text{A}/\mu\text{s}$

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature







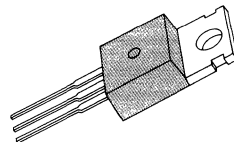
FEATURES

- Lower $R_{DS(ON)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

PRODUCT SUMMARY

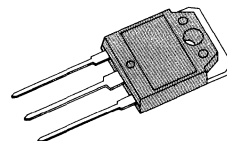
Part Number	V_{DS}	$R_{DS(on)}$		I_D
		A	STD	
SSP4N70 SSH4N70	700V	2.5Ω	3.5Ω	4.0A

TO-220



SSP4N70

TO-3P



SSH4N70

MAXIMUM RATINGS

Characteristic	Symbol	SSP4N70 SSH4N70	Unit
Drain-Source Voltage (1)	V_{DSS}	700	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	700	Vdc
Gate-Source Voltage	V_{GS}	± 20	Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	4.0	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	4.0	Adc
Drain Current—Pulsed (3)	I_{DM}	2.5	Adc
Gate Current—Pulsed	I_{GM}	± 1.5	Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	280	mJ
Avalanche Current	I_{AS}	4	A
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	125 1.0	Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300	$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse with limited by max. junction temperature

(4) $L=33mH$, $V_{dd}=50V$, $R_G=25\Omega$, starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage	700	—	—	V	$V_{GS}=0V$ $I_D=250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.5	V	$V_{DS}=V_{GS}$, $I_D=1mA$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS}=20V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	$V_{GS}=-20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS}=\text{Max. Rating}$, $V_{GS}=0V$
		—	—	1000	μA	$V_{DS}=\text{Max. Rating} \times 0.8$, $V_{GS}=0V$, $T_C=125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2)	4	—	—	A	$V_{DS}>I_{D(on)} \times R_{DS(on)max}$, $V_{GS}=10V$
$R_{DS(on)}$	Static Drain-Source On-State Resistance (2) A (4)	—	—	2.5	Ω	$V_{GS}=10V$, $I_D=2.0A$
	STD	—	—	3.5	Ω	
g_{fs}	Forward Transconductance (2)	2.5	3.6	—	Ω	$V_{DS} \geq 50V$, $I_D=2.0A$
C_{iss}	Input Capacitance	—	1457	—	pF	$V_{GS}=0V$, $V_{DS}=25V$, $f=1.0MHz$
C_{oss}	Output Capacitance	—	130	—	pF	
C_{rss}	Reverse Transfer Capacitance	—	38.8	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	—	60	ns	$V_{DD}=0.5BV_{DSS}$, $I_D=2.0A$, $Z_O=4.7\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	—	150	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	—	300	ns	
t_f	Fall Time	—	—	130	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	—	40	nC	$V_{GS}=10V$, $I_D=5.0A$, $V_{DS}=0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	15	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	25	—	nC	

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

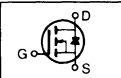
(3) Repetitive rating: Pulse width limited by max. junction temperature

(4) For ultra low "A" $R_{DS(on)}$, device add "A" suffix to part number

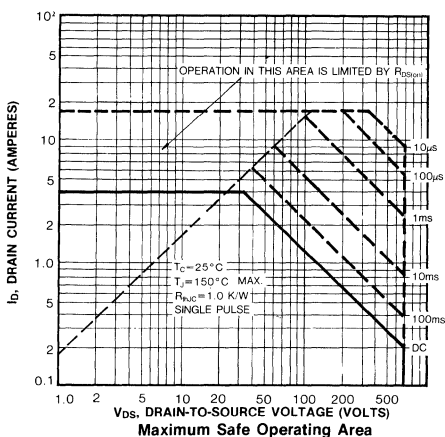
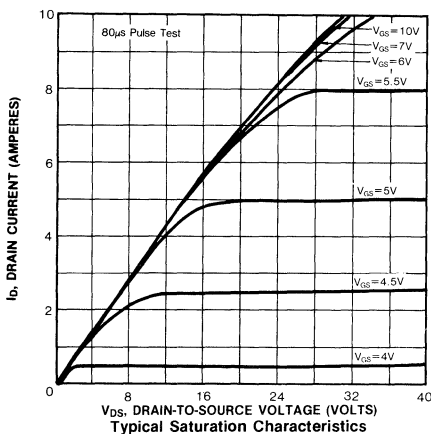
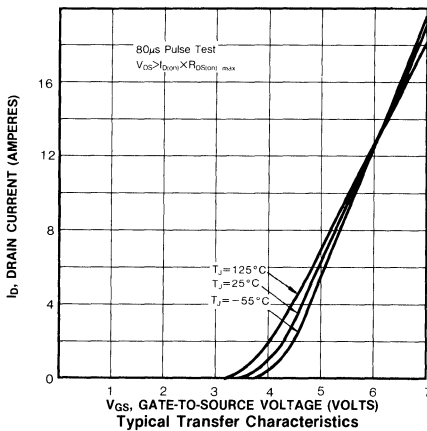
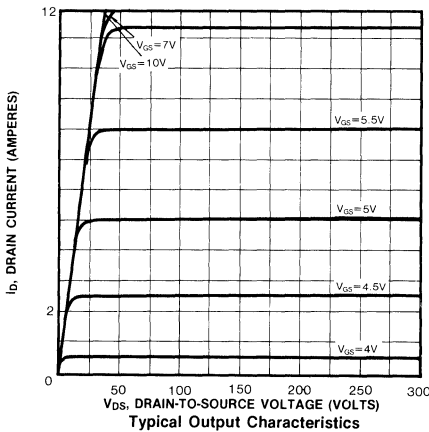
THERMAL RESISTANCE

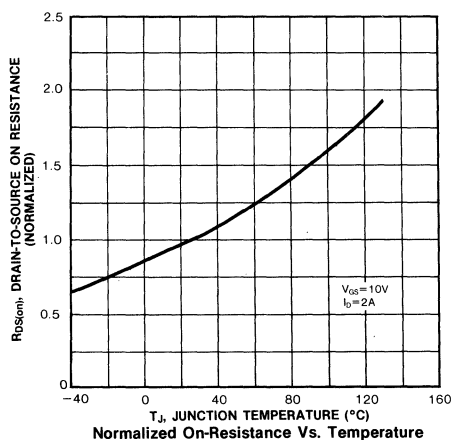
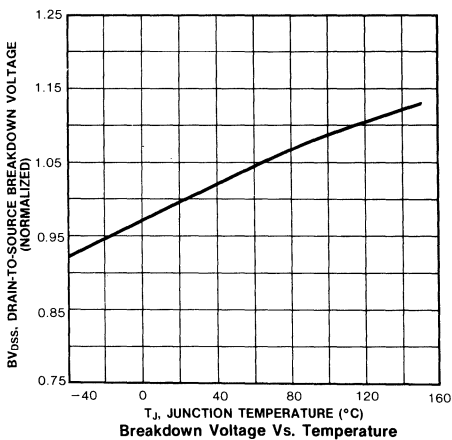
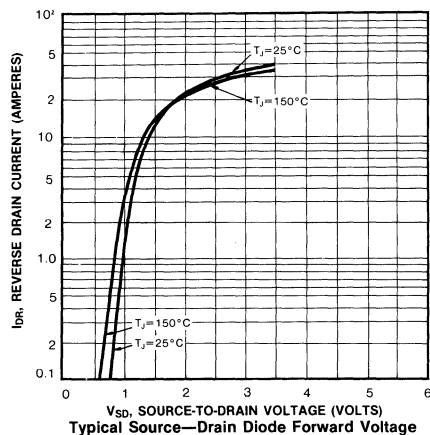
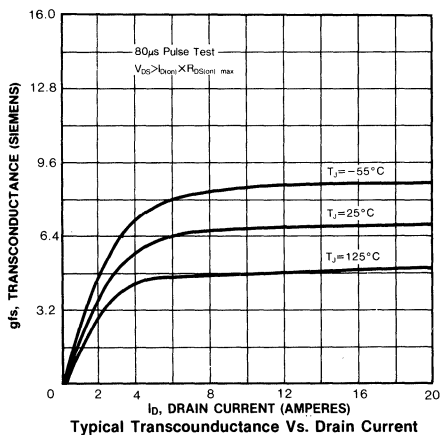
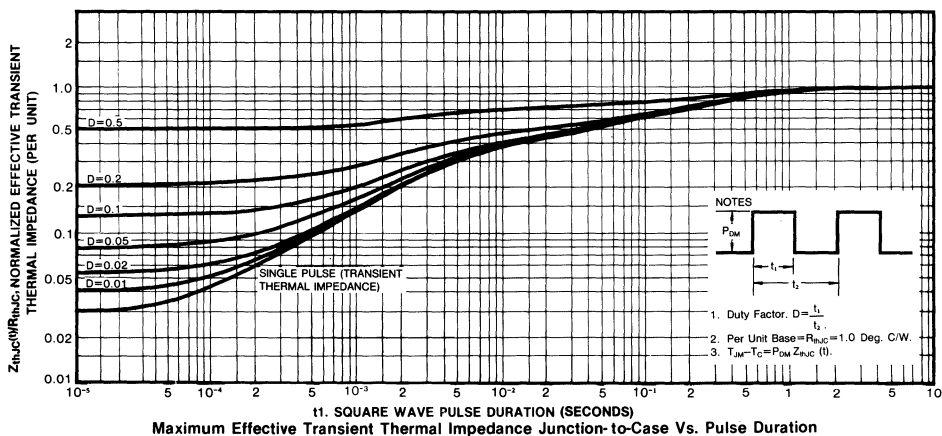
Symbol	Characteristic		SSP4N70	SSH4N70	Unit	
R_{thJC}	Junction-to-Case	MAX	1.0	1.0	K/W	
R_{thCS}	Case-to-Sink	HEW	0.5	0.24	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	MAX	80	40	K/W	Free Air Operation

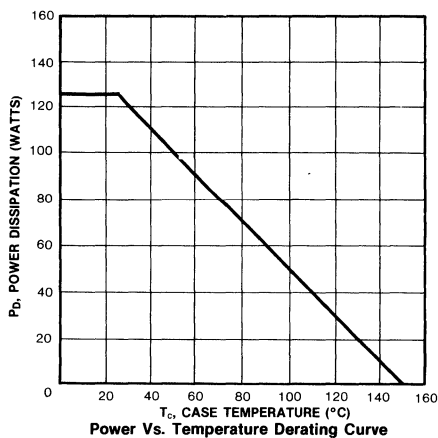
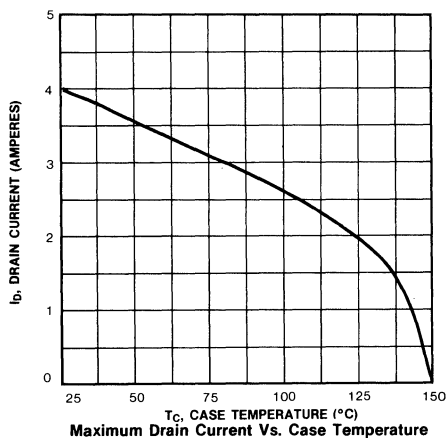
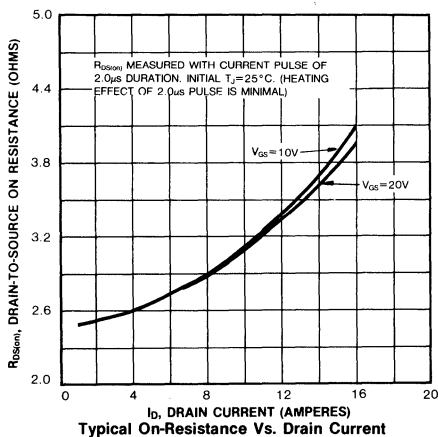
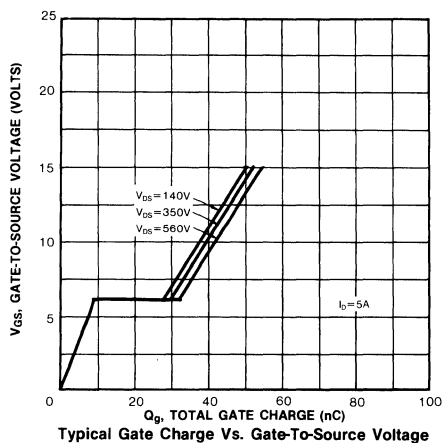
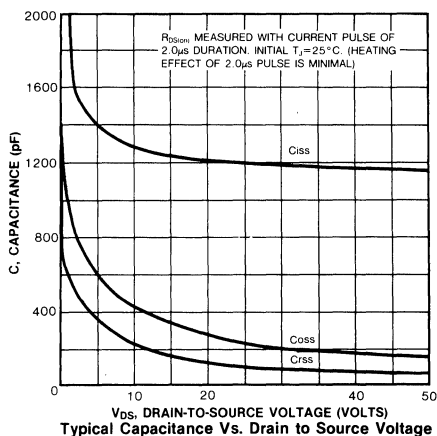
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	4.0	A	Modified MOSFET showing the integral reverse P-N junction rectifier 
I_{SM}	Pulse Source Current(Body Diode)(3)	—	—	16	A	
V_{SD}	Diode Forward Voltage(2)	—	—	1.5	V	$T_C=25^{\circ}\text{C}$, $I_S=4.0\text{A}$, $V_{GS}=0\text{V}$
t_{rr}	Reverse Recovery Time	—	600	—	ns	$T_J=150^{\circ}\text{C}$, $I_F=4.0\text{A}$, $dI_F/dt=100\text{A}/\mu\text{S}$

Notes: (1) $T_J=25^{\circ}\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature





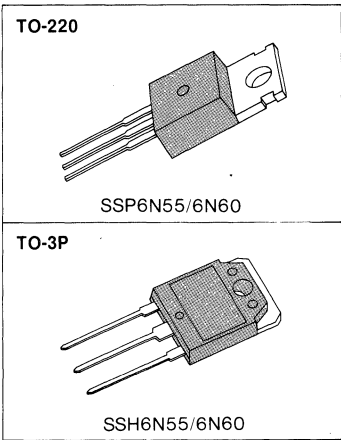


FEATURES

- Lower $R_{DS(ON)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$		I_D
		A	STD	
SSP6N55/SSH6N55	550V	1.2 Ω	1.8 Ω	6A
SSP6N60/SSH6N60	600V	1.2 Ω	1.8 Ω	6A



MAXIMUM RATINGS

Characteristic	Symbol	SSP6N55 SSH6N55	SSP6N60 SSH6N60	Unit
Drain-Source Voltage (1)	V_{DSS}	550	600	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$)(1)	V_{DGR}	550	600	Vdc
Gate-Source Voltage	V_{GS}	± 20		Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	6.0	6.0	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	4.0	4.0	Adc
Drain Current—Pulsed (3)	I_{DM}	24	24	Adc
Gate Current—Pulsed	I_{GM}	± 1.5		Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	570		mJ
Avalanche Current	I_{AS}	6.0		A
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	125 1.0		Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300		$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature
(4) $L=27mH$, $V_{dd}=50V$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-Source Breakdown Voltage SSP6N55/SSH6N55/	550	—	—	V	V _{GS} =0V I _D =250μA
	SSP6N60/SSH6N60/	600	—	—	V	
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.5	V	V _{DS} =V _{GS} , I _D =1mA
I _{GSS}	Gate-Source Leakage Forward	—	—	100	nA	V _{GS} =20V
I _{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	V _{GS} =-20V
I _{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	V _{DS} =Max. Rating, V _{GS} =0V
		—	—	1000	μA	V _{DS} =Max. Rating×0.8, V _{GS} =0V, T _C =125°C
I _{D(on)}	On-State Drain-Source Current (2)	6.0	—	—	A	V _{DS} ≥10V, V _{GS} =10V
R _{DS(on)}	Static Drain-Source On-State A Resistance (2) STD	—	—	1.2	Ω	V _{GS} =10V, I _D =3.0A
		—	—	1.8	Ω	
g _{fs}	Forward Transconductance (2)	3.0	4.8	—	Ω	V _{DS} ≥50V, I _D =3.0A
C _{iss}	Input Capacitance	—	—	1800	pF	V _{GS} =0V, V _{DS} =25V, f=1.0MHz
C _{oss}	Output Capacitance	—	—	350	pF	
C _{rss}	Reverse Transfer Capacitance	—	—	150	pF	
t _{d(on)}	Turn-On Delay Time	—	—	60	ns	V _{DD} =0.5BV _{DSS} , I _D =3.0A, Z _O =4.7Ω (MOSFET switching times are essentially independent of operating temperature)
t _r	Rise Time	—	—	150	ns	
t _{d(off)}	Turn-Off Delay Time	—	—	200	ns	
t _f	Fall Time	—	—	120	ns	
Q _g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	—	40	nC	V _{GS} =10V, I _D =7.5A, V _{DS} =0.8 Max. Rating (Gate charge is essentially independent of operating temperature.)
Q _{gs}	Gate-Source Charge	—	—	15	nC	
Q _{gd}	Gate-Drain ("Miller") Charge	—	—	25	nC	

THERMAL RESISTANCE

Symbol	Characteristic		SSP6N55/60	SSH6N55/60	Unit	
R _{thJC}	Junction-to-Case	MAX	1.0	1.0	K/W	
R _{thCS}	Case-to-Sink	TYP	0.5	0.24	K/W	Mounting surface flat, smooth, and greased
R _{thJA}	Junction-to-Ambient	MAX	80	40	K/W	Free Air Operation

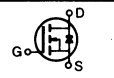
Notes: (1) T_J=25°C to 150°C

(2) Pulse test: Pulse width≤300μs, Duty Cycle≤2%

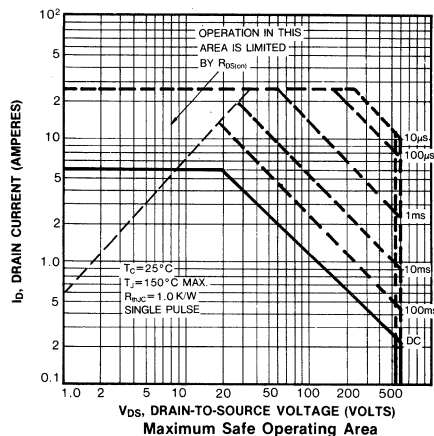
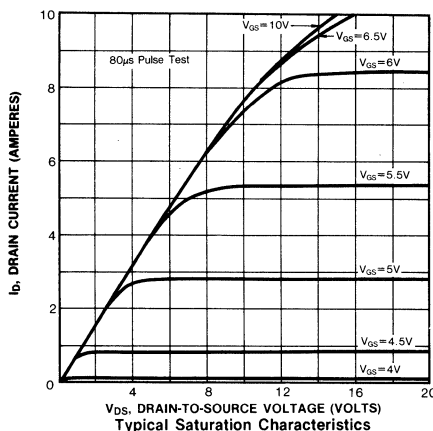
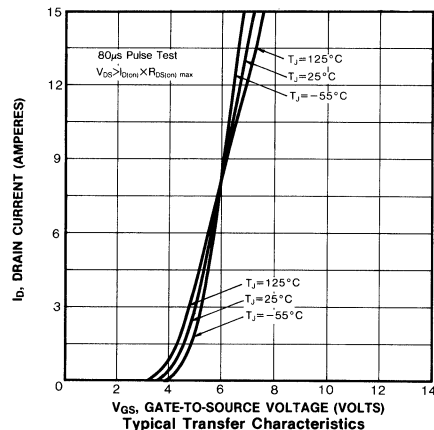
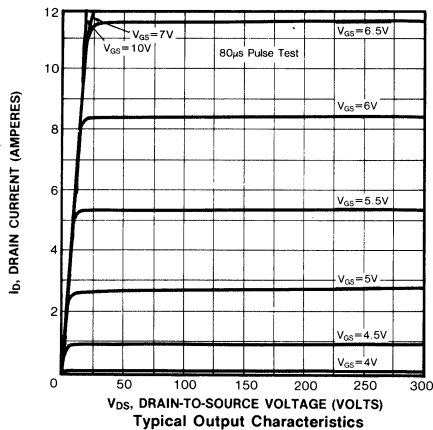
(3) Repetitive rating: Pulse width limited by max. junction temperature

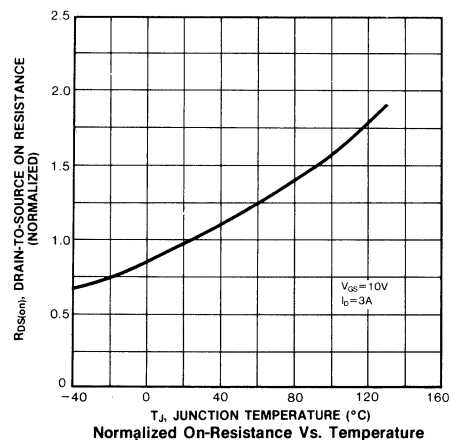
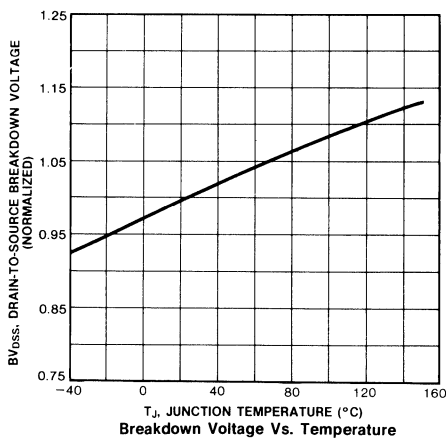
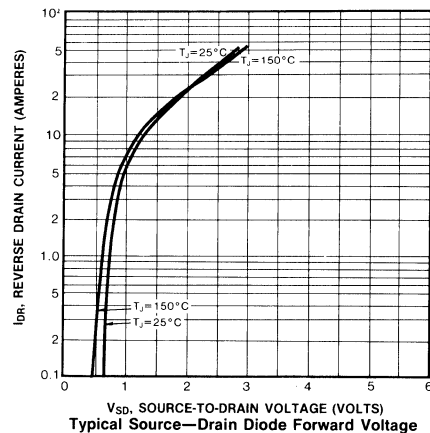
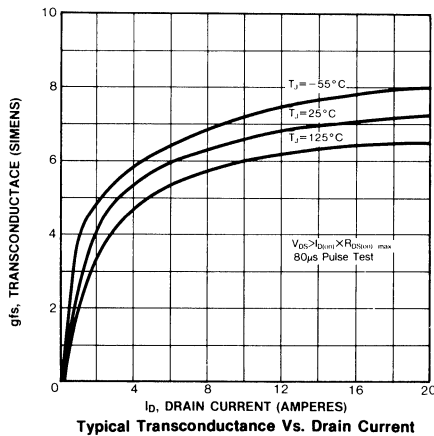
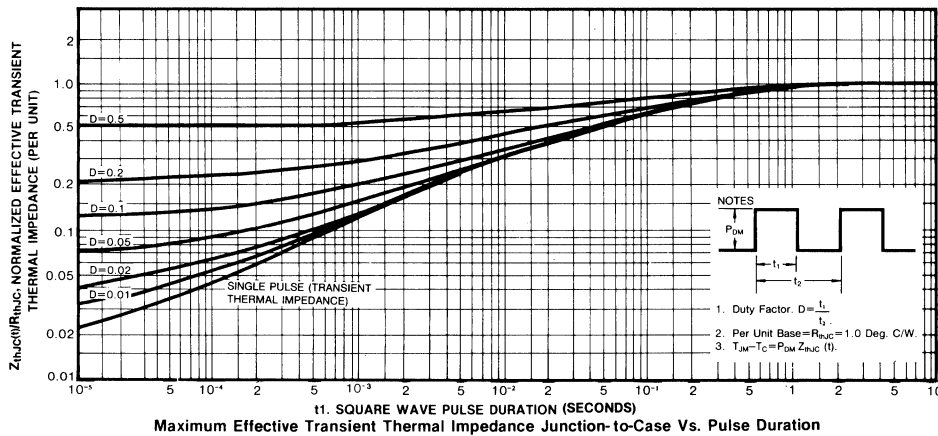
(4) For Ultra low "A" R_{DS(on)}, device add "A" suffix to part number

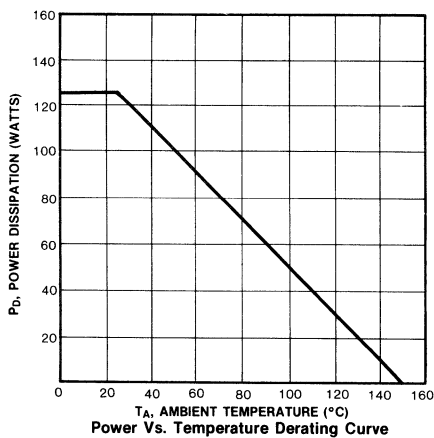
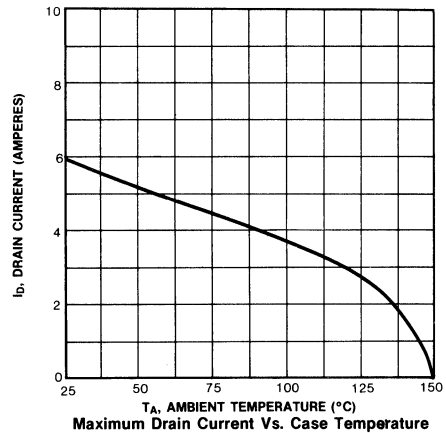
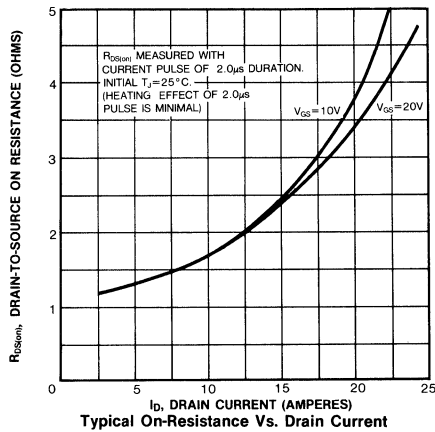
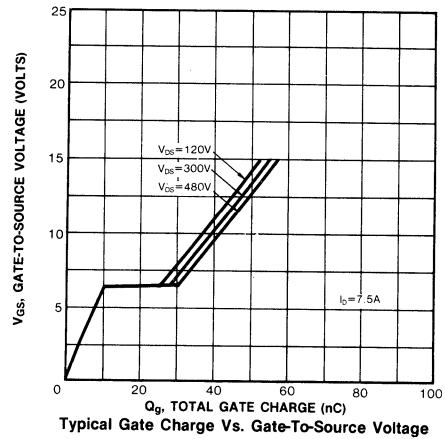
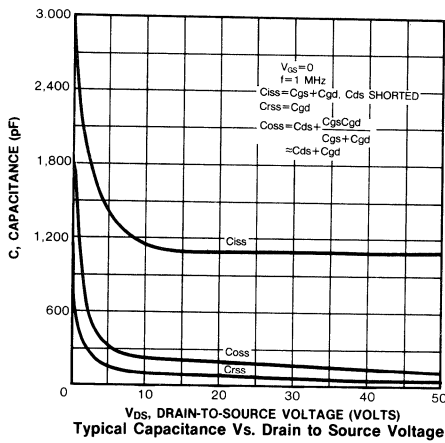
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	6.0	A	Modified MOSFET showing the integral reverse P-N junction rectifier 
I_{SM}	Pulse Source Current(Body Diode)(3)	—	—	24.0	A	
V_{SD}	Diode Forward Voltage (2)	—	—	1.5	V	$T_C=25^\circ\text{C}$, $I_S=10.0\text{A}$, $V_{GS}=0\text{V}$
t_{rr}	Reverse Recovery Time	—	450	940	ns	$T_J=150^\circ\text{C}$, $I_F=10.0\text{A}$, $dI_F/dt=100\text{A}/\mu\text{S}$

Notes: (1) $T_J=25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature







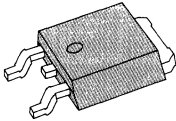
FEATURES

- Lower Rps (ON)
- Excellent voltage stability
- Fast switching time
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability

PRODUCT SUMMARY

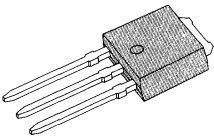
Part Number	V _{DS}	R _{DS(on)}	I _D
SSR1N60/U1N60	600V	12Ω	1.0A
SSR1N55/U1N55	550V	12Ω	1.0A

D-PACK



SSR1N60/1N55

I-PACK



SSU1N60/1N55

ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	SSR1N60/U1N60	SSR1N55/U1N55	Units
Drain-Source Voltage (1)	V _{DSS}	600	550	Vdc
Drain-Gate Voltage (R _{GS} =1.0MΩ) (1)	V _{DGR}	600	550	Vdc
Gate-Source Voltage	V _{GS}	± 20		Vdc
Continuous Drain Current T _C =25°C	I _D	1.0		Adc
Drain Current—Pulsed (3)	I _{DM}	3.0		Adc
Total Power Dissipation at T _C =25°C Derate above 25°C	P _D	40 0.32		Watts W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	- 55 to 150		°C
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T _L	300		°C

Notes: (1) T_J = 25°C to 150°C
(2) Pulse test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
(3) Repetitive rating: Pulse width limited by max. junction temperature

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage SSR1N60/U1N60	600	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
	SSR1N55/U1N55	550	—	—	V	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS} = 20V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	- 100	nA	$V_{GS} = -20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS} = \text{Max. Rating}, V_{GS} = 0V$
		—	—	1000		$V_{DS} = 0.8 \text{ Max. Rating}, T_C = 125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2)	1			A	$V_{DS} \geq 12V, V_{GS} = 10V$
$R_{DS(on)}$	Static Drain-Source On-State Resistance (2)	—	—	12	Ω	$V_{GS} = 10V, I_D = 0.5A$
g_{fs}	Forward Transconductance (2)	0.5	—	—	S	$V_{DS} \geq 15V, I_D = 0.5A$
C_{iss}	Input Capacitance	—	250	300	pF	$V_{GS} = 0V, V_{DS} = 25V, f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	25	50	pF	
C_{rss}	Reverse Transfer Capacitance	—	10	20	pF	
$t_{d(on)}$	Turn-On Delay Time	—	12	20	ns	$V_{DD} = 0.5BV_{DSS}, I_D = 0.5A, Z_O = 50\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	4	15	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	30	60	ns	
t_f	Fall Time	—	10	30	ns	
Q_g	Total Gate Charge (Gate-Source Pulse Gate-Drain)	—	20	—	nC	$V_{GS} = 10V, I_D = 1A, V_{DS} = 0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature)
Q_{gs}	Gate-Source Charge	—	3	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	9	—	nC	

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	MAX	3.125	K/W	
R_{thJA}	Junction-to-Ambient	MAX	110	K/W	Free Air Operation

Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse width limited by max. junction temperature

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
I_S	Continuous Source Current (Body Diode) SSR1N60/U1N60 SSR1N55/U1N55	—	—	1.0	A	Modified MOSFET integral reverse P-N junction rectifier 
I_{SM}	Pulse-Source Current (3) SSR1N60/U1N60 SSR1N55/U1N55	—	—	3.0	A	
V_{SD}	Diode Forward Voltage (2)	—	1	1.2	V	$T_C = 25^{\circ}\text{C}$, $I_S = 1\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	350	—	ns	$T_J = 25^{\circ}\text{C}$, $I_F = 1\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$

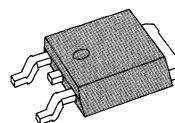
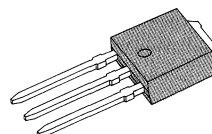
Notes: (1) $T_J = 25^{\circ}\text{C}$ to 150°C
(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse width limited by max. junction temperature

FEATURES

- Lower $R_{DS(on)}$
- Excellent voltage stability
- Fast switching speeds
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability
- D-PAK/I-PAK package

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	$I_{D(on)}$
SSR2955/U2955	-60V	0.30 Ω	-12A

D-PAK**SSR2955****I-PAK****SSU2955****MAXIMUM RATINGS**

Characteristic	Symbol	SSR2955/U2955	Units
Drain-Source Voltage (1)	V_{DSS}	- 60	Vdc
Drain-Gate Voltage ($R_{GS} = 1.0M\Omega$) (1)	V_{DGR}	- 60	Vdc
Gate-Source Voltage	V_{GS}	± 20	Vdc
Continuous Drain Current $T_C = 100^\circ\text{C}$	I_D	- 12	Adc
Continuous Drain Current $T_C = 25^\circ\text{C}$	I_D	- 8.4	Adc
Drain Current—Pulsed (3)	I_{DM}	- 36	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	42	Watts
Derate above 25°C		0.33	W/ $^\circ\text{C}$
Operation and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300	$^\circ\text{C}$

Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C

(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse width limited by max. junction temperature

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
BV_{DSS}	Drain Source Breakdown Voltage	-60	—	—	V	$V_{GS} = 0V$ $I_D = -250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	$V_{DS} = V_{GS}$, $I_D = -1.0mA$
I_{GSS}	Gate-Source Leakage Forward	—	—	-100	nA	$V_{GS} = -20V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	100	nA	$V_{GS} = 20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	-250	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0V$
		—	—	-1.0	mA	$V_{DS} = \text{Max. Rating} \times 0.8$, $V_{GS} = 0V$, $T_C = 125^\circ\text{C}$
$I_{D(on)}$	On-Static Drain-Source Current (2)	-12	—	—	A	$V_{DS} \geq I_{D(on)} \times R_{DS(on)}$ max. $V_{GS} = -10V$
$R_{DS(on)}$	Static Drain-Source On-State Resistance (2)	—	0.25	0.30	Ω	$V_{GS} = -10V$, $I_D = -6.0A$
g_{fs}	Forward Transconductance (2)	3.0	—	—	Ω	$V_{DS} \geq -15V$, $I_D = -6.0A$
C_{iss}	Input Capacitance	—	600	—	pF	$V_{GS} = 0V$, $V_{DS} = -25V$, $f = 1.0MHz$
C_{oss}	Output Capacitance	—	300	—	pF	
C_{rss}	Reverse Transfer Capacitance	—	135	—	pF	
$t_{d(on)}$	Turn On Delay Time	—	15	—	ns	$V_{DD} = -0.5BV_{DSS}$, $I_D = -6.0A$, $Z_O = 50 \text{ Ohms}$, (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	40	—	ns	
$t_{d(off)}$	Turn Off Delay Time	—	30	—	ns	
t_f	Fall Time	—	30	—	ns	
Q_g	Total Gate Charge	—	—	45	nC	$V_{GS} = -10V$, $I_D = -12A$, $V_{DS} = 0.8 \text{ max. Rating}$ (Gate charge is essentially independent of operating temperature)
Q_{gs}	Gate Source Charge	—	7	—	nC	
Q_{gd}	Gate Drain Charge	—	15	—	nC	

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	—	—	3.0	K/W	
R_{thCS}	Case-to-Sink	—	1.7	—	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	—	—	110	K/W	Free Air Operation

Note: (1) $T_J = 25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse width limited by max. junction temperature

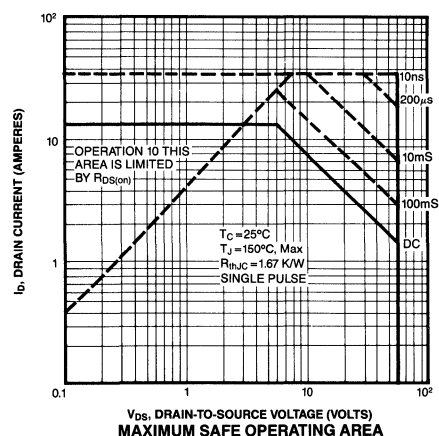
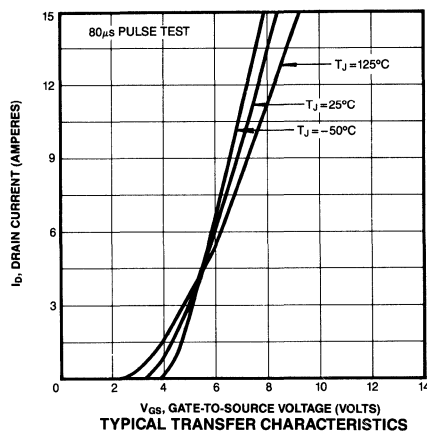
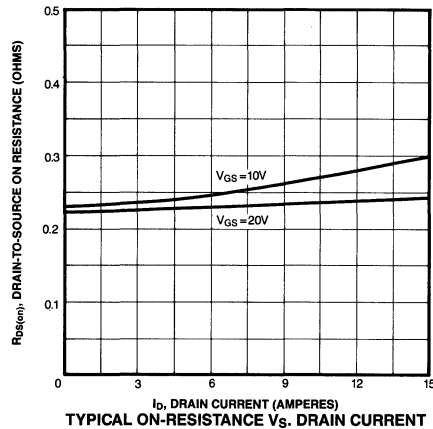
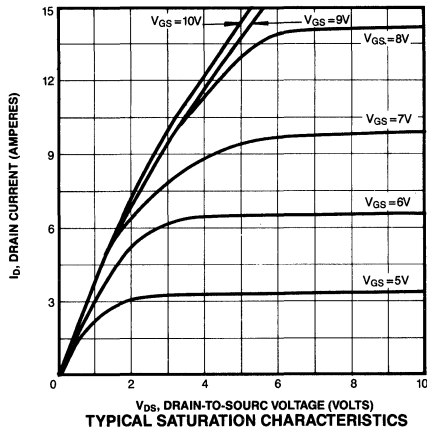
SOURCE DRAIN DIODE RATING AND CHARACTERISTICS

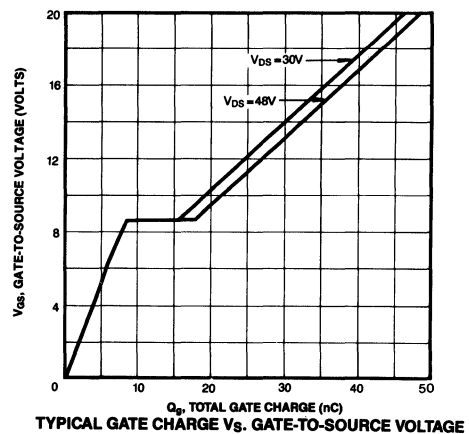
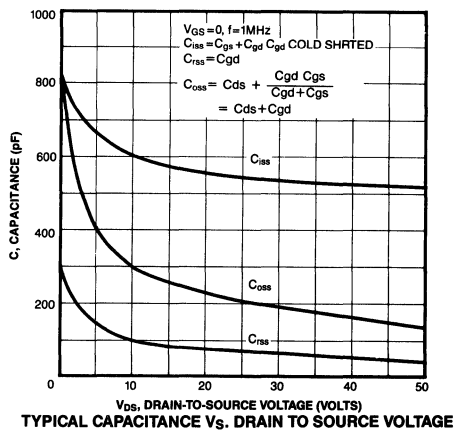
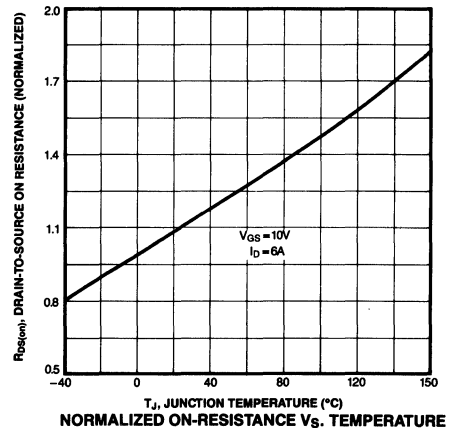
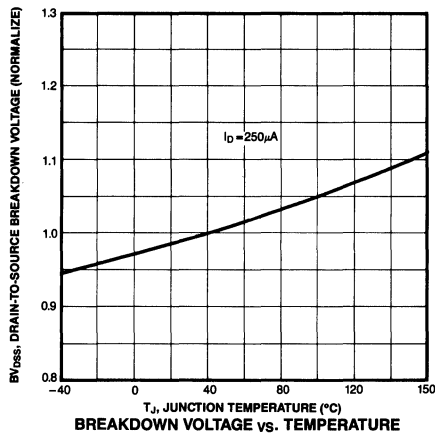
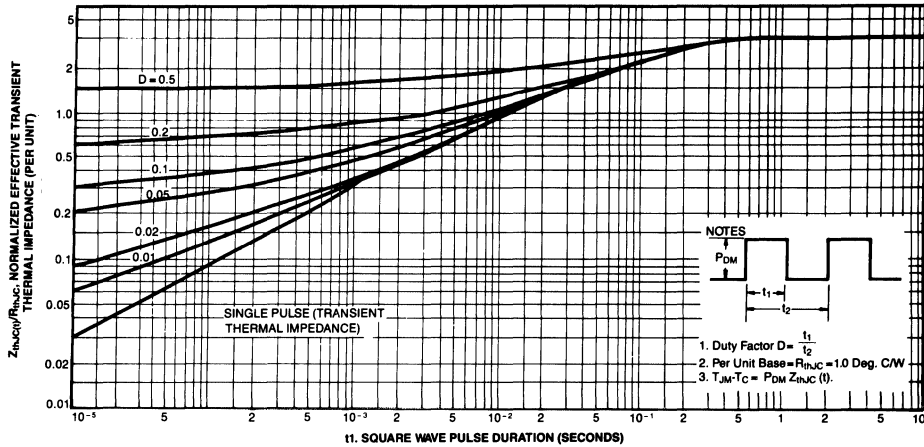
Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
I_S	Continuous Source Current (Body Diode)	—	—	- 12	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier
I_{SM}	Pulse Source Current (Body Diode) (3)	—	—	- 36	A	
V_{SD}	Diode Forward Voltage (2)	—	—	- 3.8	V	$T_C = 25^\circ\text{C}$, $I_S = -12\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	110	—	ns	$T_J = 25^\circ\text{C}$, $I_F = -12\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$

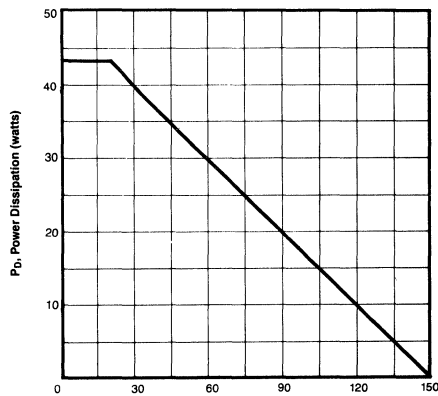
Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C

(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse width limited by max. junction temperature







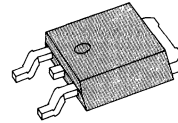
T_c , CASE TEMPERATURE (°C)
POWER VS. TEMPERATURE DERATING CURVE.

FEATURES

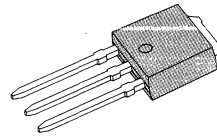
- Lower $R_{DS(on)}$
- Excellent voltage stability
- Fast switching speeds
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability
- D-PAK/I-PAK package

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	$I_D(on)$
SSR3055/SSU3055	60V	0.15 Ω	12A

D-PAK

SSR3055

I-PAK

SSU3055

MAXIMUM RATINGS

Characteristic	Symbol	SSR3055/U3055	Units
Drain-Source Voltage (1)	V_{DSS}	60	Vdc
Drain-Gate Voltage ($R_{GS} = 1.0M\Omega$) (1)	V_{DGR}	60	Vdc
Gate Source Voltage	V_{GS}	± 20	Vdc
Continuous Drain Current $T_C = 25^\circ C$	I_D	12	Adc
Continuous Drain Current $T_C = 100^\circ C$	I_D	8.4	Adc
Drain Current — Pulsed (3)	I_{DM}	26	Adc
Total Power Dissipation @ $T_C = 25^\circ C$ Derate above $25^\circ C$	P_D	42 0.33	Watts W/ $^\circ C$
Operation and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300	$^\circ C$

Notes: (1) $T_J = 25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse width limited by max. junction temperature

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
BV_{DSS}	Drain Source Breakdown Voltage	60	—	—	V	$V_{GS} = 0V$ $I_D = 250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu A$
I_{GSS}	Gate Source Leakage Forward	—	—	100	nA	$V_{GS} = 20V$
I_{GSS}	Gate Source Leakage Reverse	—	—	-100	nA	$V_{GS} = -20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0V$
		—	—	1.0	mA	$V_{DS} = \text{Max. Rating} \times 0.8$, $V_{GS} = 0V$, $T_C = 125^\circ\text{C}$
$I_{D(on)}$	On Static Drain Source Current (2)	12	—	—	A	$V_{DS} \geq R_{DS(on)}$ max. $V_{GS} = 10V$
$R_{DS(on)}$	Static Drain Source On State Resistance (2)	—	0.11	0.15	Ω	$V_{GS} = 10V$, $I_D = 6.0A$
g_{fs}	Forward Transconductance (2)	4.0	—	—	S	$V_{DS} \geq 15V$, $I_D = 6.0A$
C_{iss}	Input Capacitance	—	440	—	pF	$V_{GS} = 0V$, $V_{DS} = 25V$, $f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	170	—	pF	
C_{rss}	Reverse Transfer Capacitance	—	45	—	pF	
$t_{d(on)}$	Turn On Delay Time	—	—	20	ns	$V_{DD} = 0.5 BV_{DSS}$, $I_D = 6A$, $Z_\theta = 50 \text{ Ohms}$, (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	—	—	60	ns	
$t_{d(off)}$	Turn Off Delay Time	—	—	65	ns	
t_f	Fall Time	—	—	65	ns	
Q_g	Total Gate Charge	—	—	17	nC	$V_{GS} = 10V$, $I_D = 12A$, $V_{DS} = 0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature)
Q_{gs}	Gate Source Charge	—	6.5	—	nC	
Q_{gd}	Gate Drain Charge	—	5.5	—	nC	

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	—	—	3.0	K/W	
R_{thCS}	Case-to-Sink	—	1.7	—	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	—	—	110	K/W	Free Air Operation

Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

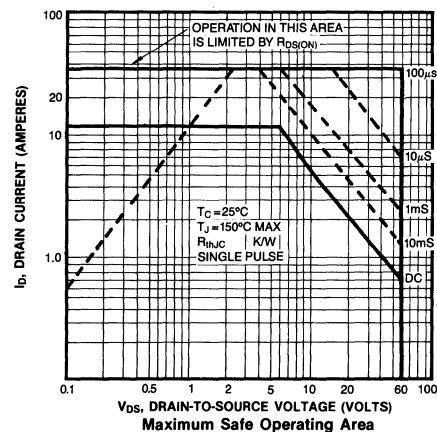
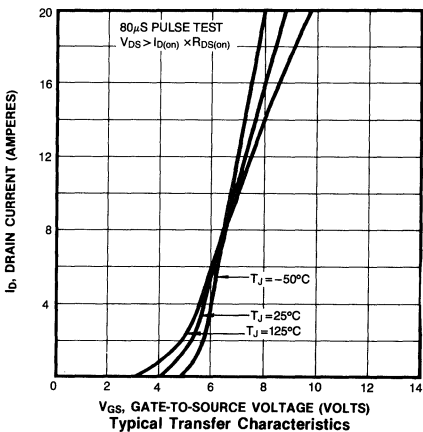
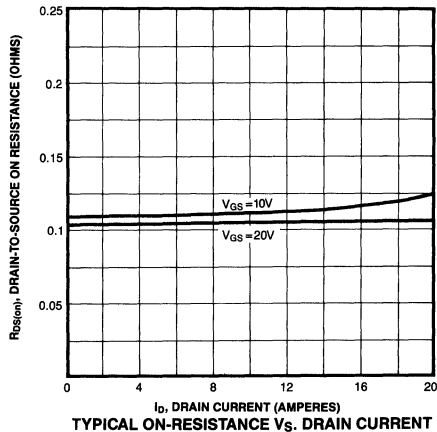
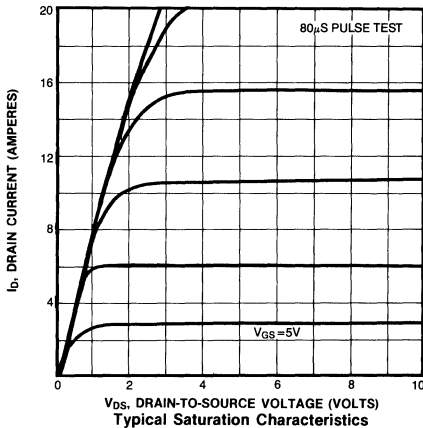
(3) Repetitive rating: Pulse width limited by max. junction temperature

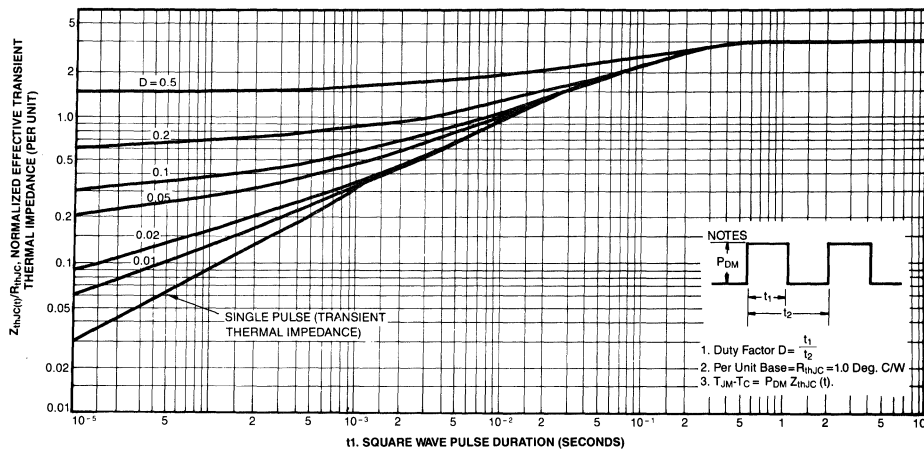
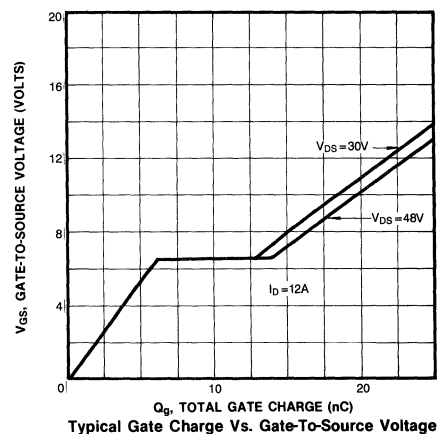
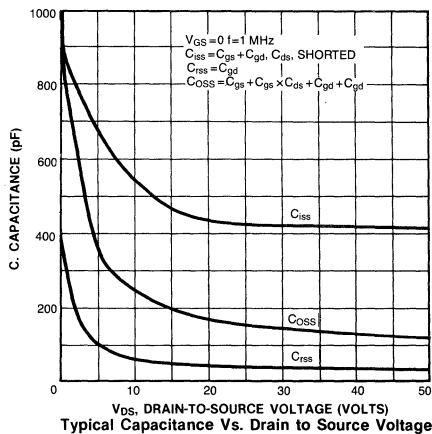
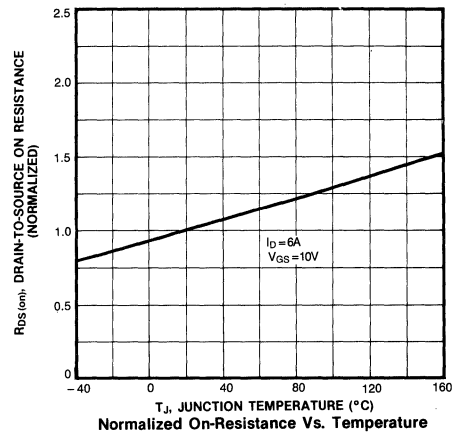
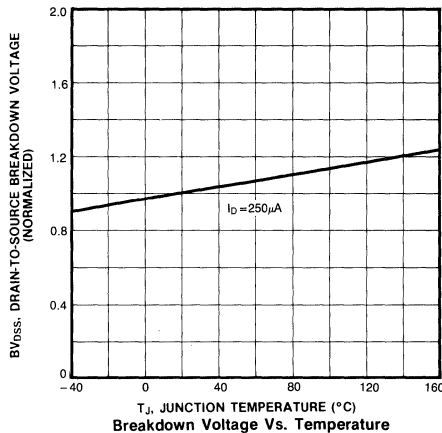
SOURCE DRAIN DIODE RATING AND CHARACTERISTICS

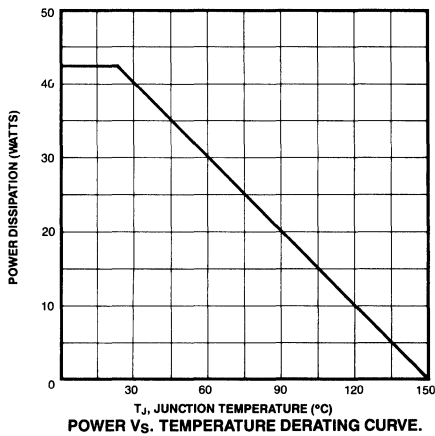
Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	12	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier
I_{SM}	Pulse Source Current (Body Diode) (3)	—	—	26	A	
V_{SD}	Diode Forward Voltage (2)	—	1.7	3.8	V	$T_C = 25^\circ\text{C}$, $I_S = 12\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	110	—	ns	$T_J = 25^\circ\text{C}$, $I_F = 12\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$

Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C
(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse width limited by max. junction temperature

2



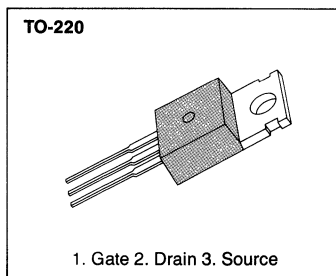
MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE JUNCTION-TO-CASE V_S PULSE DURATION



2

FEATURES

- Lower $R_{DS(on)}$
- Excellent voltage stability
- Fast switching speeds
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability
- TO-220 Package



PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	$I_{D(on)}$
IRL510	100V	0.75 Ω	4.0A
IRL511	80V	0.75 Ω	4.0A

MAXIMUM RATINGS

Characteristic	Symbol	IRL510	IRL511	Units
Drain-Source Voltage (1)	V_{DSS}	100	80	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$) (1)	V_{DGR}	100	80	Vdc
Gate-Source Voltage	V_{GS}	± 15		Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	4.0	4.0	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	2.8	2.8	Adc
Drain Current—Pulsed (3)	I_{DM}	16	16	Adc
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	25 0.2		Watts W/ $^\circ C$
Operation and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300		$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$
 (2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
 (3) Repetitive rating: Pulse width limited by max. junction temperature

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

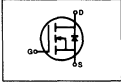
Symbol	Characteristic		Min	Typ	Max	Units	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage	IRL510 IRL511	100 80	— —	— —	V	$V_{GS} = 0V$ $I_D = 250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage		1.0	—	2.0	V	$V_{DS} = V_{GS}$, $I_D = 1mA$
I_{GSS}	Gate-Source Leakage Forward		—	—	100	nA	$V_{GS} = 15V$
I_{GSS}	Gate-Source Leakage Reverse		—	—	-100	nA	$V_{GS} = -15V$
I_{DSS}	Zero Gate Voltage Drain Current		—	—	250	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0V$
			—	—	1.0	mA	$V_{DS} = \text{Max. Rating} \times 0.8$, $V_{GS} = 0V$, $T_C = 125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2)		4.0	—	—	A	$V_{DS} \geq I_{D(on)} \times R_{DS(on)max}$, $V_{GS} = 5.0V$
$R_{DS(on)}$	Static Drain Source On State Resistance (2)		—	—	0.75	Ω	$V_{GS} = 5.0V$, $I_D = 2.0A$
g_{fs}	Forward Transconductance (2)		1.3	—	—	S	$V_{DS} \geq 25V$, $I_D = 2.0A$
C_{iss}	Input Capacitance		—	240	—	pF	$V_{GS} = 0V$, $V_{DS} = 25V$, $f = 1.0MHz$
C_{oss}	Output Capacitance		—	70	—	pF	
C_{rss}	Reverse Transfer Capacitance		—	40	—	pF	
$t_{d(on)}$	Turn-On Delay Time		—	8.0	20	ns	$V_{DD} = 0.5BV_{DSS}$, $I_D = 4.0A$, $Z_O = 15\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time		—	8.0	25	ns	
$t_{d(off)}$	Turn-Off Delay Time		—	10	25	ns	
t_f	Fall Time		—	8.0	20	ns	$V_{GS} = 5V$, $I_D = 4.0A$, $V_{DS} = 0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature)
Q_g	Total Gate Charge		—	—	7.5	nC	
Q_{gs}	Gate-Source Charge		—	1.9	—	nC	
Q_{gd}	Gate-Drain Charge		—	3.8	—	nC	

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	—	—	5.0	K/W	
R_{thCS}	Case-to-Sink	—	0.5	—	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	—	—	80	K/W	Free Air Operation

Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse width limited by max. junction temperature

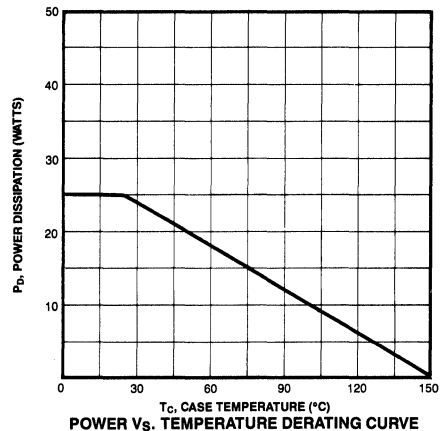
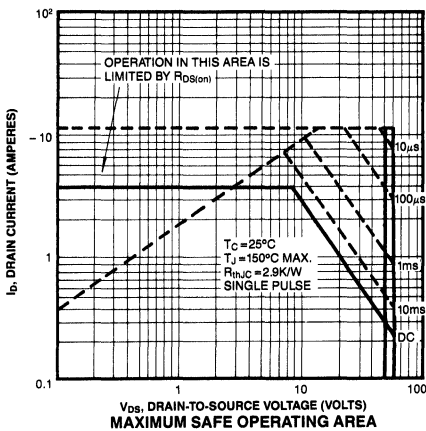
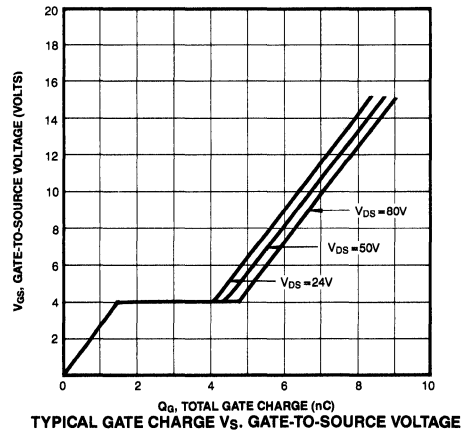
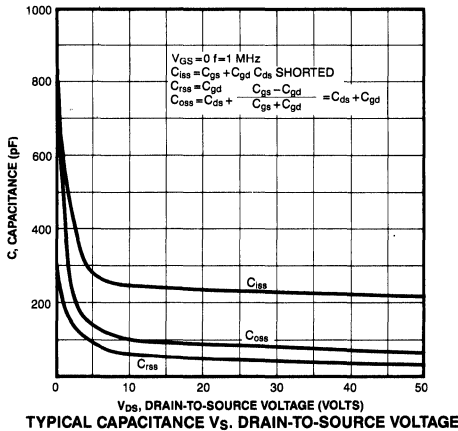
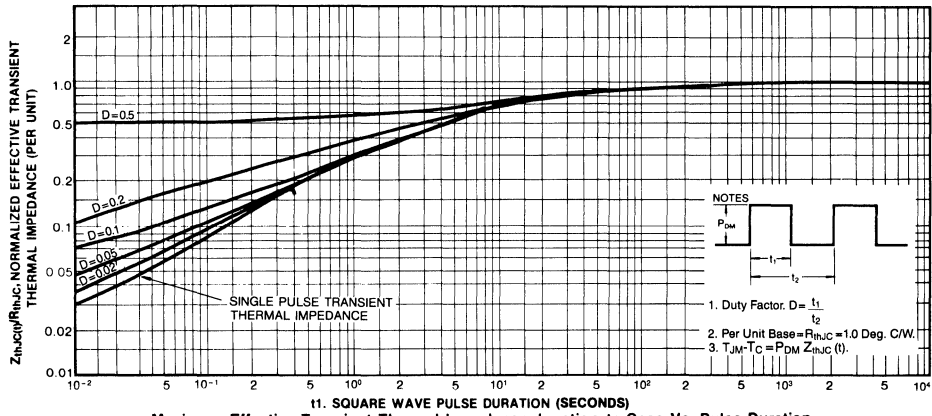
SOURCE-DRAIN DIODE RATING AND CHARACTERISTICS

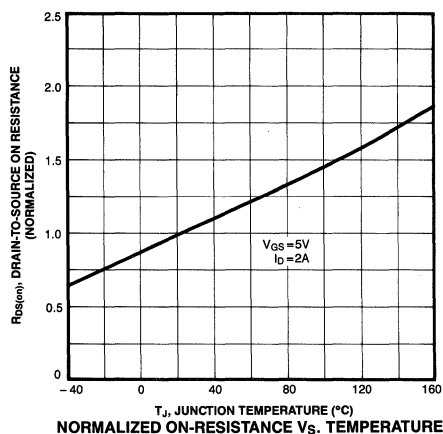
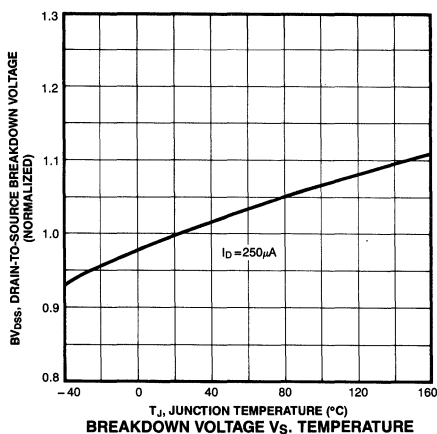
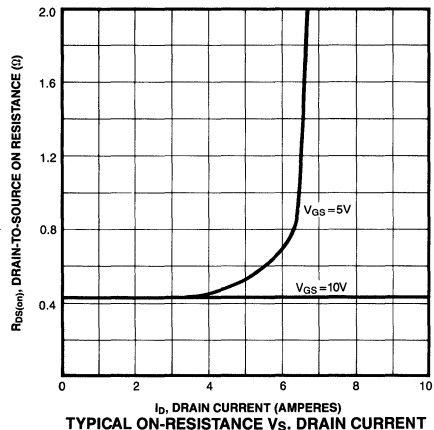
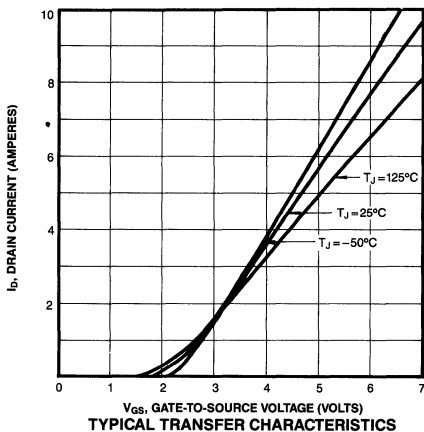
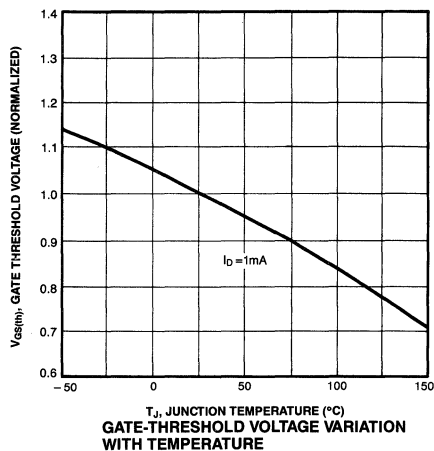
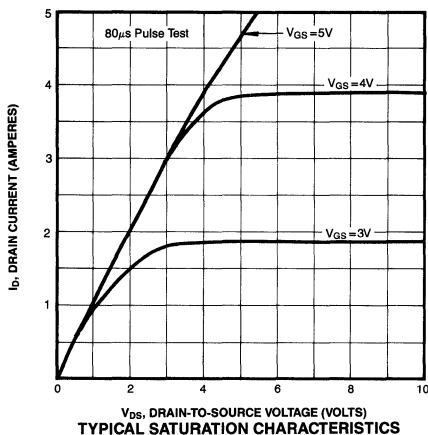
Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
I_S	Continuous Source Current (Body Diode)	—	—	4.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier 
I_{SM}	Pulse Source Current (Body Diode) (3)	—	—	16	A	
V_{SD}	Diode Forward Voltage (2)	—	—	2.5	V	$T_C = 25^\circ\text{C}$, $I_S = 4.0\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	230	—	ns	$T_J = 25^\circ\text{C}$, $I_F = 4.0\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$

Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C

(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$

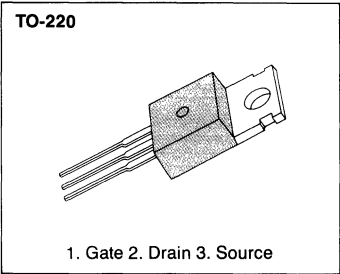
(3) Repetitive rating: Pulse width limited by max. junction temperature





FEATURES

- Lower $R_{DS(on)}$
- Excellent voltage stability
- Fast switching speeds
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability
- TO-220 Package



PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	$I_{D(on)}$
IRL520	100V	0.4Ω	7.9A
IRL521	80V	0.4Ω	7.9A

MAXIMUM RATINGS

Characteristic	Symbol	IRL520	IRL521	Units
Drain-Source Voltage (1)	V_{DS}	100	80	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$) (1)	V_{DGR}	100	80	Vdc
Gate-Source Voltage	V_{GS}	± 15		Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	7.9	7.9	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	5.5	5.5	Adc
Drain Current—Pulsed (3)	I_{DM}	32	32	Adc
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	42 0.33		Watts W/ $^\circ C$
Operation and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300		$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse width limited by max. junction temperature

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

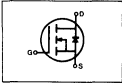
Symbol	Characteristic		Min	Typ	Max	Units	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage	IRL520 IRL521	100 80	— —	— —	V	$V_{GS} = 0V$ $I_D = 250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage		1.0	—	2.0	V	$V_{DS} = V_{GS}$, $I_D = 1mA$
I_{GSS}	Gate-Source Leakage Forward		—	—	100	nA	$V_{GS} = 15V$
I_{GSS}	Gate-Source Leakage Reverse		—	—	-100	nA	$V_{GS} = -15V$
I_{DSS}	Zero Gate Voltage Drain Current		—	—	250	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0V$
			—	—	1.0	mA	$V_{DS} = \text{Max. Rating} \times 0.8$, $V_{GS} = 0V$, $T_C = 125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2)		7.9	—	—	A	$V_{DS} \geq I_{D(on)} \times R_{DS(on)max}$, $V_{GS} = 5.0V$
$R_{DS(on)}$	Static Drain Source On State Resistance (2)		—	—	0.4	Ω	$V_{GS} = 5.0V$, $I_D = 4.0A$
g_{fs}	Forward Transconductance (2)		3.0	—	—	V	$V_{DS} \geq 25V$, $I_D = 4.0A$
C_{iss}	Input Capacitance		—	450	—	pF	$V_{GS} = 0V$, $V_{DS} = 25V$, $f = 1.0MHz$
C_{oss}	Output Capacitance		—	120	—	pF	
C_{rss}	Reverse Transfer Capacitance		—	60	—	pF	
$t_{d(on)}$	Turn-On Delay Time		—	—	15	nS	$V_{DD} = 0.5BV_{DSS}$, $I_D = 4.0A$, $Z_\theta = 50\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time		—	—	27	nS	
$t_{d(off)}$	Turn-Off Delay Time		—	—	45	nS	
t_f	Fall Time		—	—	30	nS	
Q_g	Total Gate Charge		—	9.8	15	nC	$V_{GS} = 5V$, $I_D = 8.0A$, $V_{DS} = 0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature)
Q_{gs}	Gate-Source Charge		—	3.5	—	nC	
Q_{gd}	Gate-Drain Charge		—	6.3	—	nC	

THERMAL RESISTANCE

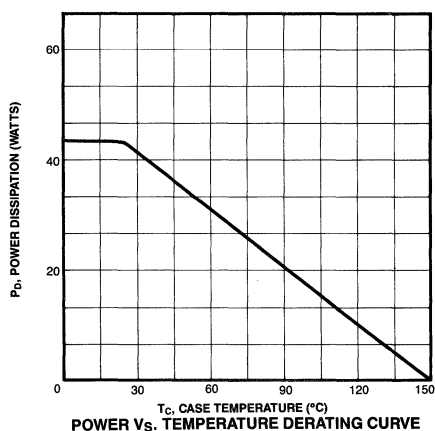
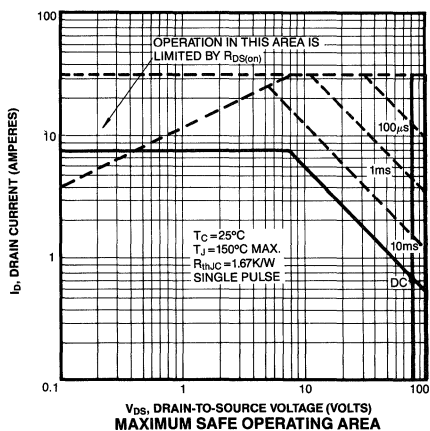
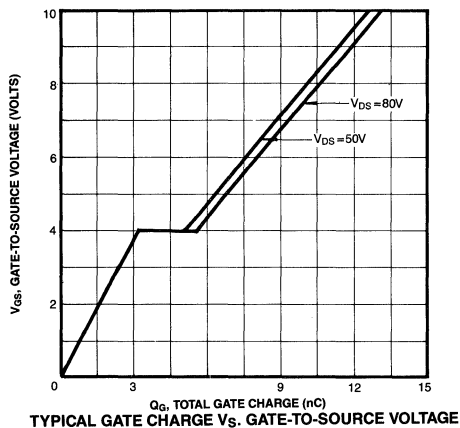
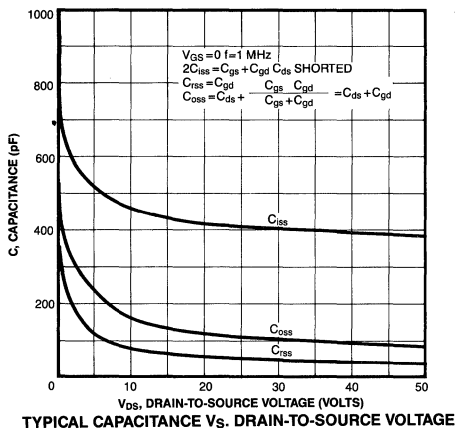
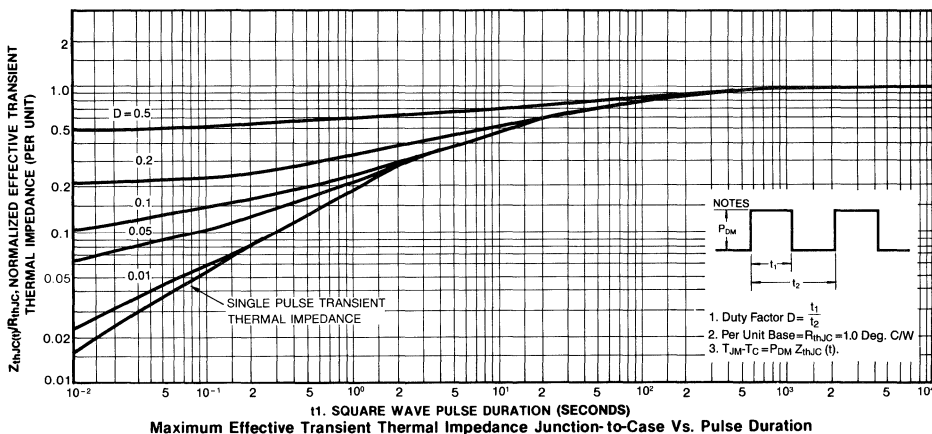
R_{thJC}	Junction-to-Case	—	—	3.0	K/W	
R_{thCS}	Case-to-Sink	—	0.5	—	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	—	—	80	K/W	Free Air Operation

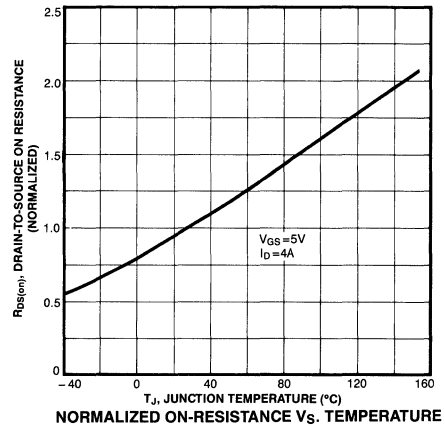
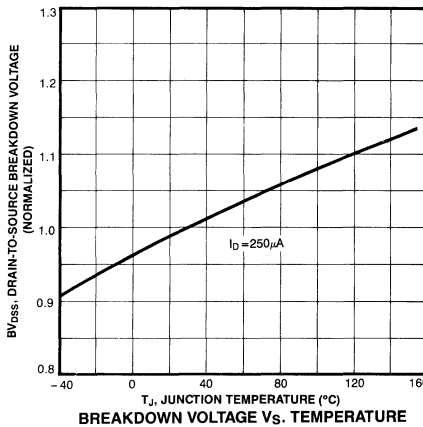
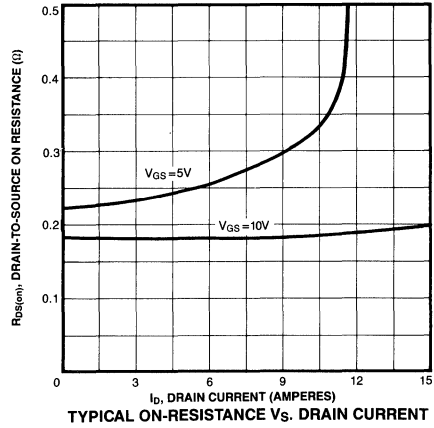
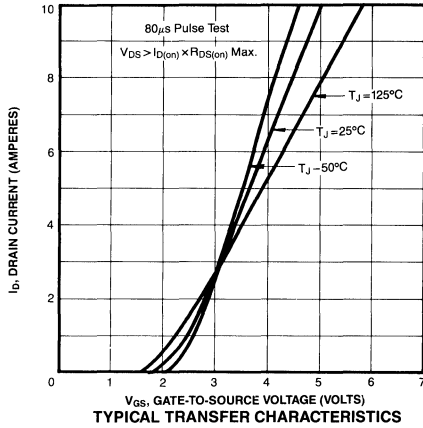
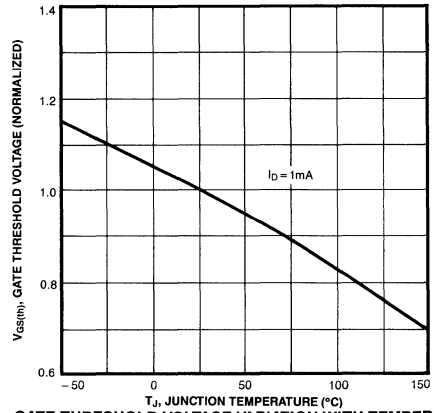
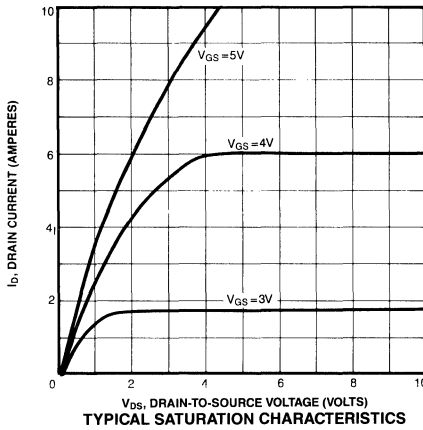
Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse width limited by max. junction temperature

SOURCE-DRAIN DIODE RATING AND CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
I_S	Continuous Source Current (Body Diode)	—	—	7.9	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier 
I_{SM}	Pulse Source Current (Body Diode) (3)	—	—	32	A	
V_{SD}	Diode Forward Voltage (2)	—	—	2.5	V	$T_C = 25^{\circ}\text{C}$, $I_S = 7.9\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	280	—	ns	$T_J = 25^{\circ}\text{C}$, $I_F = 7.9\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$

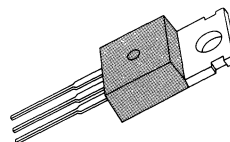
Notes: (1) $T_J = 25^{\circ}\text{C}$ to 150°C
(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse width limited by max. junction temperature





FEATURES

- Lower $R_{DS(on)}$
- Excellent voltage stability
- Fast switching speeds
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability
- TO-220 Package

TO-220

1. Gate 2. Drain 3. Source
PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	$I_{D(on)}$
IRL530	100V	0.2 Ω	13A
IRL531	80V	0.2 Ω	13A

MAXIMUM RATINGS

Characteristic	Symbol	IRL530	IRL531	Units
Drain-Source Voltage (1)	V_{DSS}	100	80	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$) (1)	V_{DGR}	100	80	Vdc
Gate-Source Voltage	V_{GS}	± 15		Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	13	13	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	9	9	Adc
Drain Current — Pulsed (3)	I_{DM}	52	52	Adc
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	75 0.6		Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	- 55 to 150		$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300		$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse width limited by max. junction temperature

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage IRL530 IRL531	100 80	— —	— —	V	$V_{GS} = 0V$ $I_D = 250\mu A$
$V_{(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	$V_{DS} = V_{GS}$, $I_D = 1mA$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS} = 15V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	$V_{GS} = -15V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0V$
		—	—	1.0	mA	$V_{DS} = \text{Max. Rating} \times 0.8$, $V_{GS} = 0V$, $T_C = 125^\circ\text{C}$
$I_{D(on)}$	On-State Drain Source Current (2)	13	—	—	A	$V_{DS} \geq I_{D(on)} \times R_{DS(on)max.}$, $V_{GS} = 5.0V$
$R_{DS(on)}$	Static Drain-Source On State Resistance (2)	—	—	0.2	Ω	$V_{GS} = 5.0V$, $I_D = 7.0A$
g_{fs}	Forward Transconductance (2)	7.0	—	—	$\bar{O}$	$V_{DS} \geq 25V$, $I_D = 7.0A$
C_{iss}	Input Capacitance	—	800	—	pF	$V_{GS} = 0V$, $V_{DS} = 25V$ $f = 1.0MHz$
C_{oss}	Output Capacitance	—	200	—	pF	
C_{rss}	Reverse Transfer Capacitance	—	90	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	—	30	ns	$V_{DD} = 0.5 BV_{DSS}$, $I_D = 7.0A$, $Z_O = 50 \Omega$ (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	—	—	75	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	—	40	ns	
t_f	Fall Time	—	—	45	ns	
Q_g	Total Gate Charge	—	18	30	nC	$V_{GS} = 5V$, $I_D = 13A$, $V_{DS} = 0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature)
Q_{gs}	Gate-Source Charge	—	6.0	—	nC	
Q_{gd}	Gate-Drain Charge	—	12.0	—	nC	

THERMAL RESISTANCE

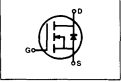
R_{thSC}	Junction-to-Case	—	—	1.7	K/W	
R_{thCS}	Case-to-Sink	—	0.5	—	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	—	—	80	K/W	Free Air Operation

Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C

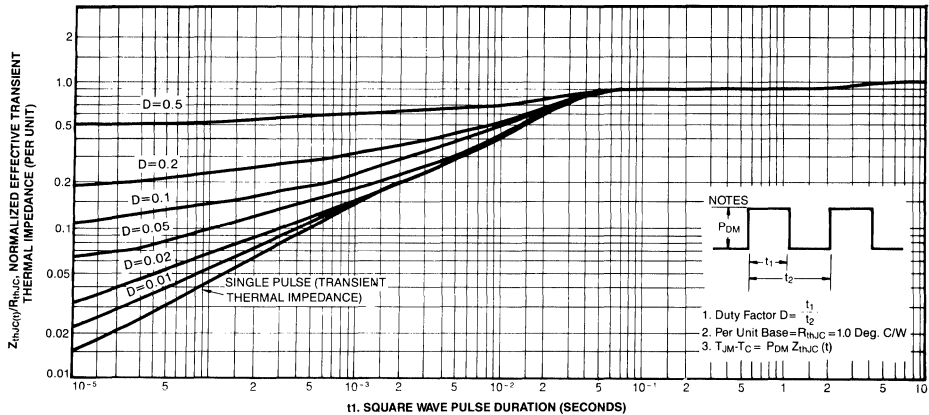
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse width limited by max. junction temperature

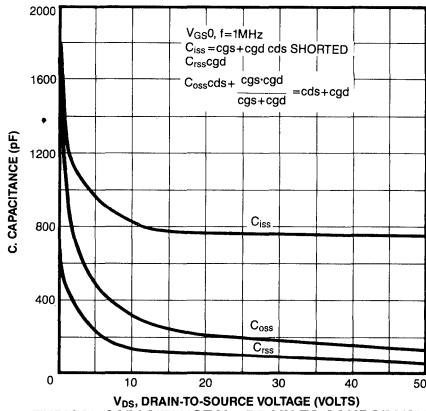
SOURCE-DRAIN DIODE RATING AND CHARACTERISTIC

Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
I_S	Continuous Source Current (Body Diode)	—	—	13	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier 
I_{SM}	Pulse Source Current (Body Diode) (3)	—	—	52	A	
V_{SD}	Diode Forward Voltage (2)	—	—	2.5	V	$T_C = 25^\circ\text{C}$, $I_S = 13\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	—	360	ns	$T_J = 25^\circ\text{C}$, $I_F = 13\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{s}$

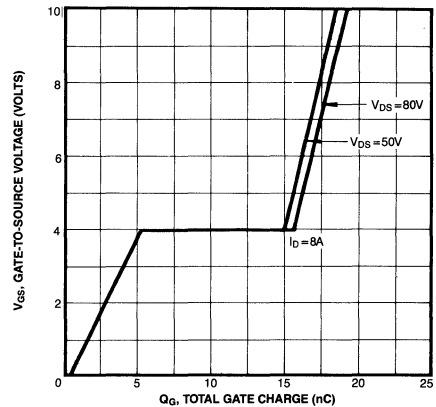
Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C
(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse width limited by max. junction temperature



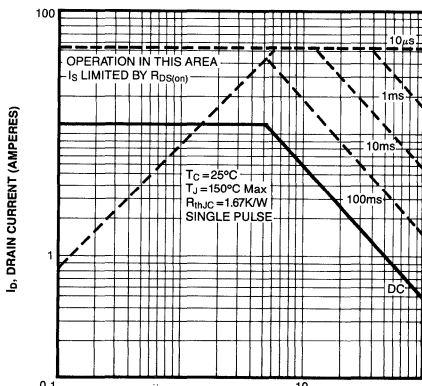
MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE JUNCTION-TO-CASE V_{GS} , PULSE DURATION



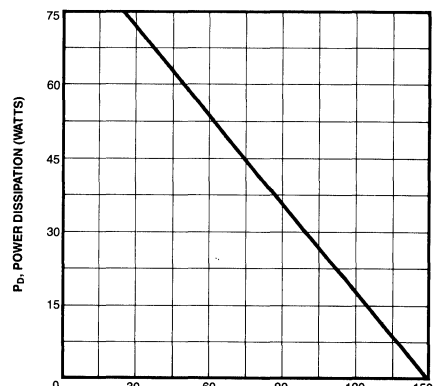
TYPICAL CAPACITANCE V_{GS} , DRAIN TO SOURCE VOLTAGE



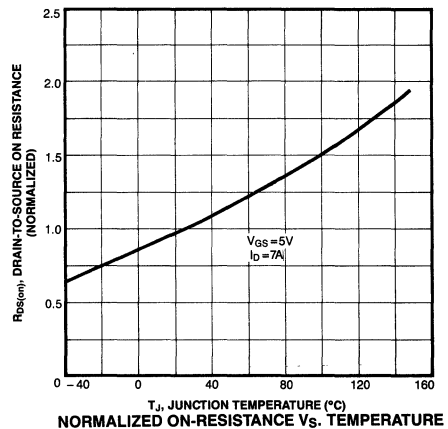
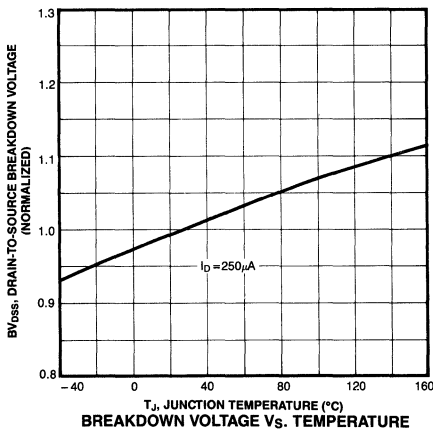
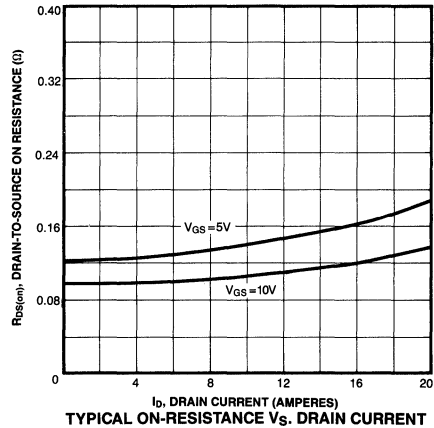
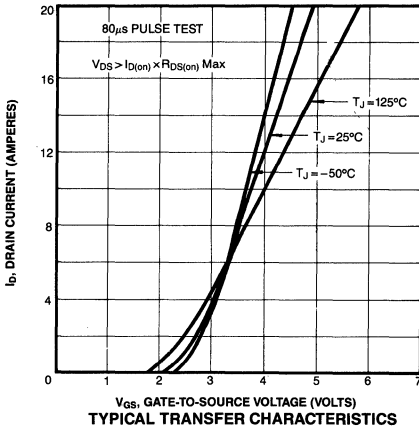
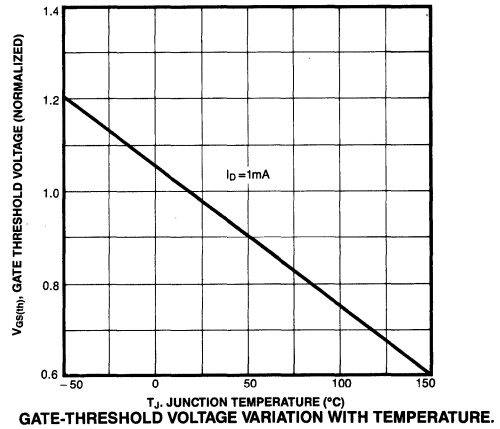
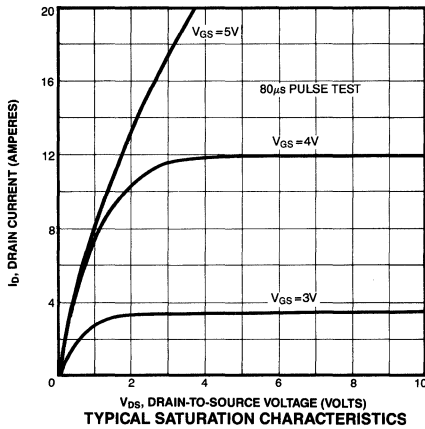
TYPICAL GATE CHARGE V_{GS} , GATE-TO-SOURCE VOLTAGE



MAXIMUM SAFE OPERATING AREA



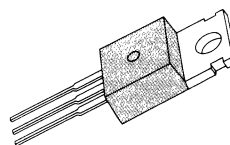
POWER V_{GS} , TEMPERATURE DERATING CURVE



FEATURES

- Lower $R_{DS(on)}$
- Excellent voltage stability
- Fast switching speeds
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability
- TO-220 Package

TO-220



1. Gate 2. Drain 3. Source

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	$I_{D(on)}$
IRL540	100V	0.11 Ω	24A
IRL541	80V	0.11 Ω	24A

MAXIMUM RATINGS

Characteristic	Symbol	IRL530	IRL531	Units
Drain-Source Voltage (1)	V_{DS}	100	80	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$) (1)	V_{DGR}	100	80	Vdc
Gate-Source Voltage	V_{GS}	± 15		Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	24	24	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	18	18	Adc
Drain Current — Pulsed (3)	I_{DM}	96	96	Adc
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	125 1.0		Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	- 55 to 150		$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300		$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse width limited by max. junction temperature

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage IRL540 IRL541	100 80	— —	— —	V	$V_{GS} = 0V$ $I_D = 250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	$V_{DS} = V_{GS}$, $I_D = 1mA$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS} = 15V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	$V_{GS} = -15V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0V$
		—	—	1.0	mA	$V_{DS} = \text{Max. Rating} \times 0.8$, $V_{GS} = 0V$, $T_C = 125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2)	24	—	—	A	$V_{DS} \geq I_{D(on)} \times R_{DS(on)max}$, $V_{GS} = 5.0V$
$R_{DS(on)}$	Static Drain-Source On State Resistance (2)	—	—	0.11	Ω	$V_{GS} = 5.0V$, $I_D = 12A$
g_{fs}	Forward Transconductance (2)	10	—	—	Ω	$V_{DS} \geq 25V$, $I_D = 12A$
C_{iss}	Input Capacitance	—	1500	—	pF	$V_{GS} = 0V$, $V_{DS} = 25V$, $f = 1.0MHz$
C_{oss}	Output Capacitance	—	400	—	pF	
C_{rss}	Reverse Transfer Capacitance	—	180	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	—	30	ns	$V_{DD} = 0.5 BV_{DSS}$, $I_D = 12A$, $Z_O = 50 \Omega$ (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	—	—	110	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	—	60	ns	
t_f	Fall Time	—	—	75	ns	
Q_g	Total Gate Charge	—	39	60	nC	$V_{GS} = 5V$, $I_D = 24A$, $V_{DS} = 0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature)
Q_{gs}	Gate-Source Charge	—	12	—	nC	
Q_{gd}	Gate-Drain Charge	—	27	—	nC	

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	—	—	1.0	K/W	
R_{thCS}	Case-to-Sink	—	0.5	—	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	—	—	80	K/W	Free Air Operation

Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C

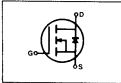
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

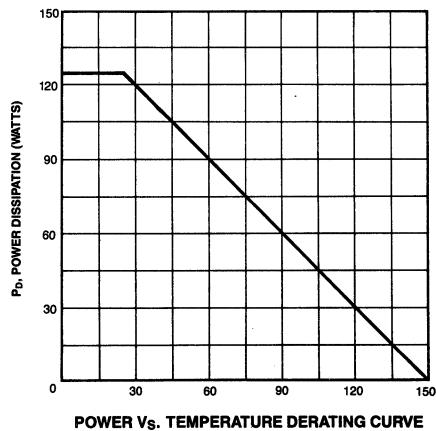
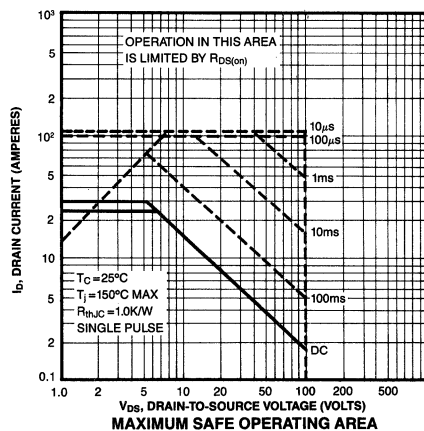
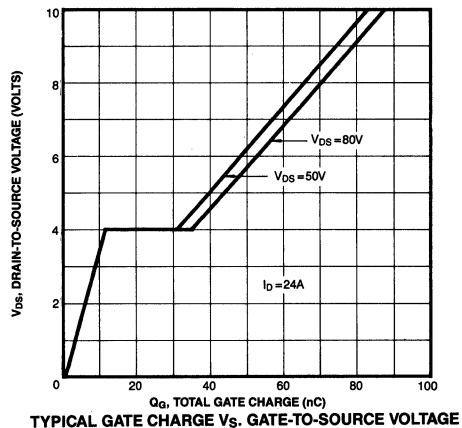
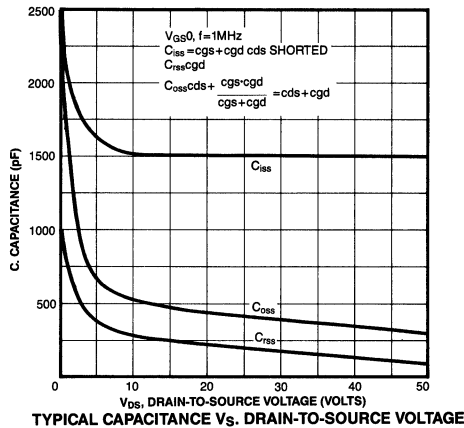
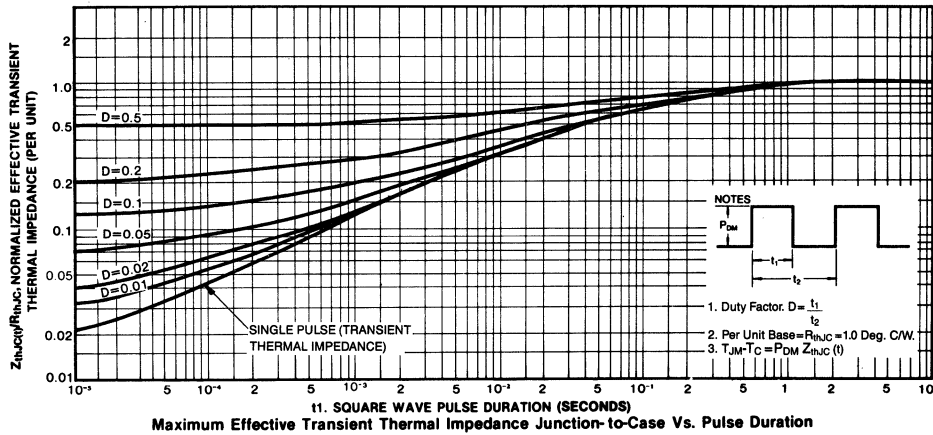
(3) Repetitive rating: Pulse width limited by max. junction temperature

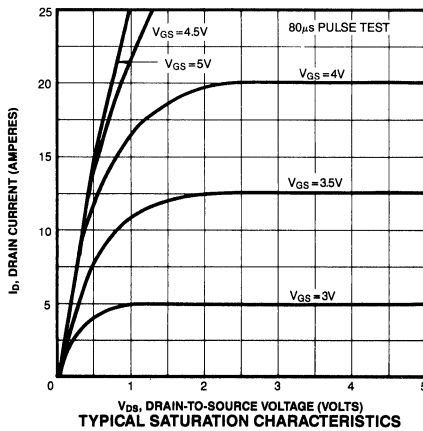
SOURCE-DRAIN DIODE RATING AND CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
I_S	Continuous Source Current (Body Diode)	—	—	24	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier
I_{SM}	Pulse Source Current (Body Diode) (3)	—	—	96	A	
V_{SD}	Diode Forward Voltage (2)	—	—	2.5	V	$T_C = 25^{\circ}\text{C}$, $I_S = 24\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	—	500	ns	$T_J = 25^{\circ}\text{C}$, $I_F = 24\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$

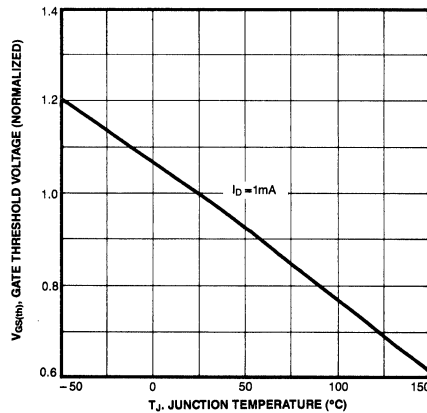
Notes: (1) $T_J = 25^{\circ}\text{C}$ to 150°C
(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse width limited by max. junction temperature



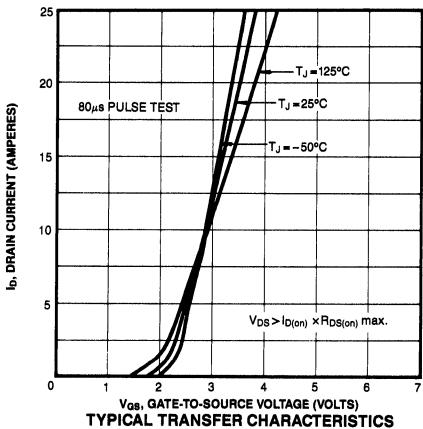




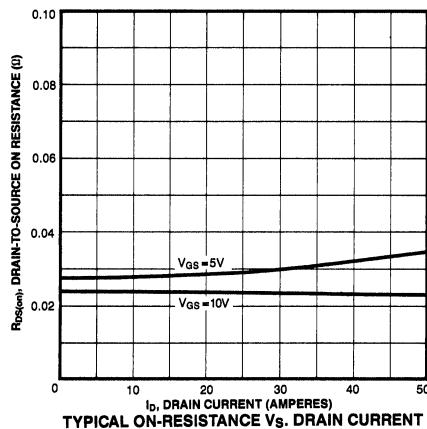
TYPICAL SATURATION CHARACTERISTICS



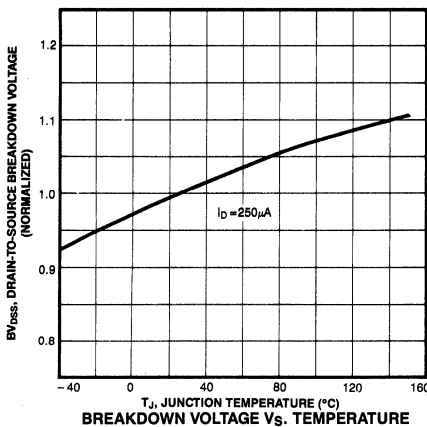
GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE.



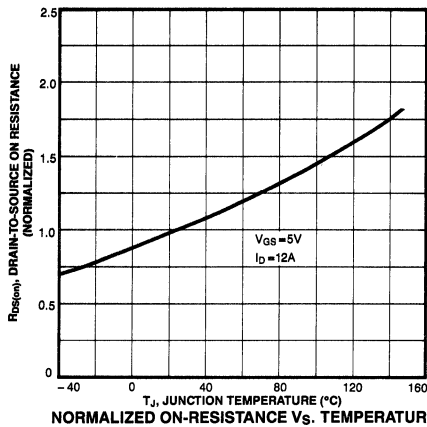
TYPICAL TRANSFER CHARACTERISTICS



TYPICAL ON-RESISTANCE V_S , DRAIN CURRENT



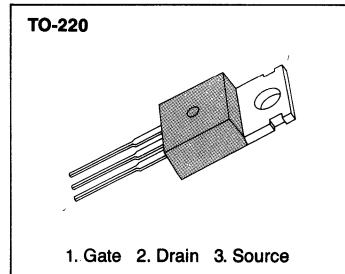
BREAKDOWN VOLTAGE V_S , TEMPERATURE



NORMALIZED ON-RESISTANCE V_S , TEMPERATURE

FEATURES

- Lower $R_{DS(on)}$
- Excellent voltage stability
- Fast switching speeds
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability
- TO-220 Package


PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	$I_{D(on)}$
IRL610	200V	2.4Ω	2.6A
IRL611	150V	2.4Ω	2.6A

MAXIMUM RATINGS

Characteristic	Symbol	IRL610	IRL611	Units
Drain-Source Voltage (1)	V_{DSS}	200	150	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$) (1)	V_{DGR}	200	150	Vdc
Gate-Source Voltage	V_{GS}	± 15		Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	2.6	2.6	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	1.6	1.6	Adc
Drain Current — Pulsed (3)	I_{DM}	8.0	8.0	Adc
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	25 0.2		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	- 55 to 150		°C
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300		°C

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$
 (2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
 (3) Repetitive rating: Pulse width limited by max. junction temperature

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
BV_{DSS}	Drain Source Breakdown Voltage IRL610 IRL611	200 150	— —	— —	V	$V_{GS} = 0V$ $I_D = 250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	$V_{DS} = V_{GS}$, $I_D = 1mA$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS} = 15V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	$V_{GS} = -15V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS} = \text{Max.}$ Rating $V_{GS} = 0V$
		—	—	1.0	mA	$V_{DS} = \text{Max.}$ Rating $\times 0.8$, $V_{GS} = 0V$, $T_C = 125^\circ\text{C}$
$I_{D(on)}$	On-State Drain Source Current (2)	2.6	—	—	A	$V_{DS} \geq I_{D(on)} \times R_{DS(on)max}$, $V_{GS} = 5.0V$
$R_{DS(on)}$	Static Drain Source On State Resistance (2)	—	—	2.40	Ω	$V_{GS} = 5.0V$, $I_D = 1.0A$
g_{fs}	Forward Transconductance (2)	0.8	—	—	S	$V_{DS} \geq 50V$, $I_D = 1.0A$
C_{iss}	Input Capacitance	—	220	—	pF	$V_{GS} = 0V$, $V_{DS} = 25V$ $f = 1.0MHz$
C_{oss}	Output Capacitance	—	45	—	pF	
C_{rss}	Reverse Transfer Capacitance	—	23	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	8.0	15	ns	$V_{DD} = 0.5 BV_{DSS}$, $I_D = 1.0A$, $Z_\theta = 15 \Omega$ (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	—	8.0	25	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	10	15	ns	
t_f	Fall Time	—	8.0	15	ns	
Q_g	Total Gate Charge	—	5.8	7.5	nC	$V_{GS} = 5V$, $I_D = 2.6A$, $V_{DS} = 0.8$ Max. Rating (Gate charge is essentially independent of operating temperature)
Q_{gs}	Gate Source Charge	—	1.9	—	nC	
Q_{gd}	Gate Drain Charge	—	3.9	—	nC	

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	—	—	5.0	K/W	
R_{thCS}	Case-to-Sink	—	0.5	—	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	—	—	80	K/W	Free Air Operation

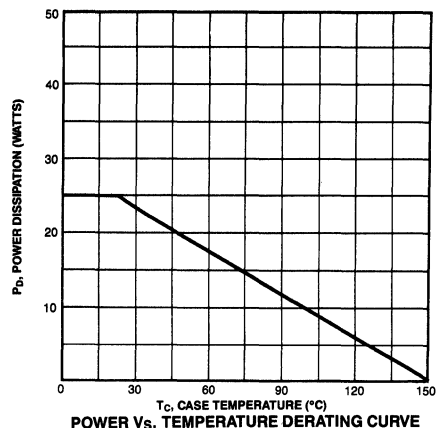
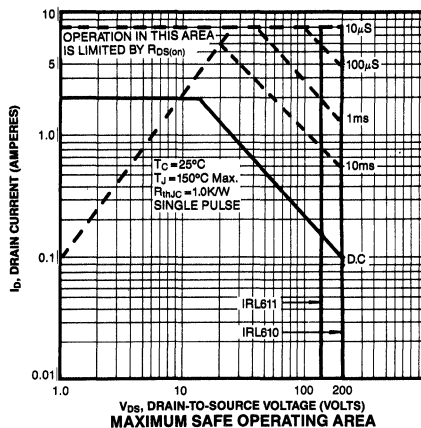
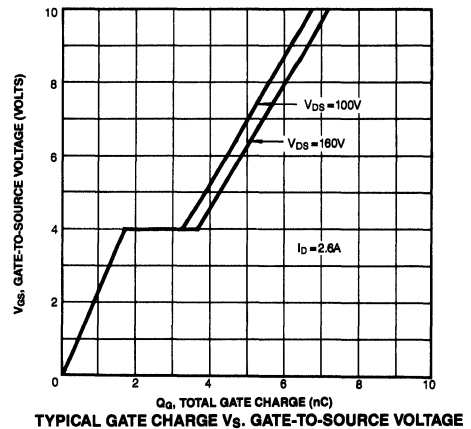
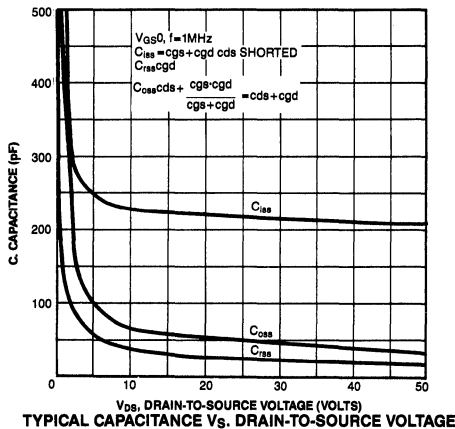
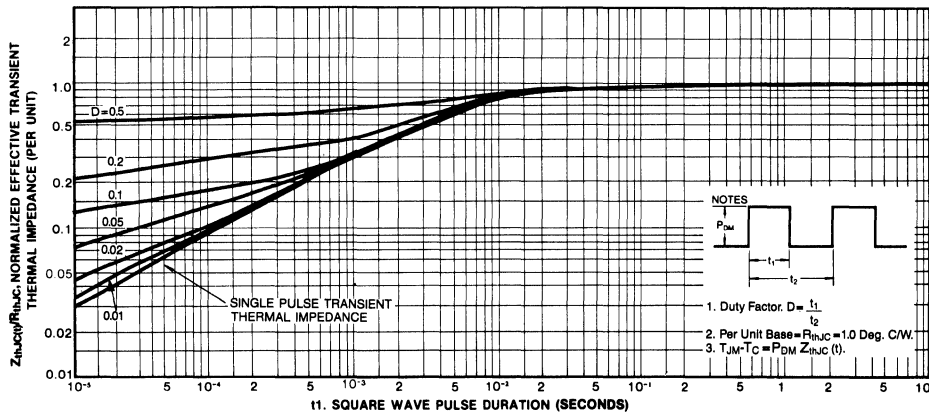
Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

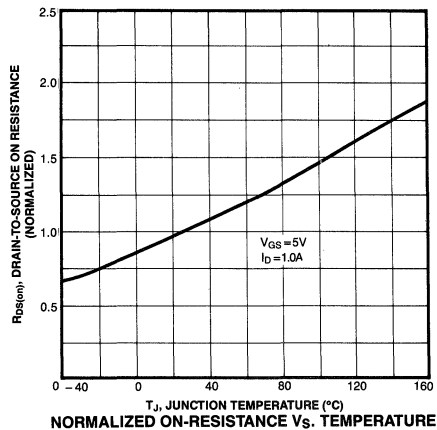
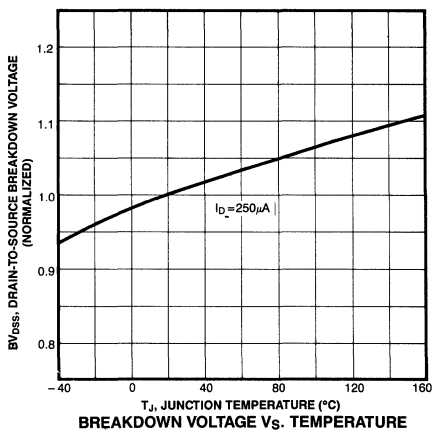
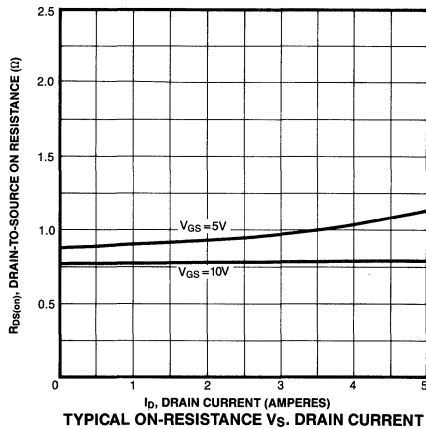
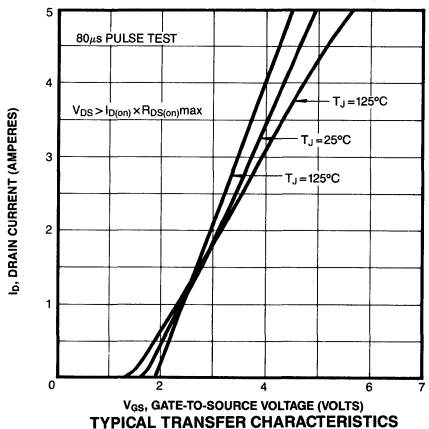
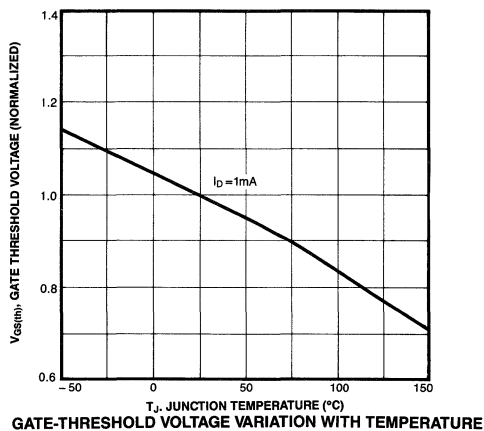
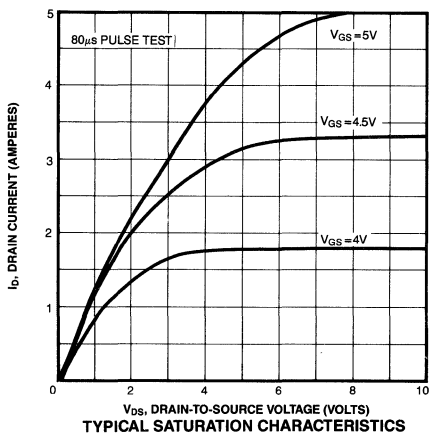
(3) Repetitive rating: Pulse width limited by max. junction temperature

SOURCE-DRAIN DIODE RATING AND CHARACTERISTIC

Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
I_S	Continuous Source Current (Body Diode)	—	—	2.6	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier
I_{SM}	Pulse Source Current (Body Diode) (3)	—	—	8.0	A	
V_{SD}	Diode Forward Voltage (2)	—	—	1.8	V	$T_C = 25^\circ\text{C}$, $I_S = 2.6\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	150	—	ns	$T_J = 25^\circ\text{C}$, $I_F = 2.6\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$

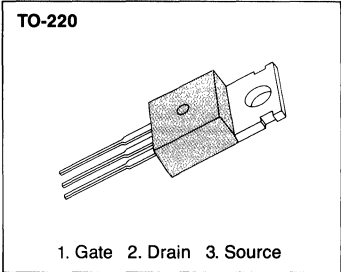
Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C
(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse width limited by max. junction temperature





FEATURES

- Lower $R_{DS(on)}$
- Excellent voltage stability
- Fast switching speeds
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability
- TO-220 Package



PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	$I_{D(on)}$
IRL620	200V	1.2 Ω	4.0A
IRL621	150V	1.2 Ω	4.0A

MAXIMUM RATINGS

Characteristic	Symbol	IRL620	IRL621	Units
Drain-Source Voltage (1)	V_{DSS}	200	150	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$) (1)	V_{DGR}	200	150	Vdc
Gate-Source Voltage	V_{GS}	± 15		Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	4.0	4.0	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	2.5	2.5	Adc
Drain Current — Pulsed (3)	I_{DM}	16	16	Adc
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	42 0.33		Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	- 55 to 150		$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300		$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse width limited by max. junction temperature

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

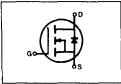
Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage IRL620 IRL621	200 150	— —	— —	V	$V_{GS} = 0V$ $I_D = 250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	$V_{DS} = V_{GS}$, $I_D = 1mA$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS} = 15V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	$V_{GS} = -15V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0V$
		—	—	1.0	mA	$V_{DS} = \text{Max. Rating} \times 0.8$, $V_{GS} = 0V$, $T_C = 125^\circ\text{C}$
$I_{D(on)}$	On-State Drain Source Current (2)	4.0	—	—	A	$V_{DS} \geq I_{D(on)} \times R_{DS(on)max}$, $V_{GS} = 5.0V$
$R_{DS(on)}$	Static Drain Source On State Resistance (2)	—	—	1.2	Ω	$V_{GS} = 5.0V$, $I_D = 2.0A$
g_{fs}	Forward Transconductance (2)	3.0	—	—	S	$V_{DS} \geq 25V$, $I_D = 2.0A$
C_{iss}	Input Capacitance	—	450	—	pF	$V_{GS} = 0V$, $V_{DS} = 25V$, $f = 1.0MHz$
C_{oss}	Output Capacitance	—	140	—	pF	
C_{rss}	Reverse Transfer Capacitance	—	60	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	—	40	ns	$V_{DD} = 0.5 BV_{DSS}$, $I_D = 2.0A$, $Z_O = 50 \Omega$ (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	—	—	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	—	100	ns	
t_f	Fall Time	—	—	60	ns	
Q_g	Total Gate Charge	—	15	17	nC	$V_{GS} = 5V$, $I_D = 4.0A$, $V_{DS} = 0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature)
Q_{gs}	Gate Source Charge	—	8.5	—	nC	
Q_{gd}	Gate Drain Charge	—	6.3	—	nC	

THERMAL RESISTANCE

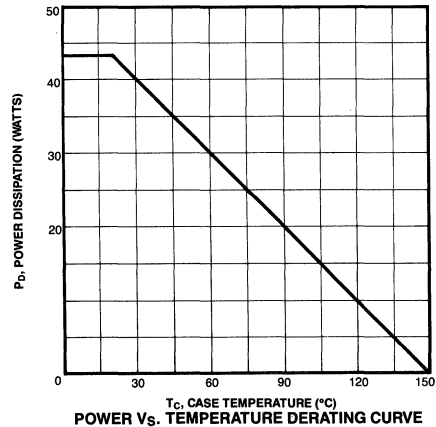
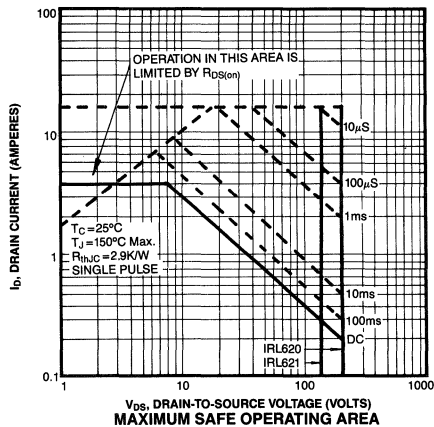
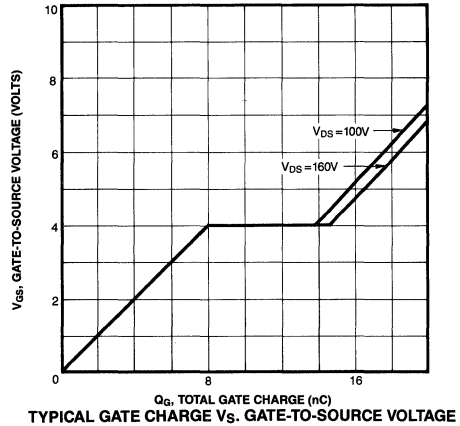
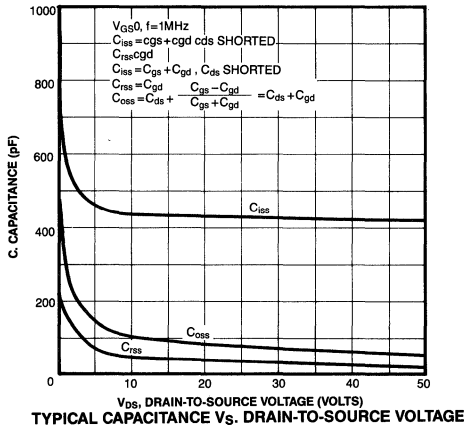
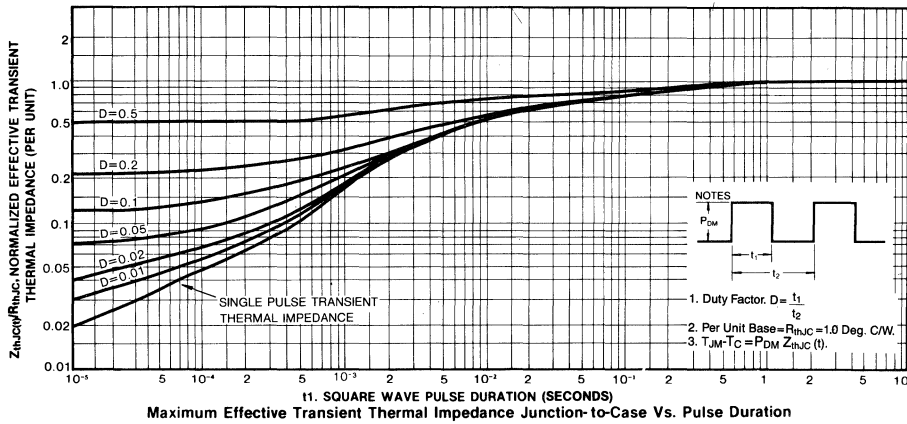
R_{thJC}	Junction-to-Case	—	—	3.0	K/W	
R_{thJC}	Case-to-Sink	—	0.5	—	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	—	—	80	K/W	Free Air Operation

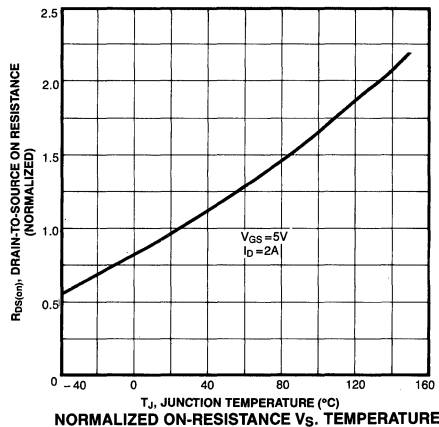
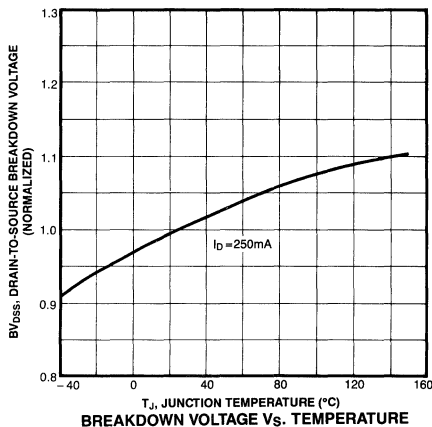
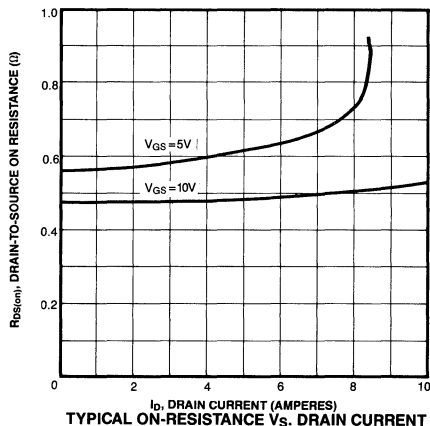
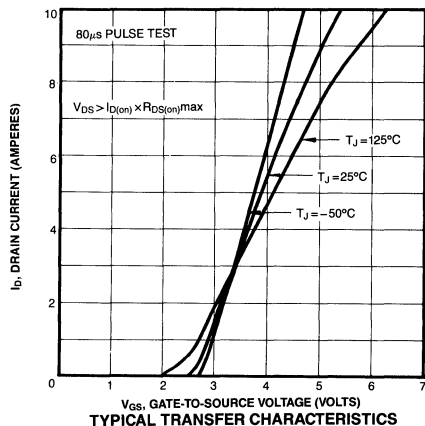
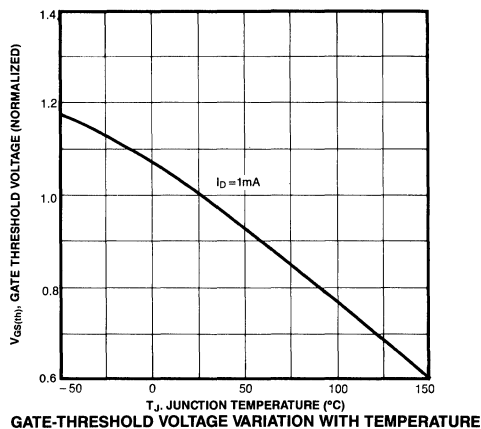
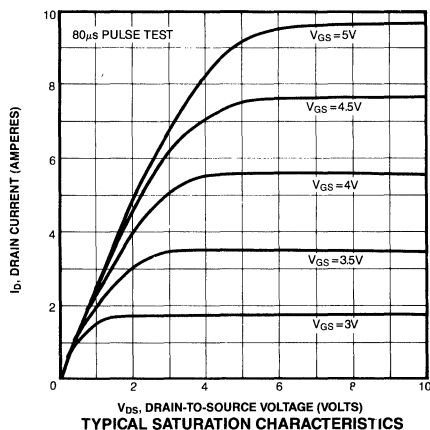
Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C
 (2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
 (3) Repetitive rating: Pulse width limited by max. junction temperature

SOURCE-DRAIN DIODE RATING AND CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
I_S	Continuous Source Current (Body Diode)	—	—	4.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier 
I_{SM}	Pulse Source Current (Body Diode) (3)	—	—	16	A	
V_{SD}	Diode Forward Voltage (2)	—	—	1.8	V	$T_C = 25^{\circ}\text{C}$, $I_S = 4.0\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	400	—	ns	$T_J = 25^{\circ}\text{C}$, $I_F = 4.0\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$

Notes: (1) $T_J = 25^{\circ}\text{C}$ to 150°C
(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse width limited by max. junction temperature

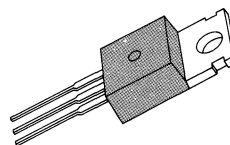




FEATURES

- Lower $R_{DS(on)}$
- Excellent voltage stability
- Fast switching speeds
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Logic level operating

TO-220



1. Gate 2. Drain 3. Source

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	$I_{D(on)}$
IRL624	250V	1.3Ω	3.3A

MAXIMUM RATINGS

Characteristic	Symbol	IRL624	Units
Drain-Source Voltage (1)	V_{DS}	250	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$) (1)	V_{DGR}	250	Vdc
Gate-Source Voltage	V_{GS}	± 15	Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	3.3	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	2.1	Adc
Drain Current — Pulsed (3)	I_{DM}	13	Adc
Gate Current — Pulsed	I_{GM}	± 1.5	Adc
Single Pulsed Avalanche Energy (4)	E_{AS}	85	mJ
Avalanche Current	I_{AS}	3.3	A
Total Power Dissipation @ $T_C=25^\circ C$	P_D	40	Watts
Derate above $25^\circ C$		0.32	W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300	$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse width limited by max. junction temperature

(4) $L=12mH$, $V_{dd}=50V$, $R_G=25\Omega$, STARTING $T_J=25^\circ C$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

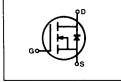
Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
BV_{DSS}	Drain Source Breakdown Voltage	250	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	$V_{DS} = V_{GS}, I_D = 1mA$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS} = 15V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	$V_{GS} = -15V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS} = \text{Max. Rating } V_{GS} = 0V$
		—	—	1000	μA	$V_{DS} = \text{Max. Rating} \times 0.8, V_{GS} = 0V, T_C = 125^\circ\text{C}$
$I_{D(on)}$	On-State Drain Source Current (2)	3.3	—	—	A	$V_{DS} \geq I_{D(on)} \times R_{DS(on)max}, V_{GS} = 5V$
$R_{DS(on)}$	Static Drain Source On State Resistance (2)	—	—	1.3	Ω	$V_{GS} = 5V, I_D = 1.7A$
g_{fs}	Forward Transconductance (2)	1.4	3.5	—	Ω	$V_{DS} \geq I_{D(on)} \times R_{DS(on)max}, I_D = 1.7A$
C_{iss}	Input Capacitance	—	460	—	pF	$V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz$
C_{oss}	Output Capacitance	—	55	—	pF	
C_{rss}	Reverse Transfer Capacitance	—	20	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	—	17	ns	$V_{DD} = 0.5 BV_{DSS}, I_D = 1.7A, Z_O = 18\Omega$ (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	—	—	36	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	—	40	ns	
t_f	Fall Time	—	—	20	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	14	22	nC	$V_{GS} = 5V, I_D = 3.3A, V_{DS} = 0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature)
Q_{gs}	Gate Source Charge	—	2.2	6.0	nC	
Q_{gd}	Gate Drain Charge	—	5.6	11	nC	

THERMAL RESISTANCE

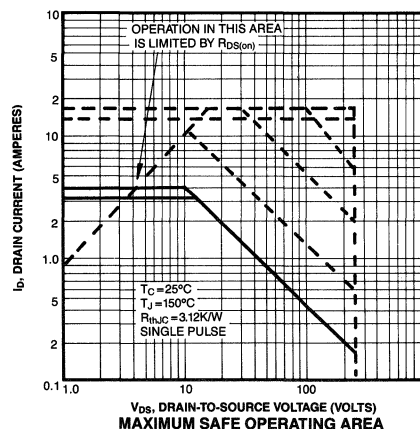
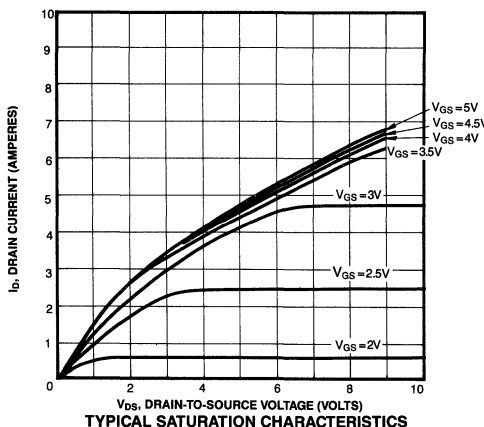
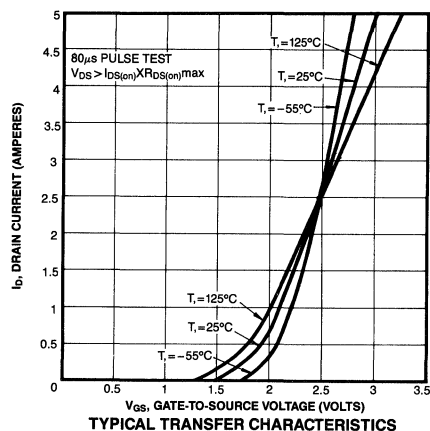
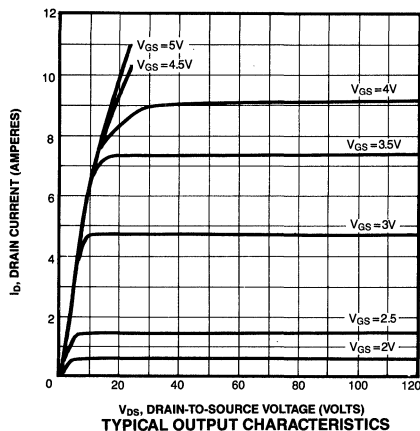
R_{thJC}	Junction-to-Case	—	—	3.12	K/W	
R_{thCS}	Case-to-Sink	—	1.0	—	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	—	—	80	K/W	Free Air Operation

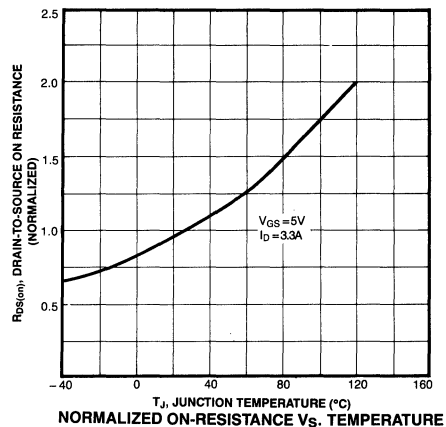
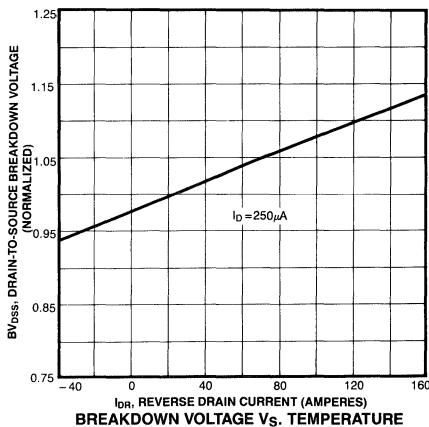
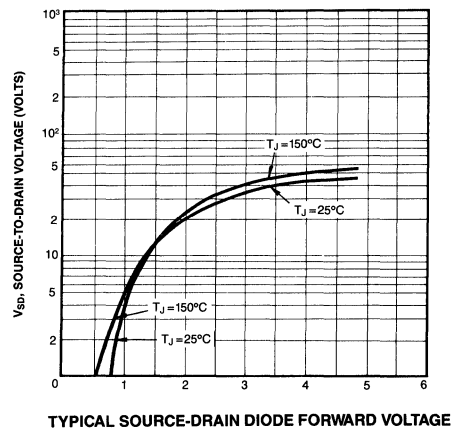
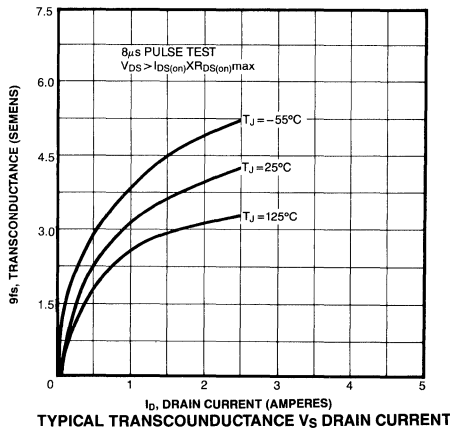
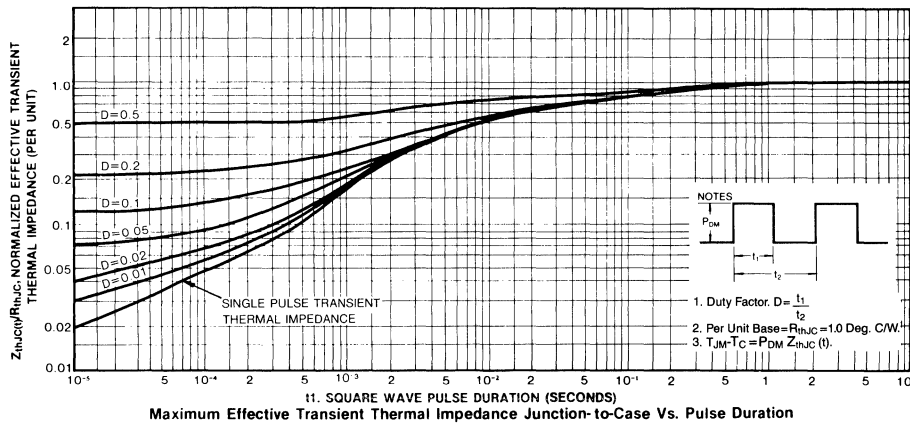
- Notes:**
- (1) $T_J = 25^\circ\text{C}$ to 150°C
 - (2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
 - (3) Repetitive rating: Pulse width limited by max. junction temperature

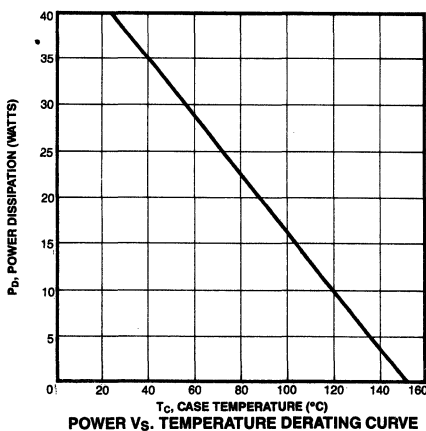
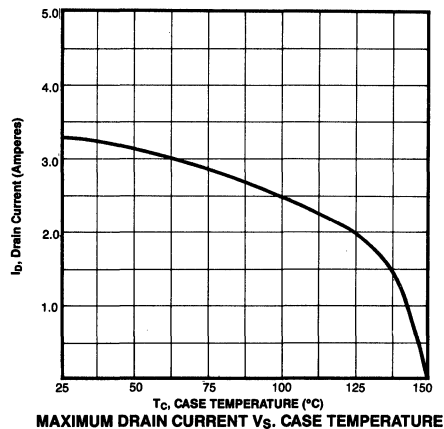
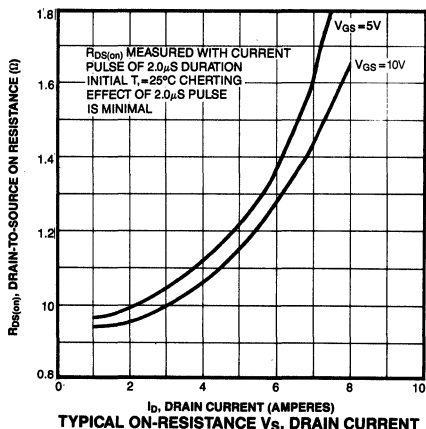
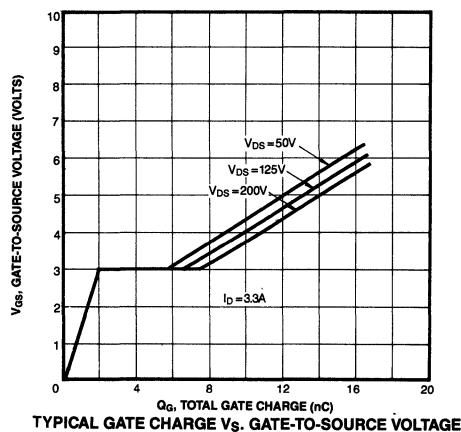
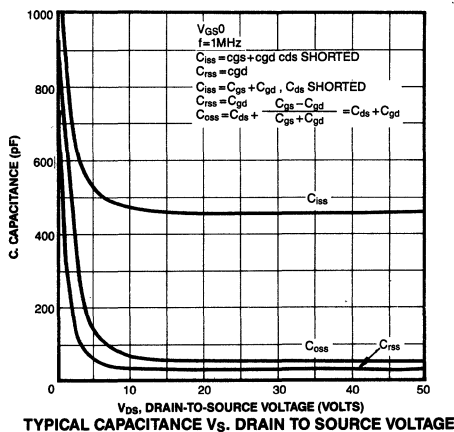
SOURCE-DRAIN DIODE RATING AND CHARACTERISTIC

Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
I_S	Continuous Source Current (Body Diode)	—	—	3.3	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier 
I_{SM}	Pulse Source Current (Body Diode) (3)	—	—	13	A	
V_{SD}	Diode Forward Voltage (2)	—	—	1.8	V	$T_C = 25^\circ\text{C}$, $I_S = 3.3\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	180	—	ns	$T_J = 25^\circ\text{C}$, $I_F = 3.3\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{s}$

- Notes:**
- (1) $T_J = 25^\circ\text{C}$ to 150°C
 - (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
 - (3) Repetitive rating: Pulse width limited by max. junction temperature



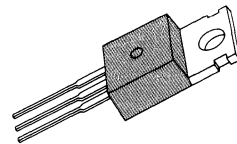




FEATURES

- Lower $R_{DS(on)}$
- Excellent voltage stability
- Fast switching speeds
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability
- TO-220 Package

TO-220



1. Gate 2. Drain 3. Source

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	$I_{D(on)}$
IRL630	200V	0.6 Ω	8.0A
IRL631	150V	0.6 Ω	8.0A

MAXIMUM RATINGS

Characteristic	Symbol	IRL630	IRL631	Units
Drain-Source Voltage (1)	V_{DSS}	200	150	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$) (1)	V_{DGR}	200	150	Vdc
Gate-Source Voltage	V_{GS}	± 15		Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	8.0	8.0	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	6.0	6.0	Adc
Drain Current — Pulsed (3)	I_{DM}	32	32	Adc
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	75 0.6		Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300		$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse width limited by max. junction temperature

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic		Min	Typ	Max	Units	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage	IRL630 IRL631	200 150	— —	— —	V	$V_{GS} = 0V$ $I_D = 250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage		1.0	—	2.0	V	$V_{DS} = V_{GS}$, $I_D = 1mA$
I_{GSS}	Gate-Source Leakage Forward		—	—	100	nA	$V_{GS} = 15V$
I_{GSS}	Gate-Source Leakage Reverse		—	—	- 100	nA	$V_{GS} = -15V$
I_{DSS}	Zero Gate Voltage Drain Current		—	—	250	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0V$
			—	—	1.0	mA	$V_{DS} = \text{Max. Rating} \times 0.8$, $V_{GS} = 0V$, $T_C = 125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2)		8.0	—	—	A	$V_{DS} \geq I_{D(on)} \times R_{DS(on)max}$, $V_{GS} = 5.0V$
$R_{DS(on)}$	Static Drain-Source On State Resistance (2)		—	—	0.6	Ω	$V_{GS} = 5.0V$, $I_D = 4.0A$
g_{fs}	Forward Transconductance (2)		6.0	—	—	S	$V_{DS} \geq 50V$, $I_D = 4.0A$
C_{iss}	Input Capacitance		—	800	—	pF	$V_{GS} = 0V$, $V_{DS} = 25V$ $f = 1.0MHz$
C_{oss}	Output Capacitance		—	150	—	pF	
C_{rss}	Reverse Transfer Capacitance		—	50	—	pF	
$t_{d(on)}$	Turn-On Delay Time		—	—	30	ns	$V_{DD} = 0.5 BV_{DSS}$, $I_D = 4.0A$, $Z_O = 15\Omega$ (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time		—	—	50	ns	
$t_{d(off)}$	Turn-Off Delay Time		—	—	50	ns	
t_f	Fall Time		—	—	40	ns	
Q_g	Total Gate Charge		—	19	30	nC	$V_{GS} = 5V$, $I_D = 8.0A$, $V_{DS} = 0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature)
Q_{gs}	Gate-Source Charge		—	9	—	nC	
Q_{gd}	Gate-Drain Charge		—	10	—	nC	

THERMAL RESISTANCE

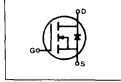
ALL	Junction-to-Case	—	—	1.7	K/W	
ALL	Case-to-Sink	—	0.5	—	K/W	Mounting surface flat, smooth, and greased
ALL	Junction-to-Ambient	—	—	80	K/W	Free Air Operation

Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C

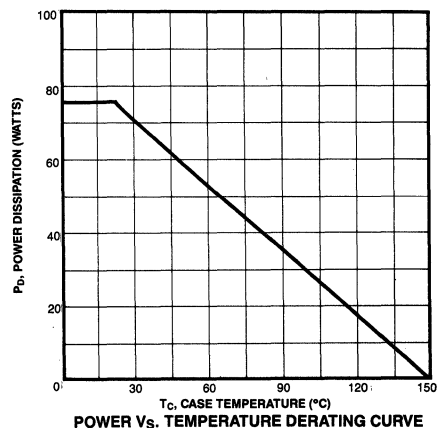
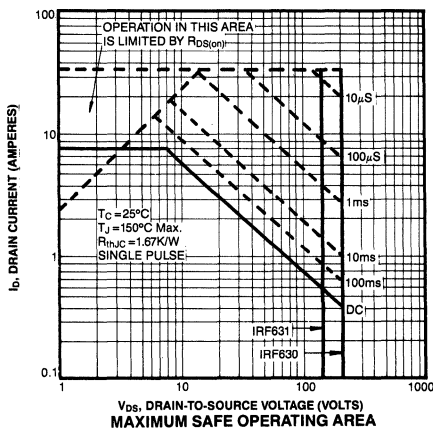
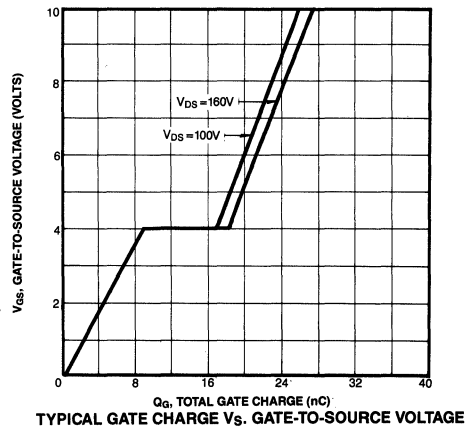
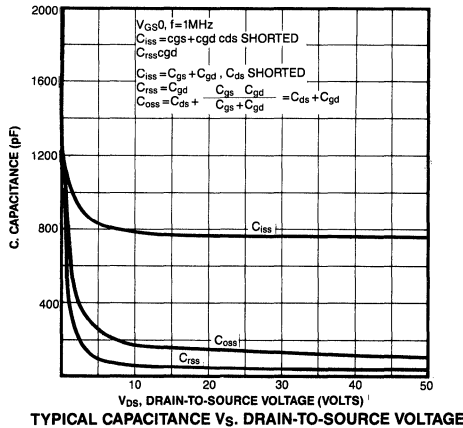
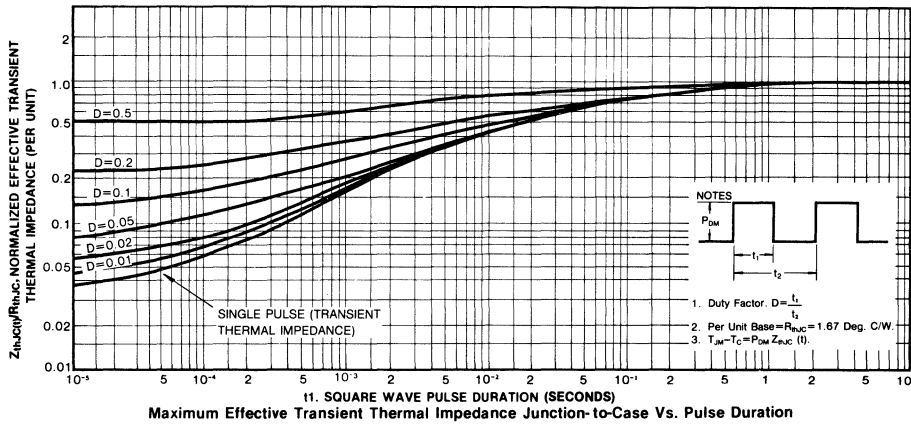
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

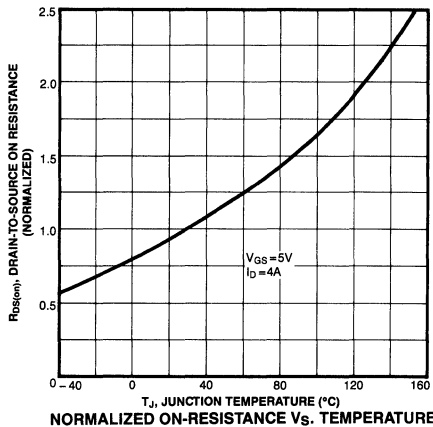
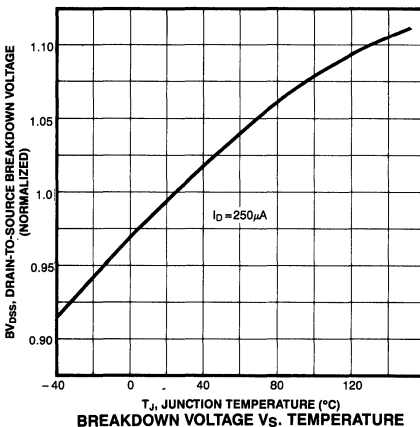
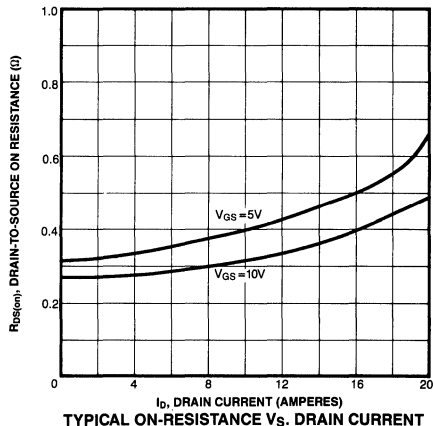
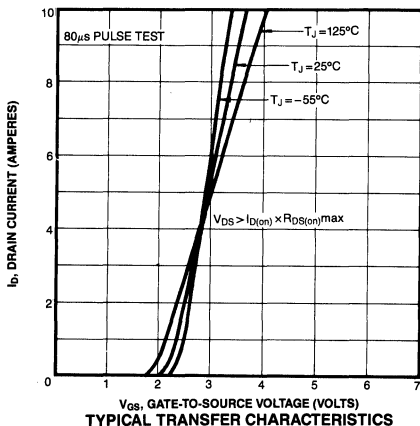
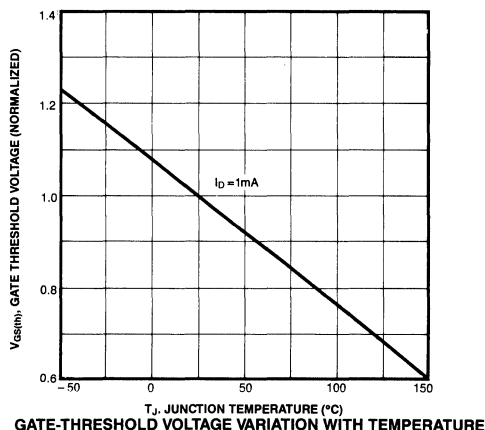
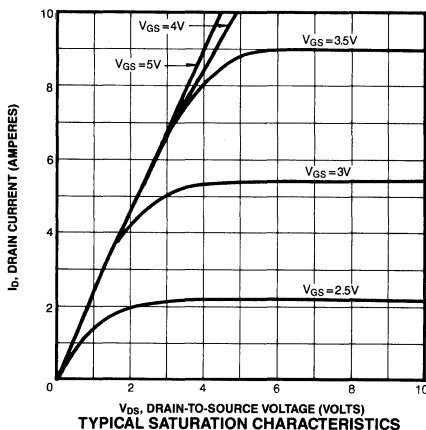
(3) Repetitive rating: Pulse width limited by max. junction temperature

SOURCE-DRAIN DIODE RATING AND CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
I_S	Continuous Source Current (Body Diode)	—	—	8.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier 
I_{SM}	Pulse Source Current (Body Diode) (3)	—	—	32	A	
V_{sp}	Diode Forward Voltage (2)	—	—	2.0	V	$T_C = 25^\circ\text{C}$, $I_S = 8.0\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	450	—	ns	$T_J = 25^\circ\text{C}$, $I_F = 8.0\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$

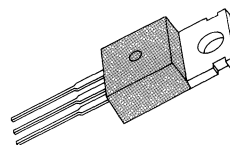
- Notes:** (1) $T_J = 25^\circ\text{C}$ to 150°C
 (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
 (3) Repetitive rating: Pulse width limited by max. junction temperature





FEATURES

- Lower $R_{DS(on)}$
- Excellent voltage stability
- Fast switching speeds
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability
- TO-220 Package

TO-220

1. Gate 2. Drain 3. Source
PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	$I_{D(on)}$
IRL640	200V	0.22Ω	16A
IRL641	150V	0.22Ω	16A

MAXIMUM RATINGS

Characteristic	Symbol	IRL640	IRL641	Units
Drain-Source Voltage (1)	V_{DSS}	200	150	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$) (1)	V_{DGR}	200	150	Vdc
Gate-Source Voltage	V_{GS}	± 15		Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	16	16	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	10	10	Adc
Drain Current — Pulsed (3)	I_{DM}	64	64	Adc
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	125 1.0		Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	- 55 to 150		$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300		$^\circ C$

Notes: (1) $T_J=25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse width limited by max. junction temperature

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic		Min	Typ	Max	Units	Test Condition
BV_{DS}	Drain-Source Breakdown Voltage	IRL640 IRL641	200 150	— —	— —	V	$V_{GS} = 0V$ $I_D = 250\mu A$
$V_{(th)}$	Gate Threshold Voltage		1.0	—	2.0	V	$V_{DS} = V_{GS}$, $I_D = 1mA$
I_{GSS}	Gate-Source Leakage Forward		—	—	100	nA	$V_{GS} = 15V$
I_{GSS}	Gate-Source Leakage Reverse		—	—	- 100	nA	$V_{GS} = -15V$
I_{DSS}	Zero Gate Voltage Drain Current		—	—	250	μA	$V_{DS} = \text{Max. Rating}$ $V_{GS} = 0V$
			—	—	1.0	mA	$V_{DS} = \text{Max. Rating} \times 0.8$, $V_{GS} = 0V$, $T_C = 125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2)		16	—	—	A	$V_{DS} \geq I_{D(on)} \times R_{DS(on)max}$, $V_{GS} = 5.0V$
$R_{DS(on)}$	Static Drain Source On State Resistance (2)		—	—	0.22	Ω	$V_{GS} = 5.0V$, $I_D = 8.0A$
g_{fs}	Forward Transconductance (2)		9	—	—	Ω	$V_{DS} \geq 50V$, $I_D = 8.0A$
C_{iss}	Input Capacitance		—	1400	—	pF	$V_{GS} = 0V$, $V_{DS} = 25V$ $f = 1.0MHz$
C_{oss}	Output Capacitance		—	240	—	pF	
C_{rss}	Reverse Transfer Capacitance		—	90	—	pF	
$t_{d(on)}$	Turn-On Delay Time		—	—	30	ns	$V_{DD} = 0.5 BV_{DS}$, $I_D = 8.0A$, $Z_O = 50 \Omega$ (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time		—	—	60	ns	
$t_{d(off)}$	Turn-Off Delay Time		—	—	80	ns	
t_f	Fall Time		—	—	60	ns	
Q_g	Total Gate Charge		—	44	—	nC	$V_{GS} = 5V$, $I_D = 16A$, $V_{DS} = 0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature)
Q_{gs}	Gate Source Charge		—	9	—	nC	
Q_{gd}	Gate Drain Charge		—	35	—	nC	

THERMAL RESISTANCE

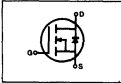
R_{thJC}	Junction-to-Case	—	—	1.0	K/W	
R_{thCS}	Case-to-Sink	—	0.5	—	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	—	—	80	K/W	Free Air Operation

Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C

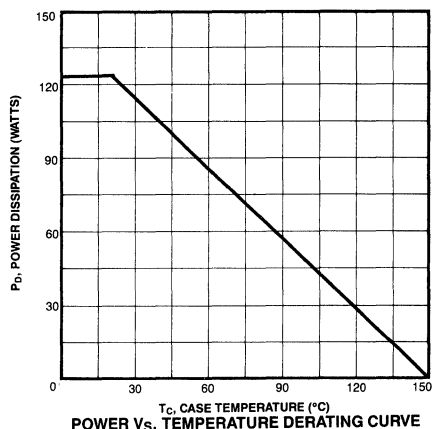
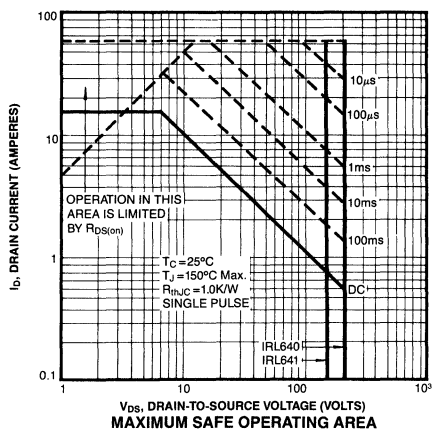
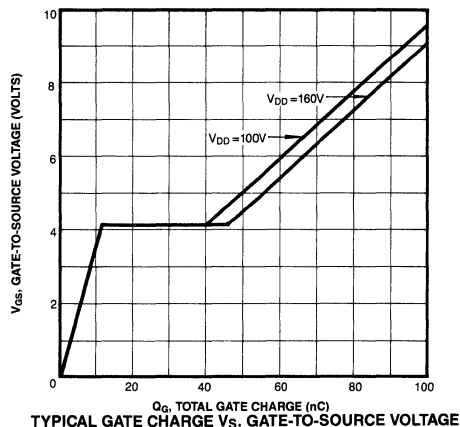
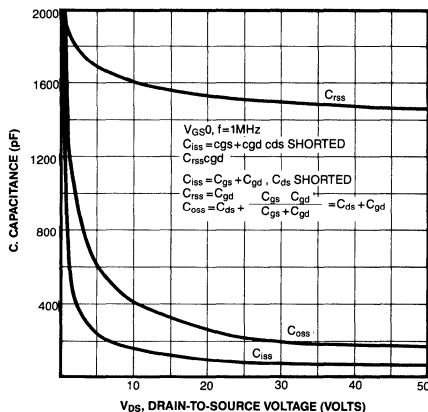
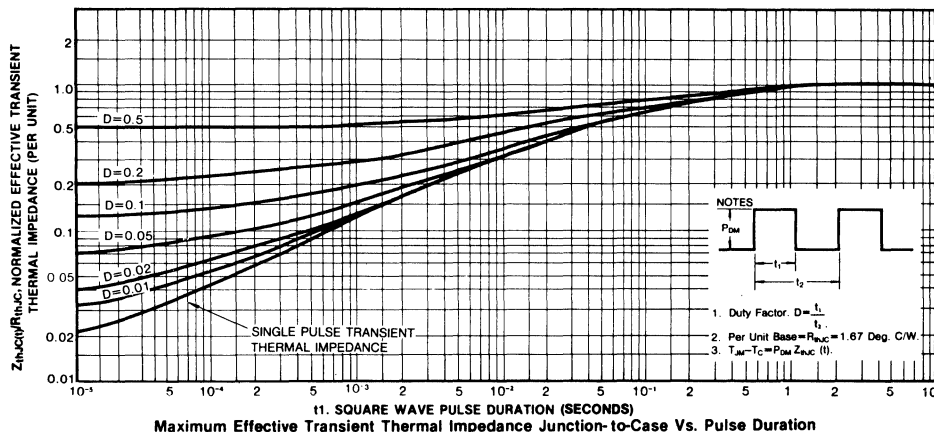
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

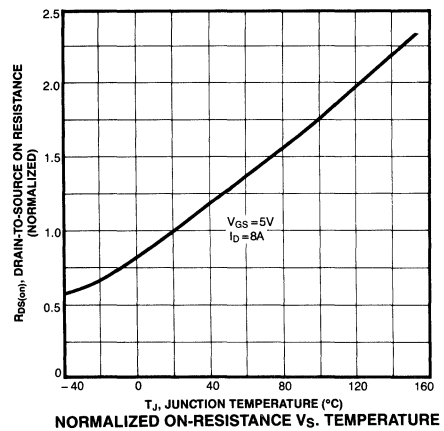
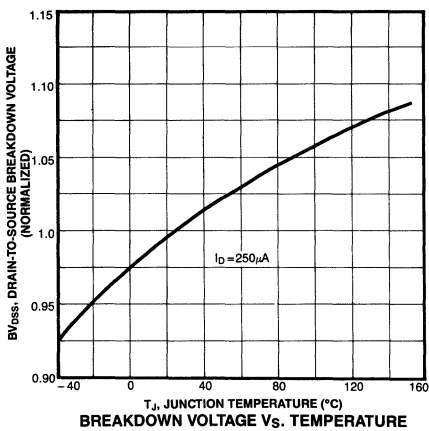
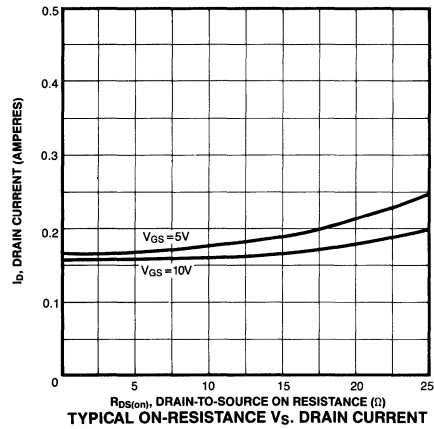
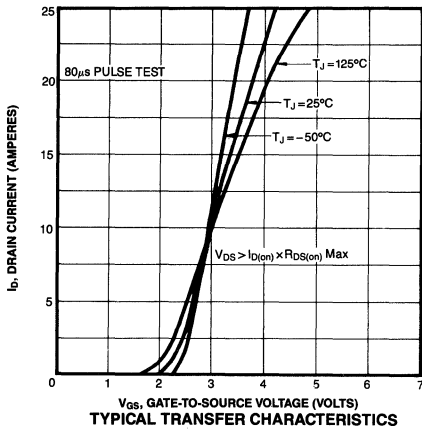
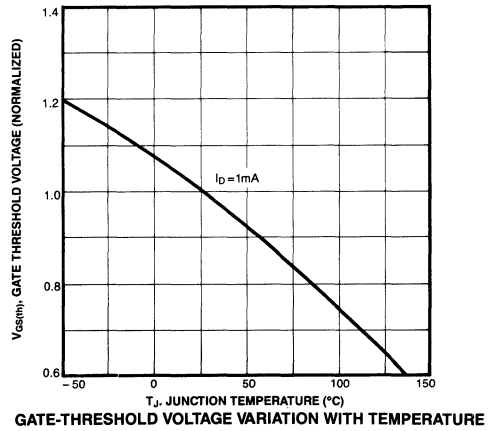
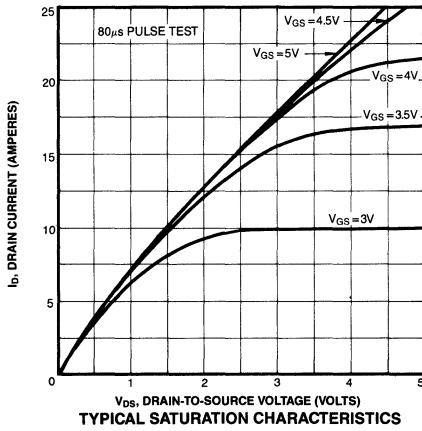
(3) Repetitive rating: Pulse width limited by max. junction temperature

SOURCE-DRAIN DIODE RATING AND CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
I_S	Continuous Source Current (Body Diode)	—	—	16	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier 
I_{SM}	Pulse Source Current (Body Diode) (3)	—	—	64	A	
V_{SD}	Diode Forward Voltage (2)	—	—	2.0	V	$T_C = 25^\circ\text{C}$, $I_S = 16\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	650	—	ns	$T_J = 25^\circ\text{C}$, $I_F = 16\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$

Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C
 (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
 (3) Repetitive rating: Pulse width limited by max. junction temperature





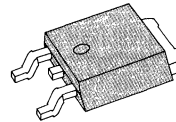
FEATURES

- Lower $R_{DS(on)}$
- Excellent voltage stability
- Fast switching speeds
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability
- D-PAK/I-PAK

PRODUCT SUMMARY

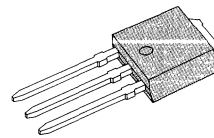
Part Number	V_{DS}	$R_{DS(on)}$	$I_{D(on)}$
IRLR014/IRLU014	60V	0.30 Ω	6.7A
IRLR010/IRLU010	50V	0.30 Ω	6.7A

D-PAK



IRLR010/014

I-PAK



IRLU010/014

MAXIMUM RATINGS

Characteristic	Symbol	IRLR014 IRLU014	IRLR010 IRLU010	Units
Drain-Source Voltage (1)	V_{DSS}	60	50	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$) (1)	V_{DGR}	60	50	Vdc
Gate-Source Voltage	V_{GS}	± 15		Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	6.7	6.7	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	4.2	4.2	Adc
Drain Current—Pulsed (3)	I_{DM}	27	27	Adc
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	25 0.20		Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ C$
Maximum Lead Temp, for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300		$^\circ C$

Notes: (1) $T_J = 25^\circ C$ to $150^\circ C$
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse width limited by max. junction temperature

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

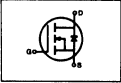
Symbol	Characteristic		Min	Typ	Max	Units	Test Condition
BV_{DSS}	Drain Source Breakdown Voltage	IRLR014	60	—	—	V	$V_{GS} = 0V$ $I_D = 250\mu A$
		IRLU014	60	—	—		
		IRLR010	50	—	—		
		IRLU010	50	—	—		
$V_{GS(th)}$	Gate Threshold Voltage		1.0	—	2.0	V	$V_{DS} = V_{GS}$, $I_D = 1.0mA$
I_{GSS}	Gate-Source Leakage Forward		—	—	100	nA	$V_{GS} = 15V$
I_{GSS}	Gate-Source Leakage Reverse		—	—	- 100	nA	$V_{GS} = -15V$
I_{DSS}	Zero Gate Voltage Drain Current		—	—	250	μA	$V_{DS} = \text{Max. Rating}$ $V_{GS} = 0V$
			—	—	1.0	mA	$V_{DS} = \text{Max. Rating} \times 0.8$, $V_{GS} = 0V$, $T_C = 125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2)		6.7	—	—	A	$V_{DS} \geq I_{D(on)} \times R_{DS(on)max}$, $V_{GS} = 5.0V$
$R_{DS(on)}$	Static Drain-Source On-State Resistance (2)		—	0.18	0.30	Ω	$V_{GS} = 5.0V$, $I_D = 4.0A$
g_{fs}	Forward Transconductance (2)		4.0	—	—	S	$V_{DS} \geq 15V$, $I_D = 4.0A$
C_{iss}	Input Capacitance		—	400	—	pF	$V_{GS} = 0V$, $V_{DS} = 25V$, $f = 1.0MHz$
C_{oss}	Output Capacitance		—	150	—	pF	
C_{rss}	Reverse Transfer Capacitance		—	50	—	pF	
$t_d(on)$	Turn-On Delay Time		—	12	20	ns	$V_{DD} = 0.5 BV_{DSS}$, $I_D = 4.0A$, $Z_O = 50\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time		—	35	50	ns	
$t_d(off)$	Turn-Off Delay Time		—	35	50	ns	
t_f	Fall Time		—	30	40	ns	
Q_g	Total Gate Charge		—	—	10	nC	$V_{GS} = 5V$, $I_D = 6.7A$, $V_{DS} = 0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature)
Q_{gs}	Gate-Source Charge		—	7	—	nC	
Q_{gd}	Gate-Drain Charge		—	1.5	—	nC	

THERMAL RESISTANCE

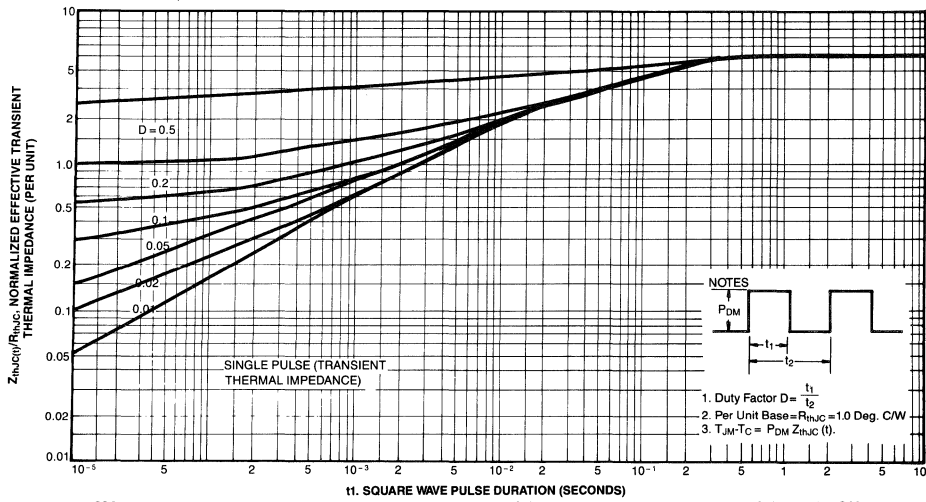
R_{thJC}	Junction-to-Case	—	—	5.0	K/W	
R_{thCS}	Case-to-Sink	—	1.7	—	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	—	—	110	K/W	Free Air Operation

Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse width limited by max. junction temperature

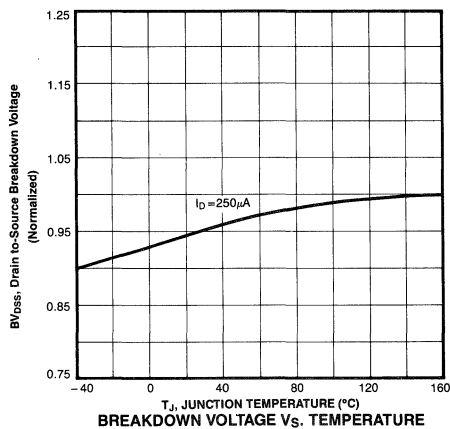
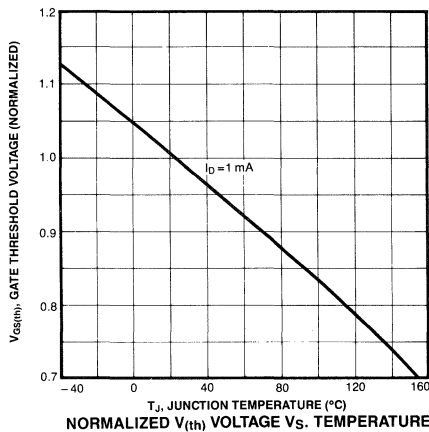
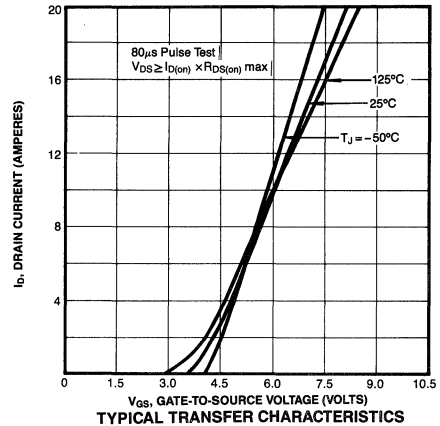
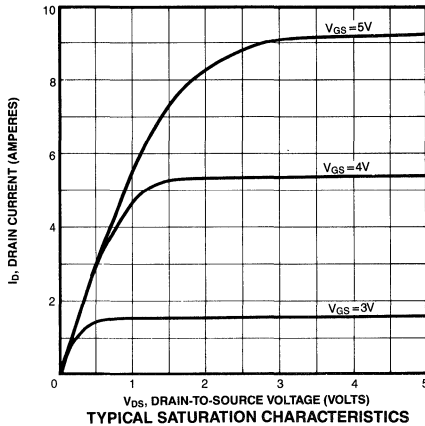
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

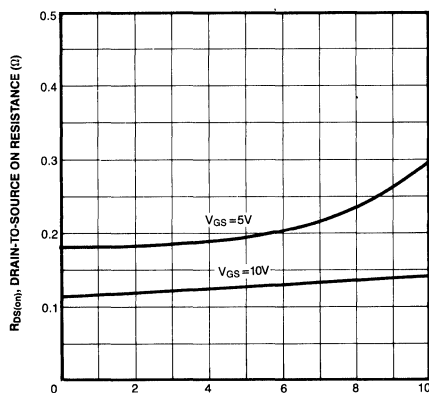
Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
I_S	Continuous Source Current (Body Diode)	—	—	6.7	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier 
I_{SM}	Pulse Source Current (Body Diode) (3)	—	—	27	A	
V_{SD}	Diode Forward Voltage (2)	—	—	1.8	V	$T_C = 25^{\circ}\text{C}$, $I_S = 6.7\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	—	200	ns	$T_J = 25^{\circ}\text{C}$, $I_F = 6.7\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$

Notes: (1) $T_J = 25^{\circ}\text{C}$, to 150°C
(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse with limited by max. junction temperature

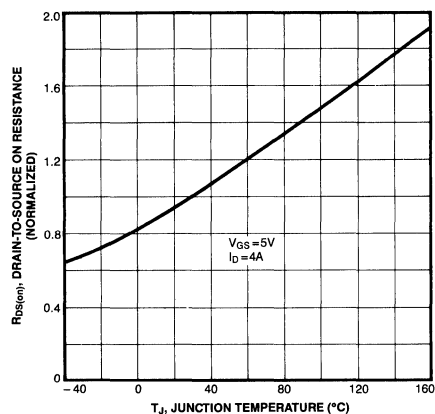


MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE JUNCTION-TO-CASE VS. PULSE DURATION

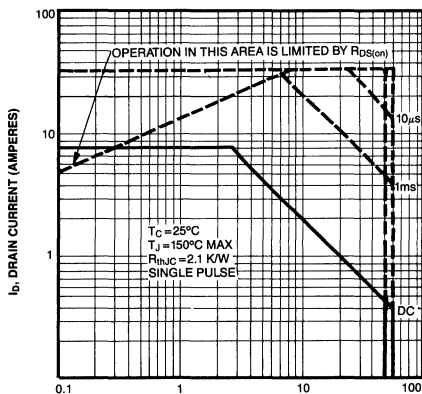




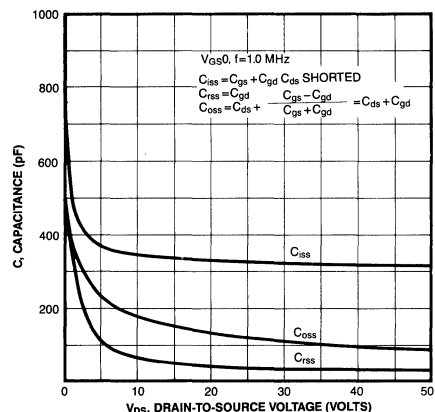
TYPICAL ON-RESISTANCE V_{GS} DRAIN CURRENT



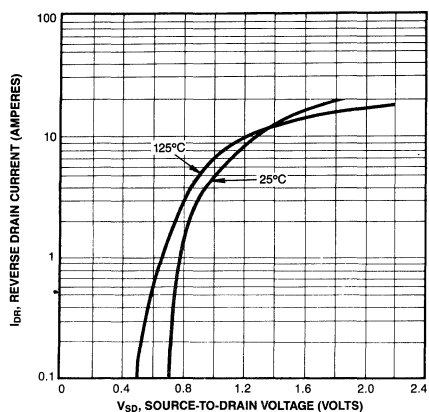
NORMALIZED ON-RESISTANCE V_{GS} TEMPERATURE



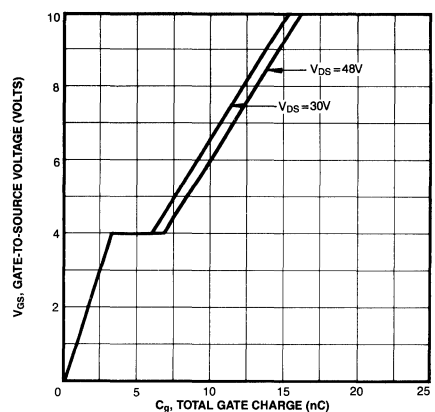
MAXIMUM SAFE OPERATING AREA



TYPICAL CAPACITANCE V_{GS} DRAIN-TO-SOURCE V_{CS} TAG



TYPICAL SOURCE — DRAIN DIODE FORWARD VOLTAGE



TYPICAL GATE CHARGE V_{GS} GATE-TO-SOURCE VOLTAGE

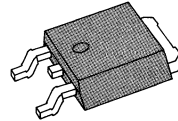
FEATURES

- Lower $R_{DS(on)}$
- Excellent voltage stability
- Fast switching speeds
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability
- D-PAK/I-PAK

PRODUCT SUMMARY

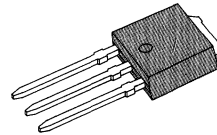
Part Number	V_{DS}	$R_{DS(on)}$	$I_D(on)$
IRLR024/IRLU024	60V	0.15 Ω	14A
IRLR020/IRLU020	50V	0.15 Ω	14A

D-PAK



IRLR020/024

I-PAK



IRLU020/024

MAXIMUM RATINGS

Characteristic	Symbol	IRLR024 IRLU024	IRLR020 IRLU020	Units
Drain-Source Voltage (1)	V_{DSS}	60	50	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$) (1)	V_{DGR}	60	50	Vdc
Gate-Source Voltage	V_{GS}	± 15		Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	14.0	14.0	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	8.7	8.7	Adc
Drain Current—Pulsed (3)	I_{DM}	52	52	Adc
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	42 0.33		Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300		$^\circ C$

Notes: (1) $T_J = 25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse width limited by max. junction temperature

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic		Min	Typ	Max	Units	Test Condition
BV _{DSS}	Drain Source Breakdown Voltage	IRLR014	60	—	—	V	V _{GS} = 0V I _D = 250μA
		IRLU014	60	—	—		
		IRLR020	50	—	—		
		IRLU020	50	—	—		
V _{GS(th)}	Gate Threshold Voltage		1.0	—	2.0	V	V _{DS} = V _{GS} , I _D = 1mA
I _{GSS}	Gate-Source Leakage Forward		—	—	100	nA	V _{GS} = 15V
I _{GSS}	Gate-Source Leakage Reverse		—	—	– 100	nA	V _{GS} = – 15V
I _{DSS}	Zero Gate Voltage Drain Current		—	—	250	μA	V _{DS} = Max. Rating V _{GS} = 0V
			—	—	1.0	mA	V _{DS} = Max. Rating × 0.8, V _{GS} = 0V, T _C = 125°C
I _{D(on)}	On-State Drain-Source Current (2)		14	—	—	A	V _{DS} ≥ I _{D(on)} × R _{DS(on)max} , V _{GS} = 5.0V
R _{DS(on)}	Static Drain-Source On-State Resistance (2)		—	0.10	0.15	Ω	V _{GS} = 5.0V, I _D = 8.0A
g _{fs}	Forward Transconductance (2)		2.0	—	—	S	V _{DS} ≥ 15V, I _D = 8.0A
C _{iss}	Input Capacitance		—	750	—	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0MHz
C _{oss}	Output Capacitance		—	250	—	pF	
C _{rss}	Reverse Transfer Capacitance		—	120	—	pF	
t _{d(on)}	Turn-On Delay Time		—	—	30	ns	V _{DD} = 0.5 BV _{DSS} , I _D = 8.0A, Z _O = 50Ω (MOSFET switching times are essentially independent of operating temperature)
t _r	Rise Time		—	—	90	ns	
t _{d(off)}	Turn-Off Delay Time		—	—	40	ns	
t _f	Fall Time		—	—	30	ns	
Q _g	Total Gate Charge		—	—	38	nC	V _{GS} = 5V, I _D = 14A, V _{DS} = 0.8 Max. Rating (Gate charge is essentially independent of operating temperature)
Q _{gs}	Gate-Source Charge		—	25	—	nC	
Q _{gd}	Gate-Drain Charge		—	5.0	—	nC	

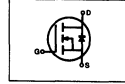
THERMAL RESISTANCE

R _{thJC}	Junction-to-Case	—	—	3.0	K/W	
R _{thCS}	Case-to-Sink	—	1.7	—	K/W	Mounting surface flat, smooth, and greased
R _{thJA}	Junction-to-Ambient	—	—	110	K/W	Free Air Operation

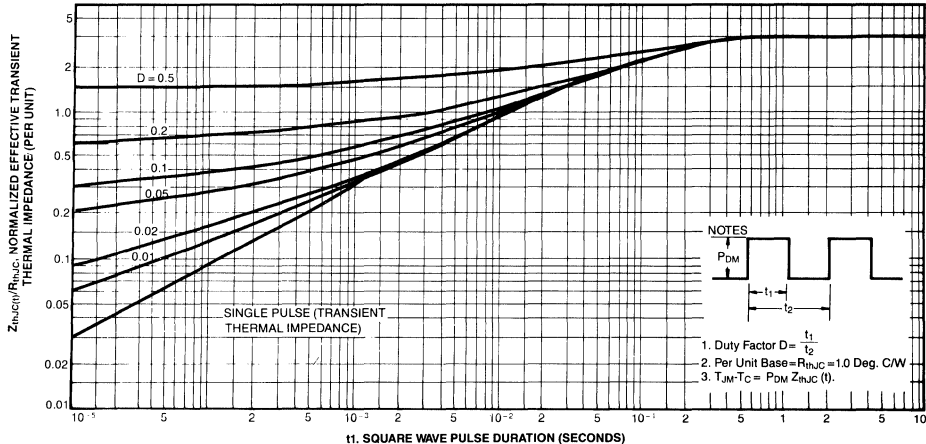
Notes: (1) T_J = 25°C to 150°C
(2) Pulse test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
(3) Repetitive rating: Pulse width limited by max. junction temperature

SOURCE-DRAIN DIODE RATING AND CHARACTERISTICS

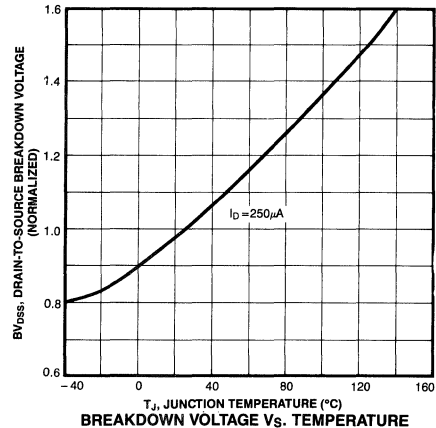
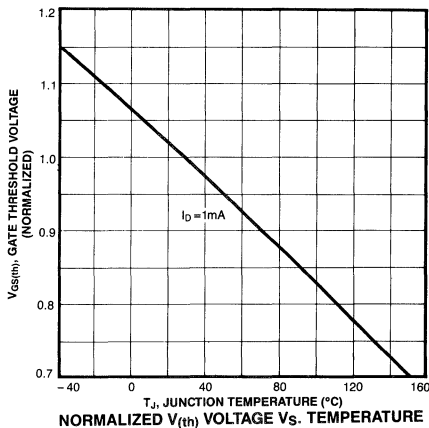
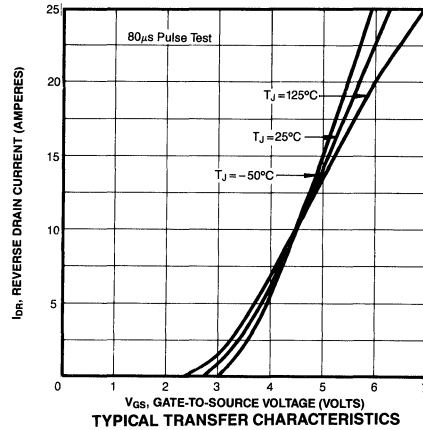
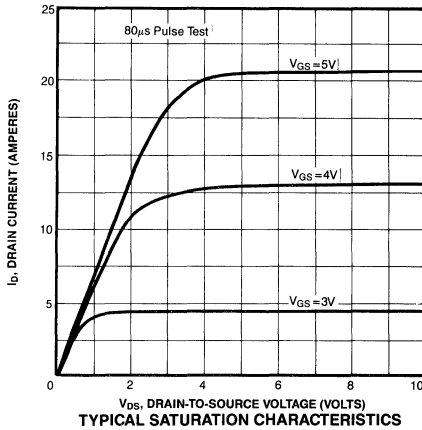
Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
I_S	Continuous Source Current (Body Diode)	—	—	14	A	Modified MOSFET showing the symbol integral reverse P-N junction rectifier
I_{SM}	Pulse Source Current (Body Diode) (3)	—	—	52	A	
V_{SD}	Diode Forward Voltage (2)	—	—	1.4	V	$T_C = 25^\circ\text{C}$, $I_S = 14\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	—	300	ns	$T_J = 25^\circ\text{C}$, $I_F = 14\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$

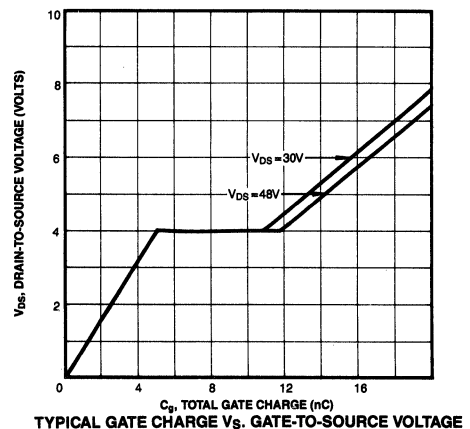
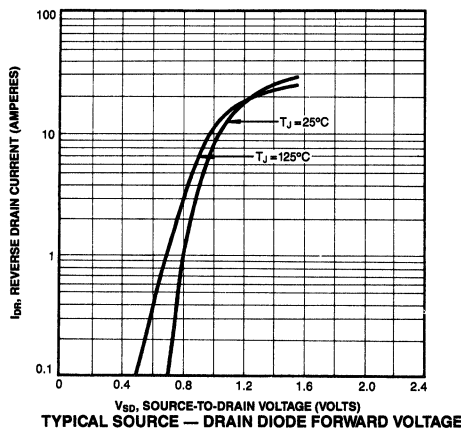
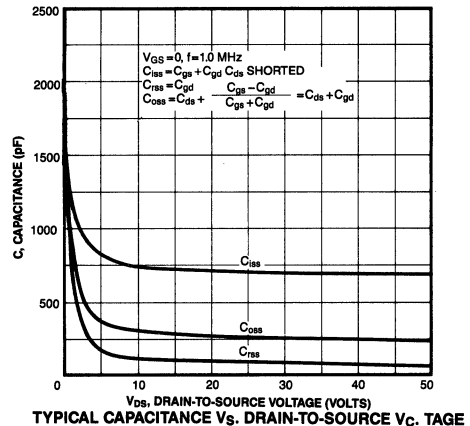
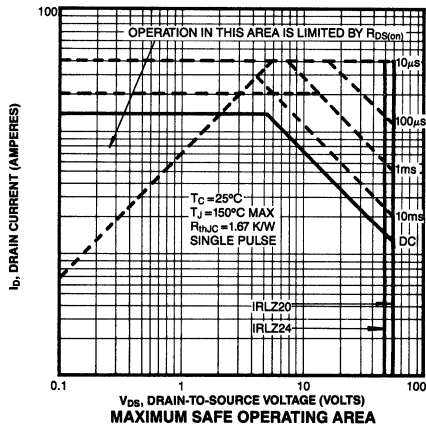
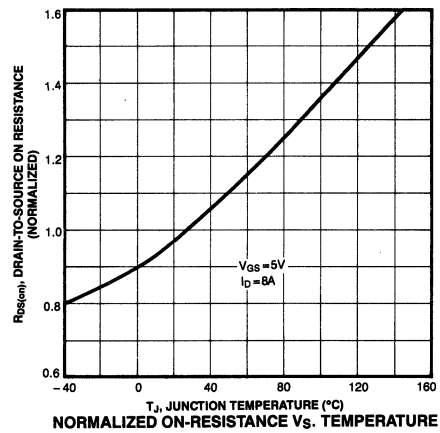
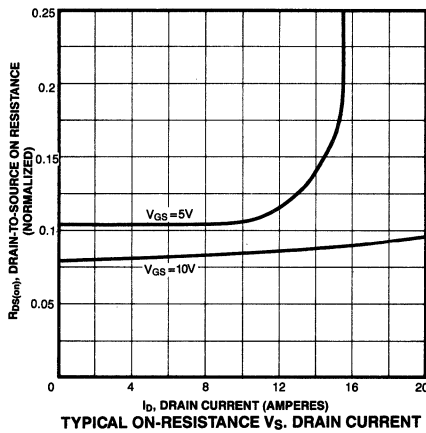


- Notes:** (1) $T_J = 25^\circ\text{C}$ to 150°C
(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse width limited by max. junction temperature



MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE JUNCTION-TO-CASE VS. PULSE DURATION





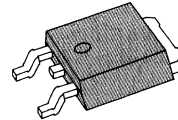
FEATURES

- Lower $R_{DS(on)}$
- Excellent voltage stability
- Fast switching speeds
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability
- D-PAK/I-PAK

PRODUCT SUMMARY

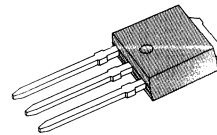
Part Number	V_{DS}	$R_{DS(on)}$	$I_{D(on)}$
IRLR110/IRLU110	100V	0.75 Ω	4.0A
IRLR111/IRLU111	80V	0.75 Ω	4.0A

D-PAK



IRLR110/111

I-PAK



IRLU110/111

MAXIMUM RATINGS

Characteristic	Symbol	IRLR110/IRLU110	IRLR111/IRLU111	Units
Drain-Source Voltage (1)	V_{DSS}	100	80	Vdc
Drain-Gate Voltage ($R_{GS} = 1.0M\Omega$) (1)	V_{DGR}	100	80	Vdc
Gate-Source Voltage	V_{GS}	± 15		Vdc
Continuous Drain Current $T_C = 25^\circ C$	I_D	4.0	4.0	Adc
Continuous Drain Current $T_C = 100^\circ C$	I_D	2.8	2.8	Adc
Drain Current—Pulsed (3)	I_{DM}	16	16	Adc
Total Power Dissipation @ $T_C = 25^\circ C$ Derate above $25^\circ C$	P_D	30 0.24		Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	- 55 to 150		$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300		$^\circ C$

Notes: (1) $T_J = 25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse width limited by max. junction temperature

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
BV_{DSS}	Drain Source Breakdown Voltage	IRLR110 IRLU110 IRLR111 IRLU111	100	—	—	$V_{GS} = 0V$ $I_D = 250\mu A$
		80	—	—	—	
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	$V_{DS} = V_{GS}$, $I_D = 1mA$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS} = 15V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	$V_{GS} = -15V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0V$
		—	—	1.0	mA	$V_{DS} = \text{Max. Rating} \times 0.8$, $V_{GS} = 0V$, $T_C = 125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2)	4.0	—	—	A	$V_{DS} \geq I_{D(on)} \times R_{DS(on)max.}$, $V_{GS} = 5.0V$
$R_{DS(on)}$	Static Drain-Source On-State Resistance (2)	—	—	0.75	Ω	$V_{GS} = 5.0V$, $I_D = 2.0A$
g_{fs}	Forward Transconductance (2)	1.3	—	—	S	$V_{DS} \geq 25V$, $I_D = 2.0A$
C_{iss}	Input Capacitance	—	240	—	pF	$V_{GS} = 0V$, $V_{DS} = 25V$, $f = 1.0MHz$
C_{oss}	Output Capacitance	—	70	—	pF	
C_{rss}	Reverse Transfer Capacitance	—	40	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	8.0	20	ns	$V_{DD} = 0.5BV_{DSS}$, $I_D = 4.0A$, $Z_O = 15\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	8.0	25	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	10	25	ns	
t_f	Fall Time	—	8.0	20	ns	
Q_g	Total Gate Charge	—	—	7.5	nC	$V_{GS} = 5V$, $I_D = 4.0A$, $V_{DS} = 0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature)
Q_{gs}	Gate-Source Charge	—	1.9	—	nC	
Q_{gd}	Gate-Drain Charge	—	3.8	—	nC	

THERMAL RESISTANCE

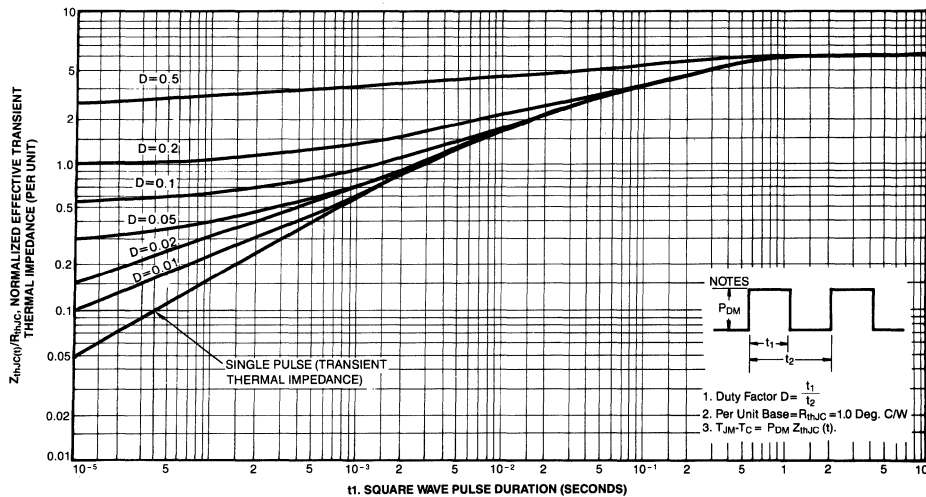
R_{thJC}	Junction-to-Case	—	—	4.2	K/W	
R_{thCS}	Case-to-Sink	—	1.7	—	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	—	—	110	K/W	Free Air Operation

- Notes:** (1) $T_J = 25^\circ\text{C}$ to 150°C
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse width limited by max. junction temperature

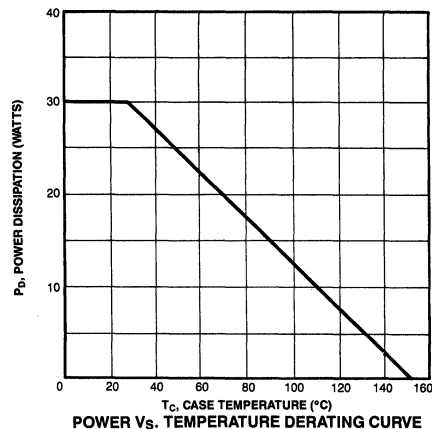
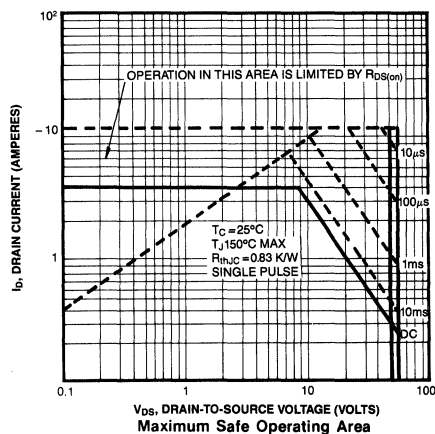
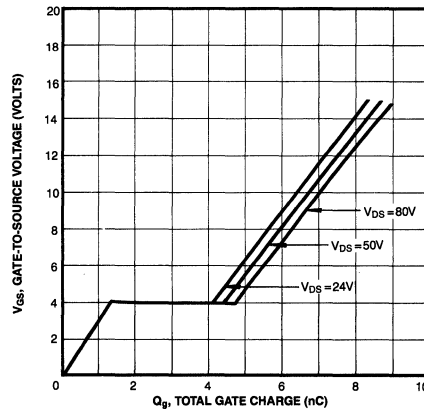
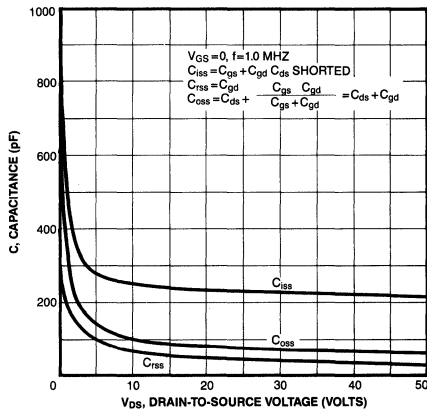
SOURCE-DRAIN DIODE RATING AND CHARACTERISTICS

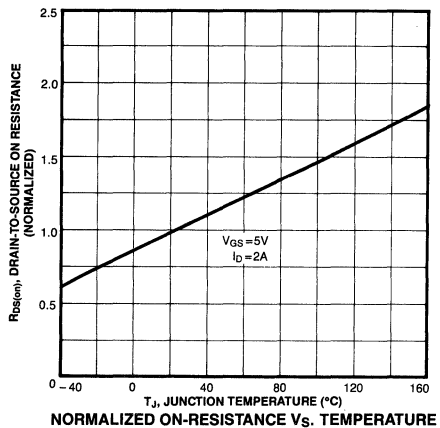
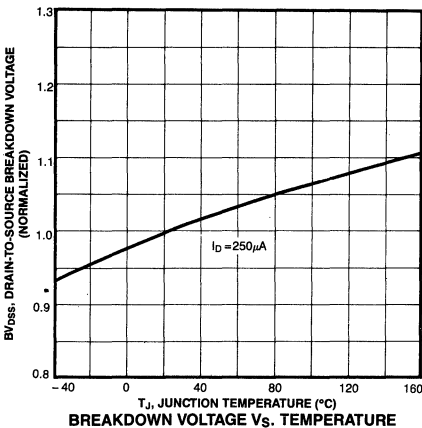
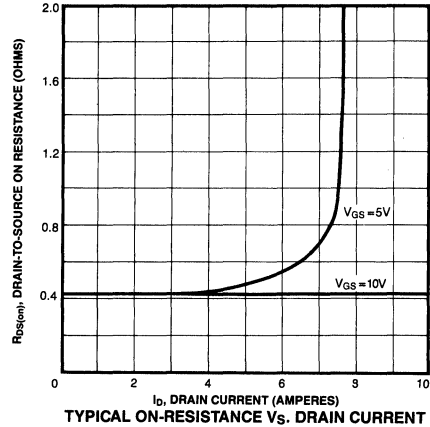
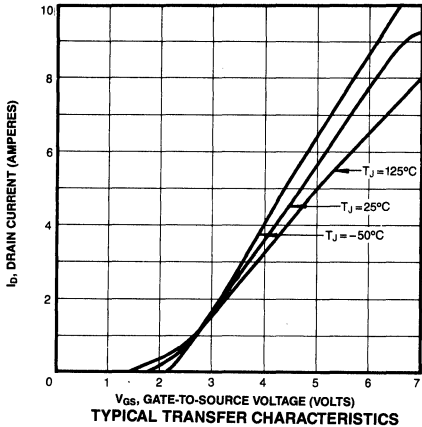
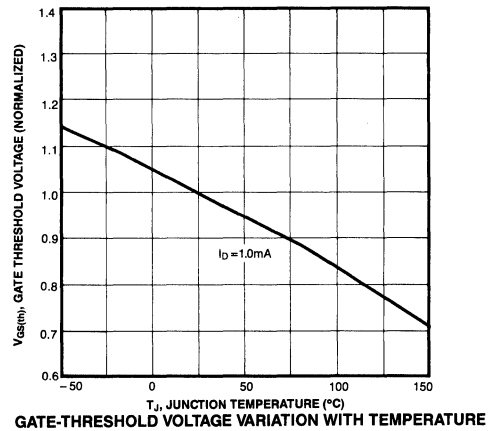
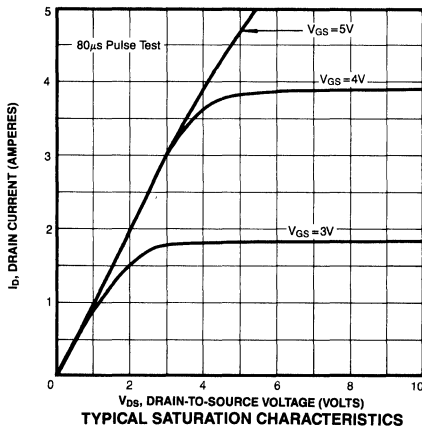
Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
I_S	Continuous Source Current (Body Diode)	—	—	4.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier
I_{SM}	Pulse-Source Current (Body Diode) (3)	—	—	16	A	
V_{SD}	Diode Forward Voltage (2)	—	—	2.5	V	$T_C = 25^\circ\text{C}$, $I_S = 4.0\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	230	—	ns	$T_J = 25^\circ\text{C}$, $I_F = 4.0\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$

Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C
(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse width limited by max. junction temperature



MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE JUNCTION-TO-CASE V_S PULSE DURATION





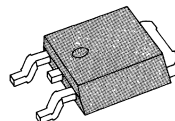
FEATURES

- Lower $R_{DS(on)}$
- Excellent voltage stability
- Fast switching speeds
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability
- D-PAK/I-PAK

PRODUCT SUMMARY

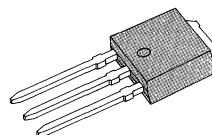
Part Number	V_{DS}	$R_{DS(on)}$	$I_{D(on)}$
IRLR120	100V	0.4 Ω	7.9A
IRLR121	80V	0.4 Ω	7.9A
IRLU120	100V	0.4 Ω	7.9A
IRLU121	80V	0.4 Ω	7.9A

D-PAK



IRLR120/121

I-PAK



IRLU120/121

MAXIMUM RATINGS

Characteristics	Symbol	IRLR120/U120	IRLR121/U121	Units
Drain-Source Voltage (1)	V_{DSS}	100	80	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\Omega$) (1)	V_{DGR}	100	80	Vdc
Gate-Source Voltage	V_{GS}	± 15		Vdc
Continuous Drain Current $T_C=25^\circ C$	I_D	7.9	7.9	Adc
Continuous Drain Current $T_C=100^\circ C$	I_D	5.1	5.1	Adc
Drain Current—Pulsed (3)	I_{DM}	32	32	Adc
Total Power Dissipation @ $T_C=25^\circ C$ Derate above $25^\circ C$	P_D	42 0.33		Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	- 55 to 150		$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300		$^\circ C$

Notes: (1) $T_J = 25^\circ C$ to $150^\circ C$
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse width limited by max. junction temperature

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic		Min	Typ	Max	Units	Test Condition
BV_{DSS}	Drain Source Breakdown Voltage	IRLR120	100	—	—	V	$V_{GS} = 0V$ $I_D = 250\mu A$
		IRLU120 IRLR121 IRLR121	80	—	—		
$V_{GS(th)}$	Gate Threshold Voltage		1.0	—	2.0	V	$V_{DS} = V_{GS}$, $I_D = 1mA$
I_{GSS}	Gate-Source Leakage Forward		—	—	100	nA	$V_{GS} = 15V$
I_{GSS}	Gate-Source Leakage Reverse		—	—	- 100	nA	$V_{GS} = -15V$
I_{DSS}	Zero Gate Voltage Drain Current		—	—	250	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0V$
			—	—	1.0	mA	$V_{DS} = \text{Max. Rating} \times 0.8$, $V_{GS} = 0V$, $T_C = 125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2)		7.9	—	—	A	$V_{DS} \geq I_{D(on)} \times R_{DS(on)max}$, $V_{GS} = 5.0V$
$R_{DS(on)}$	Static Drain-Source On-State Resistance (2)		—	—	0.4	Ω	$V_{GS} = 5.0V$, $I_D = 4.0A$
g_{fs}	Forward Transconductance (2)		3.0	—	—	S	$V_{DS} \geq 25V$, $I_D = 4.0A$
C_{iss}	Input Capacitance		—	450	—	pF	$V_{GS} = 0V$, $V_{DS} = 25V$, $f = 1.0MHz$
C_{oss}	Output Capacitance		—	120	—	pF	
C_{rss}	Reverse Transfer Capacitance		—	60	—	pF	
$t_{d(on)}$	Turn-On Delay Time		—	—	15	ns	$V_{DD} = 0.5BV_{DSS}$, $I_D = 4.0A$, $Z_O = 50\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_2	Rise Time		—	—	27	ns	
$t_{d(off)}$	Turn-Off Delay Time		—	—	45	ns	
t_f	Fall Time		—	—	30	ns	
Q_g	Total Gate Charge		—	9.8	15	nC	$V_{GS} = 5V$, $I_D = 8.0A$, $V_{DS} = 0.8$ Max. Rating (Gate charge is essentially independent of operating temperature)
Q_{gs}	Gate-Source Charge		—	3.5	—	nC	
Q_{gd}	Gate-Drain Charge		—	6.3	—	nC	

THERMAL RESISTANCE

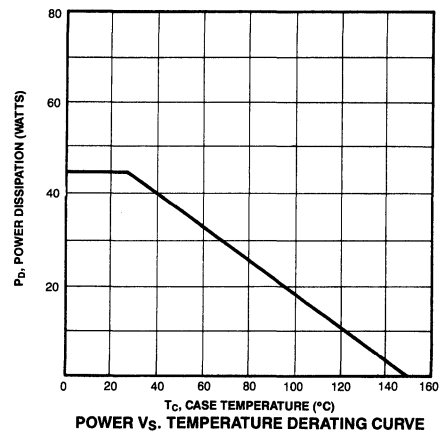
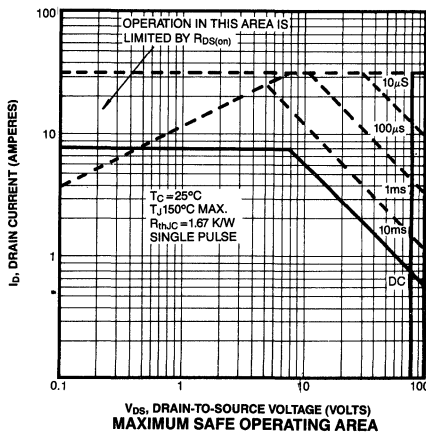
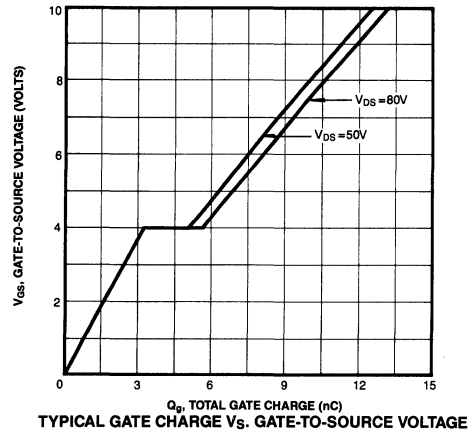
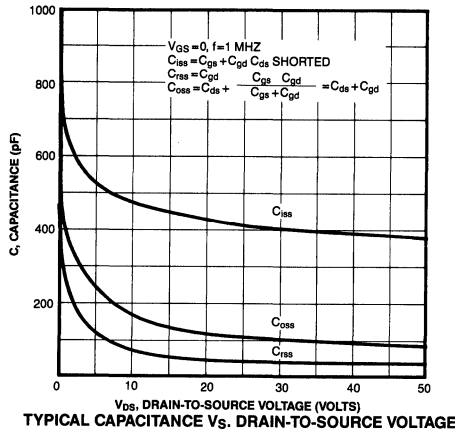
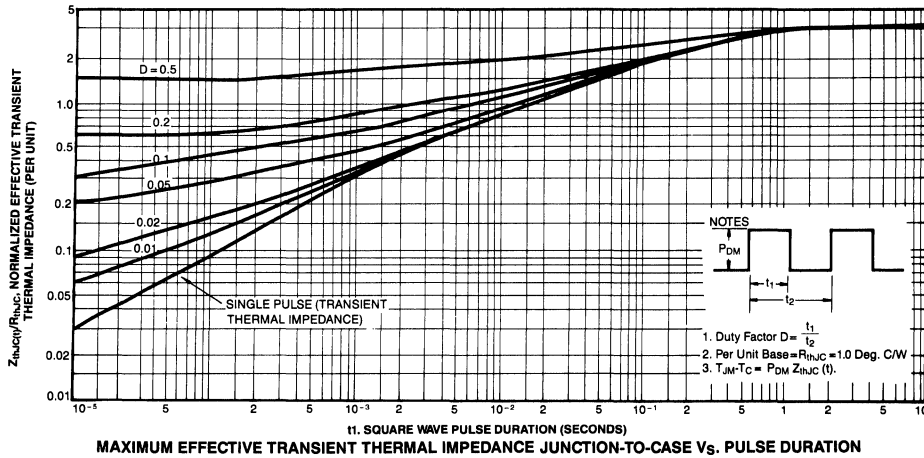
R_{thJC}	Junction-to-Case	—	—	3.0	K/W	
R_{thCS}	Case-to-Sink	—	1.7	—	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	—	—	110	K/W	Free Air Operation

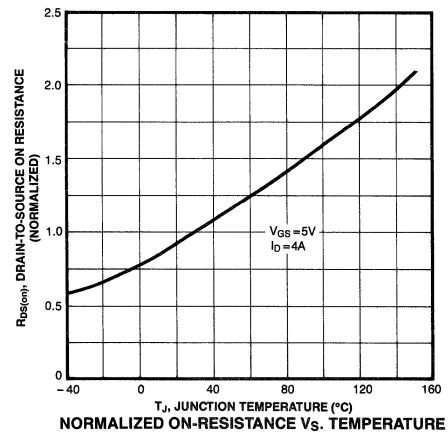
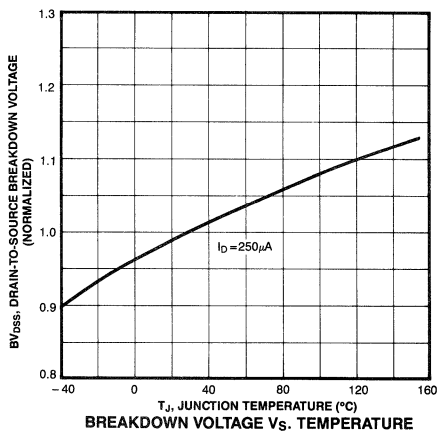
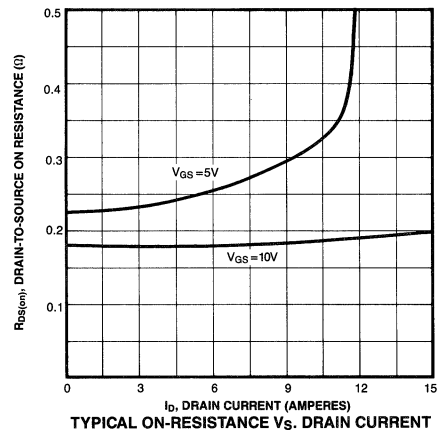
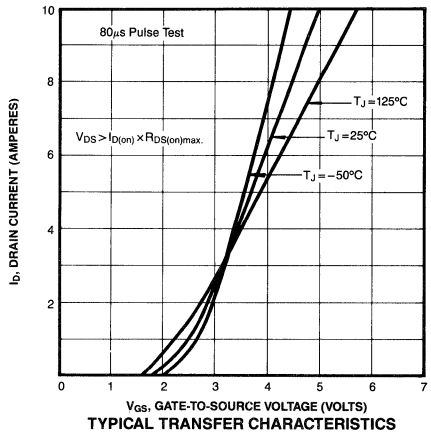
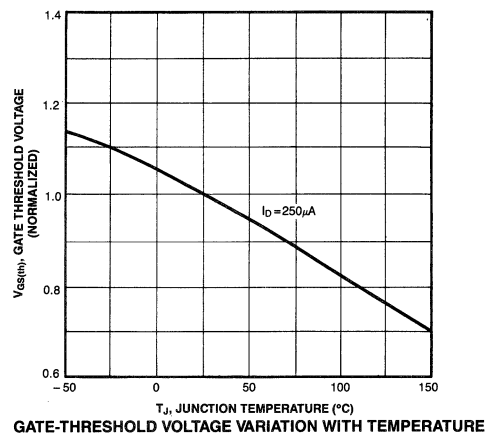
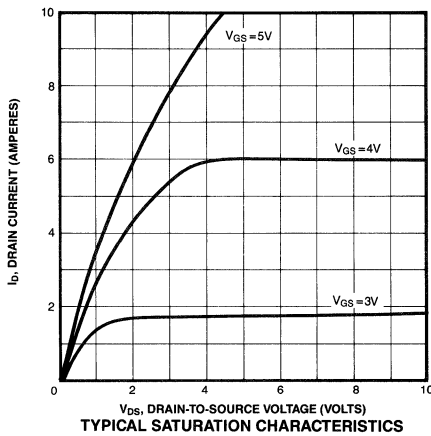
- Notes:** (1) $T_J = 25^\circ\text{C}$ to 150°C
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse width limited by max. junction temperature

SOURCE-DRAIN DIODE RATING AND CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
I_S	Continuous Source Current (Body Diode)	—	—	7.9	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier
I_{SM}	Pulse-Source Current (Body Diode) (3)	—	—	32	A	
V_{SD}	Diode Forward Voltage (2)	—	—	2.5	V	$T_C = 25^\circ\text{C}$, $I_S = 7.9\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	280	—	ns	$T_J = 25^\circ\text{C}$, $I_F = 7.9\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$

Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C
(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse width limited by max. junction temperature





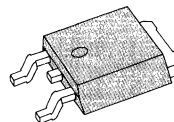
FEATURES

- Lower $R_{DS(on)}$
- Excellent voltage stability
- Fast switching speeds
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability
- D-PAK/I-PAK

PRODUCT SUMMARY

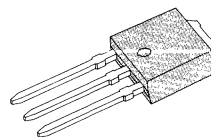
Part Number	V_{DS}	$R_{DS(on)}$	$I_{D(on)}$
IRLR210	200V	2.4Ω	2.0A
IRLR211	150V	2.4Ω	2.0A
IRLU210	200V	2.4Ω	2.0A
IRLU211	150V	2.4Ω	2.0A

D-PAK



IRLR210/211

I-PAK



IRLU210/211

2

MAXIMUM RATINGS

Characteristic	Symbol	IRLR210/U210	IRLR211/U211	Units
Drain-Source Voltage (1)	V_{DSS}	200	150	Vdc
Drain-Gate Voltage ($R_{GS} = 1.0M\Omega$) (1)	V_{DGR}	200	150	Vdc
Gate-Source Voltage	V_{GS}	± 15		Vdc
Continuous Drain Current $T_C = 25^\circ C$	I_D	2.0	2.0	Adc
Continuous Drain Current $T_C = 100^\circ C$	I_D	1.2	1.2	Adc
Drain Current—Pulsed (3)	I_{DM}	8.0	8.0	Adc
Total Power Dissipation @ $T_C = 25^\circ C$ Derate above $25^\circ C$	P_D	25 0.2		Watts W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	- 55 to 150		$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300		$^\circ C$

Notes: (1) $T_J = 25^\circ C$ to $150^\circ C$
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse width limited by max. junction temperature

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
BV_{DSS}	Drain Source Breakdown Voltage	IRLR210 IRLU210 IRLR211 IRLR211	200	—	—	V $V_{GS} = 0V$ $I_D = 250\mu A$
			150	—	—	
V_{th}	Gate Threshold Voltage	1.0	—	2.0	V	$V_{DS} = V_{GS}$, $I_D = 1mA$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS} = 15V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	-100	nA	$V_{GS} = -15V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0V$
		—	—	1.0	mA	$V_{DS} = \text{Max. Rating} \times 0.8$, $V_{GS} = 0V$, $T_C = 125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2)	2.0	—	—	A	$V_{DS} \geq I_{D(on)} \times R_{DS(on)max.}$, $V_{GS} = 5.0V$
$R_{DS(on)}$	Static Drain-Source On-State Resistance (2)	—	—	2.40	Ω	$V_{GS} = 5.0V$, $I_D = 1.0A$
g_{fs}	Forward Transconductance (2)	0.8	—	—	$ g $	$V_{DS} \geq 50V$, $I_D = 1.0A$
C_{iss}	Input Capacitance	—	220	—	pF	$V_{GS} = 0V$, $V_{DS} = 25V$, $f = 1.0MHz$
C_{oss}	Output Capacitance	—	45	—	pF	
C_{rss}	Reverse Transfer Capacitance	—	23	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	8.0	15	ns	$V_{DD} = 0.5BV_{DSS}$, $I_D = 2.0A$, $Z_O = 15\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	8.0	25	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	10	15	ns	
t_f	Fall Time	—	8.0	15	ns	
Q_g	Total Gate Charge	—	—	7.5	nC	$V_{GS} = 5V$, $I_D = 2.0A$, $V_{DS} = 0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature)
Q_{gs}	Gate-Source Charge	—	1.9	—	nC	
Q_{gd}	Gate-Drain Charge	—	3.9	—	nC	

THERMAL RESISTANCE

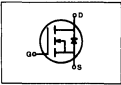
R_{thJC}	Junction-to-Case	—	—	5.0	K/W	
R_{thCS}	Case-to-Sink	—	1.7	—	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	—	—	110	K/W	Free Air Operation

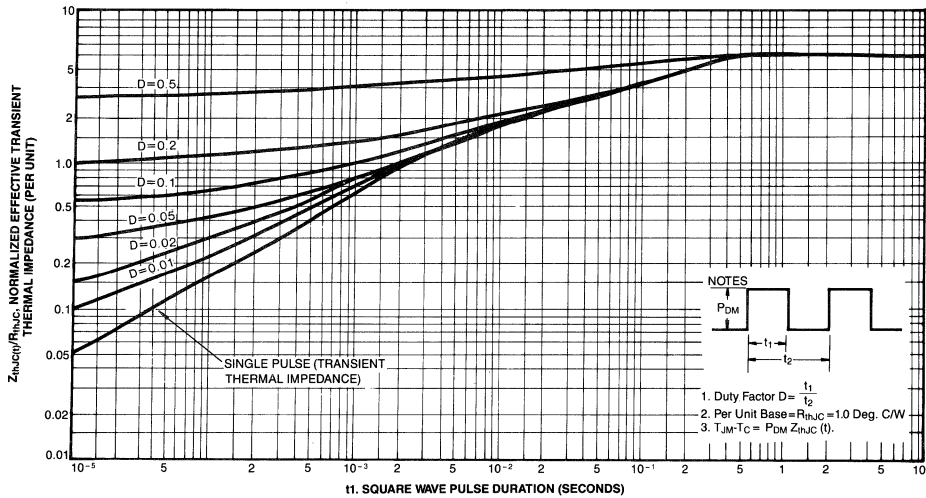
Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse width limited by max. junction temperature

SOURCE-DRAIN DIODE RATING AND CHARACTERISTICS

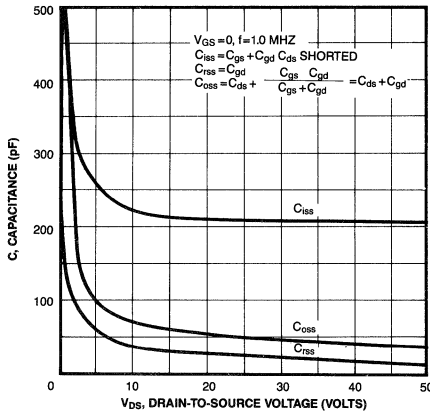
Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
I_S	Continuous Source Current (Body Diode)	—	—	2.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier
I_{SM}	Pulse-Source Current (Body Diode) (3)	—	—	8.0	A	
V_{SD}	Diode Forward Voltage (2)	—	—	1.8	V	$T_C = 25^{\circ}\text{C}$, $I_S = 2.0\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	150	—	ns	$T_J = 25^{\circ}\text{C}$, $I_F = 2.0\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$

Notes: (1) $T_J = 25^{\circ}\text{C}$ to 150°C
(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse width limited by max. junction temperature

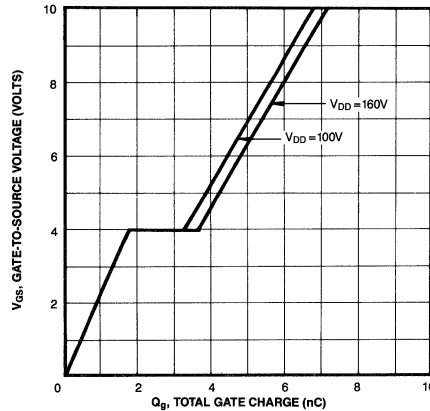




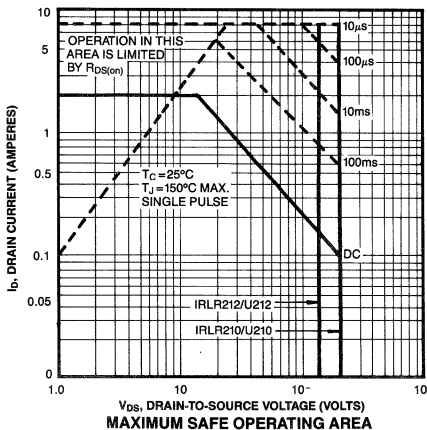
MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE JUNCTION-TO-CASE V_S , PULSE DURATION



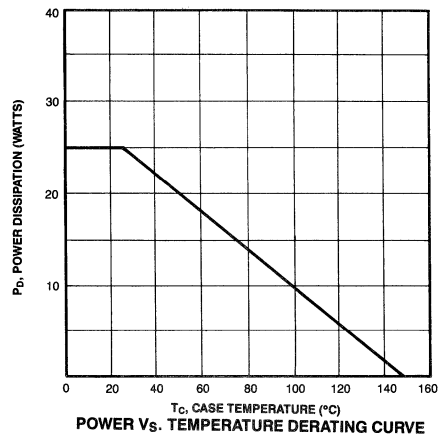
TYPICAL CAPACITANCE V_S , DRAIN-TO-SOURCE VOLTAGE

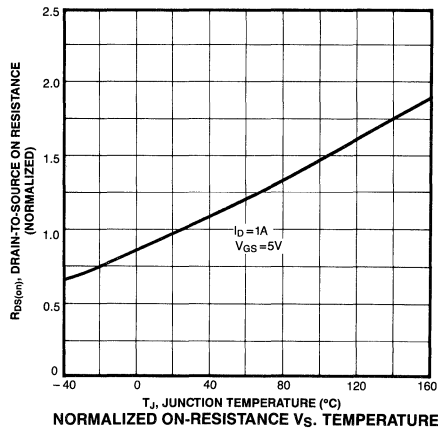
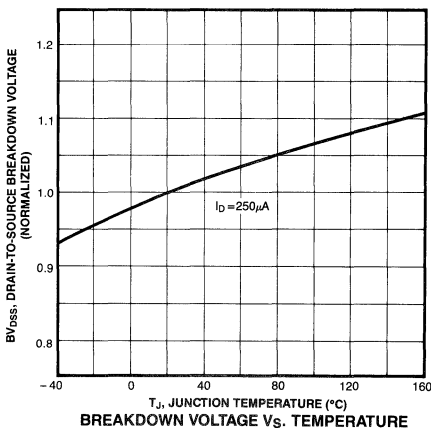
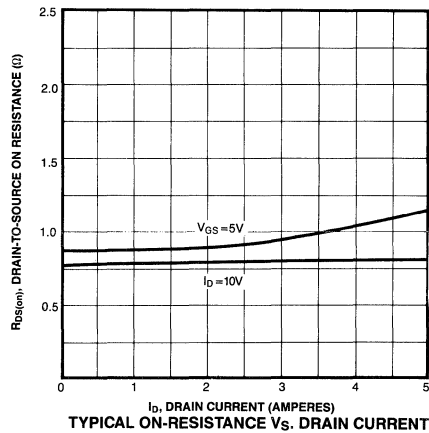
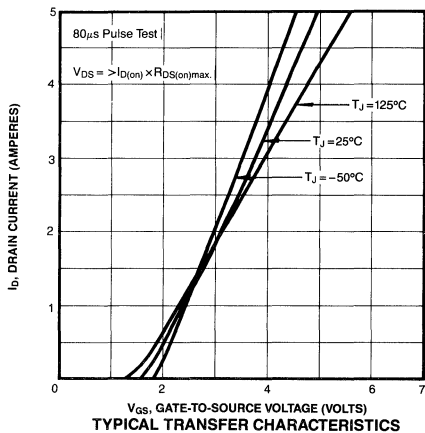
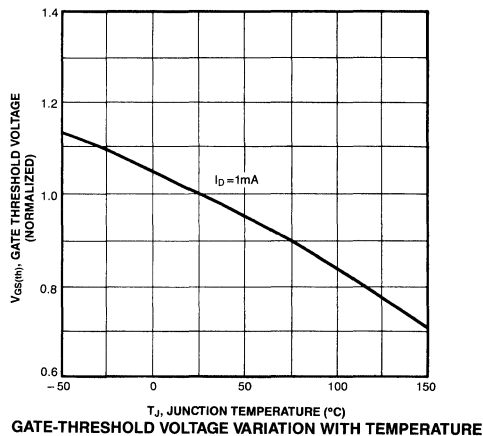
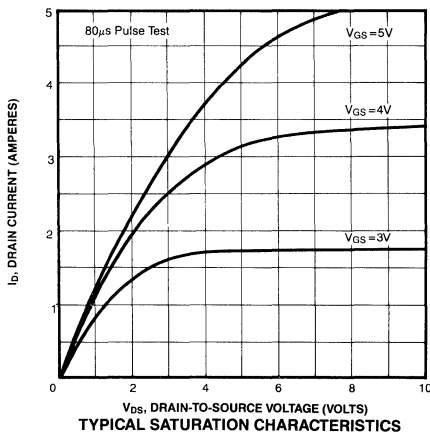


TYPICAL GATE CHARGE V_S , GATE-TO-SOURCE VOLTAGE



MAXIMUM SAFE OPERATING AREA





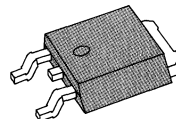
FEATURES

- Lower $R_{DS(on)}$
- Excellent voltage stability
- Fast switching speeds
- Lower input capacitance
- Rugged polysilicon gate cell structure
- Extended safe operating area
- Improved high temperature reliability
- D-PAK/I-PAK

PRODUCT SUMMARY

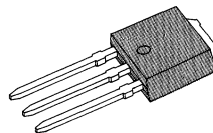
Part Number	V_{DS}	$R_{DS(on)}$	$I_{D(on)}$
IRLR220/IRLU220	200V	1.2 Ω	4.0A
IRLU221/IRLU221	150V	1.2 Ω	4.0A

D-PAK



IRLR220/221

I-PAK



IRLU220/221

MAXIMUM RATINGS

Characteristic	Symbol	IRLR220/U220	IRLR221/U221	Units
Drain-Source Voltage (1)	V_{DSS}	200	150	Vdc
Drain-Gate Voltage ($R_{GS} = 1.0M \Omega$) (1)	V_{DGR}	200	150	Vdc
Gate-Source Voltage	V_{GS}	± 15		Vdc
Continuous Drain Current $T_C = 25^\circ C$	I_D	4.0	4.0	Adc
Continuous Drain Current $T_C = 100^\circ C$	I_D	2.6	2.6	Adc
Drain Current—Pulsed (3)	I_{DM}	16	16	Adc
Total Power Dissipation @ $T_C = 25^\circ C$ Derate above $25^\circ C$	P_D	42 0.33		Watts W/ $^\circ C$
Operation and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300		$^\circ C$

Notes: (1) $T_J = 25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse width limited by max. junction temperature

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

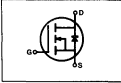
Symbol	Characteristic		Min	Typ	Max	Units	Test Condition
BV _{DSS}	Drain Source Breakdown Voltage	IRLR220	200	—	—	V	V _{GS} = 0V I _D = 250 μ A
		IRLU220 IRLR221 IRLU221	150	—	—		
V _{GS(th)}	Gate Threshold Voltage		1.0	—	2.0	V	V _{DS} = V _{GS} , I _D = 1mA
I _{GSS}	Gate-Source Leakage Forward		—	—	100	nA	V _{GS} = 15V
I _{GSS}	Gate-Source Leakage Reverse		—	—	- 100	nA	V _{GS} = - 15V
I _{DSS}	Zero Gate Voltage Drain Current		—	—	250	μ A	V _{DS} = Max. Rating, V _{GS} = 0V
			—	—	1.0	mA	V _{DS} = Max. Rating $\times$ 0.8, V _{GS} = 0V, T _C = 125°C
I _{D(on)}	On-State Drain-Source Current (2)		4.0	—	—	A	V _{DS} $\geq$ I _{D(on)} $\times$ R _{DS(on)max} , V _{GS} = 5.0V
R _{DS(on)}	Static Drain Source On State Resistance (2)		—	—	1.2	Ω	V _{GS} = 5.0V, I _D = 2.0A
g _{fs}	Forward Transconductance (2)		3.0	—	—	S	V _{DS} $\geq$ 25V, I _D = 2.0A
C _{iss}	Input Capacitance		—	450	—	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0MHz
C _{oss}	Output Capacitance		—	140	—	pF	
C _{rss}	Reverse Transfer Capacitance		—	60	—	pF	
t _{d(on)}	Turn-On Delay Time		—	—	40	ns	V _{DD} = 0.5BV _{DSS} , I _D = 2.0A, Z _O = 50 Ω (MOSFET switching times are essentially independent of operating temperature)
t _r	Rise Time		—	—	60	ns	
t _{d(off)}	Turn-Off Delay Time		—	—	100	ns	
t _f	Fall Time		—	—	15	ns	V _{GS} = 5V, I _D = 4.0A, V _{DS} = 0.8 Max. Rating (Gate charge is essentially independent of operating temperature)
Q _g	Total Gate Charge		—	—	2.0	nC	
Q _{gs}	Gate-Source Charge		—	8.5	—	nC	
Q _{gd}	Gate-Drain Charge		—	6.3	—	nC	

THERMAL RESISTANCE

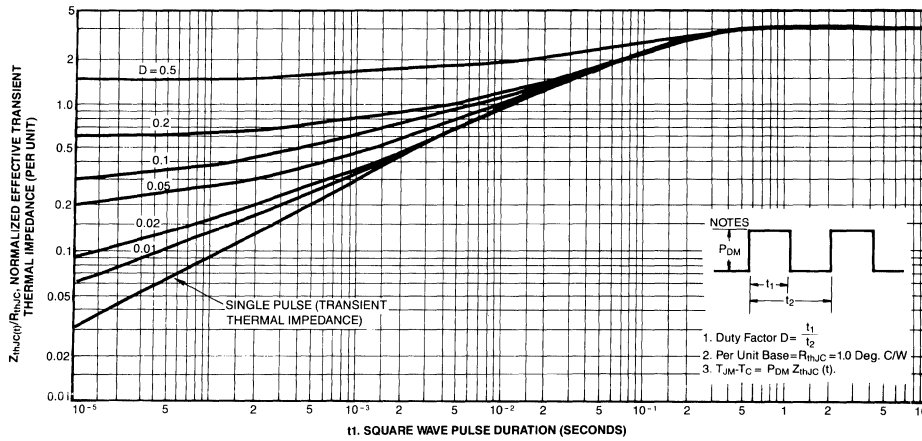
R _{thJC}	Junction-to-Case	—	—	3.0	K/W	
R _{thCS}	Case-to-Sink	—	1.7	—	K/W	Mounting surface flat, smooth, and greased
R _{thJA}	Junction-to-Ambient	—	—	110	K/W	Free Air Operation

Notes: (1) T_J = 25°C to 150°C
(2) Pulse test: Pulse width $\leq$ 300 μ s, Duty Cycle $\leq$ 2%
(3) Repetitive rating: Pulse width limited by max. junction temperature

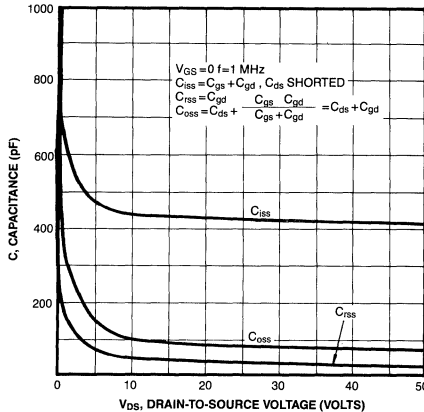
SOURCE-DRAIN DIODE RATING AND CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
I_S	Continuous Source Current (Body Diode)	—	—	4.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier 
I_{SM}	Pulse Source Current (Body Diode) (3)	—	—	16	A	
V_{SD}	Diode Forward Voltage (2)	—	—	1.8	V	$T_C = 25^\circ\text{C}$, $I_S = 4.0\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	400	—	ns	$T_J = 25^\circ\text{C}$, $I_F = 4.0\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$

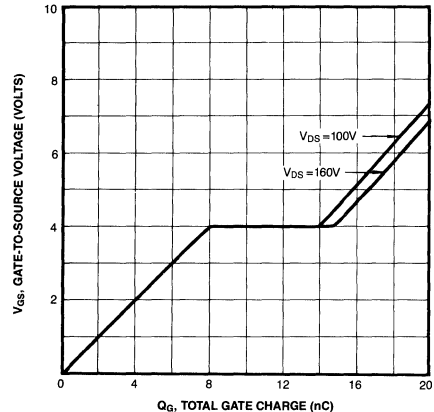
Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C
(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse width limited by max. junction temperature



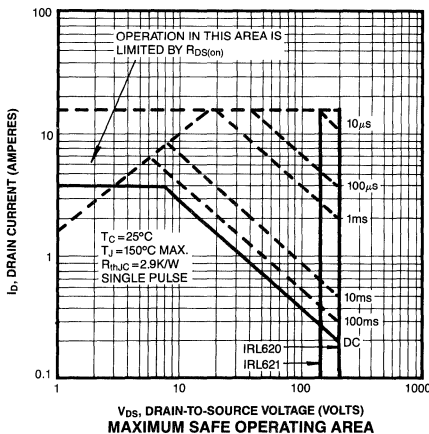
MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE JUNCTION-TO-CASE V_S , PULSE DURATION



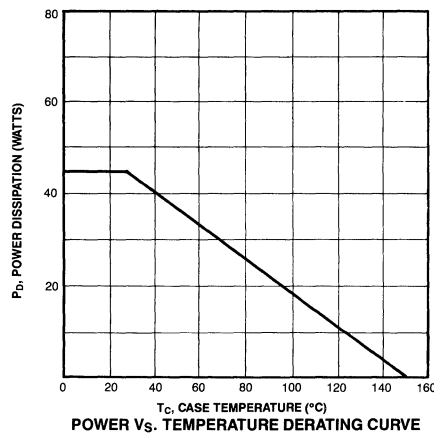
TYPICAL CAPACITANCE V_S , DRAIN-TO-SOURCE VOLTAGE



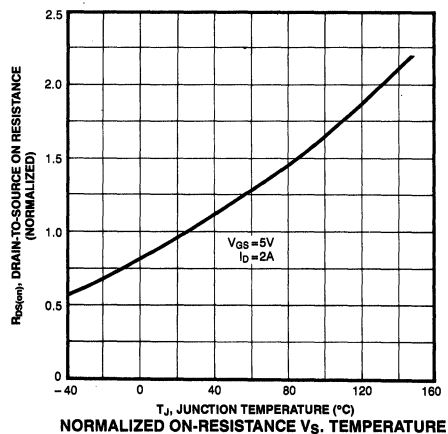
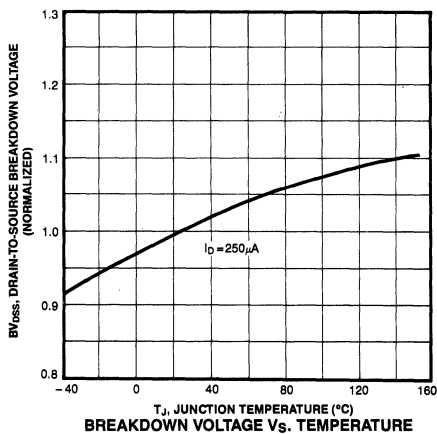
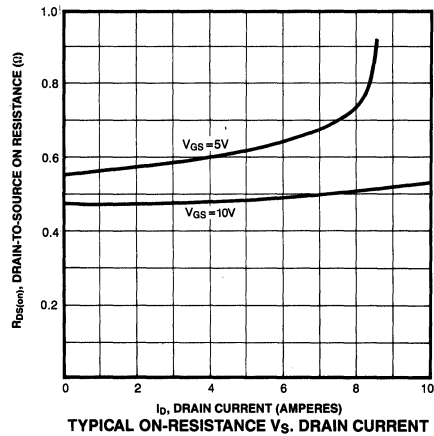
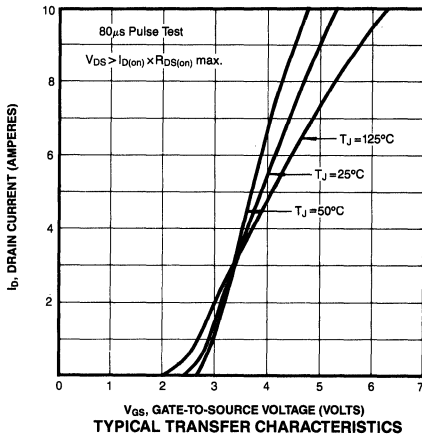
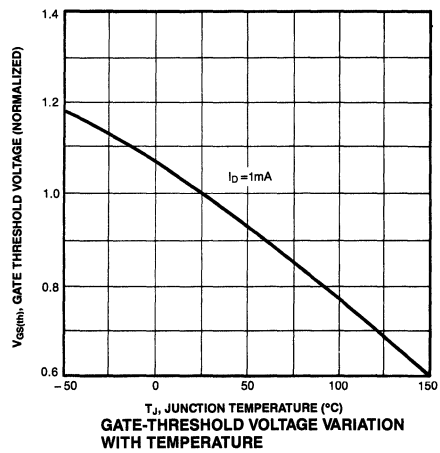
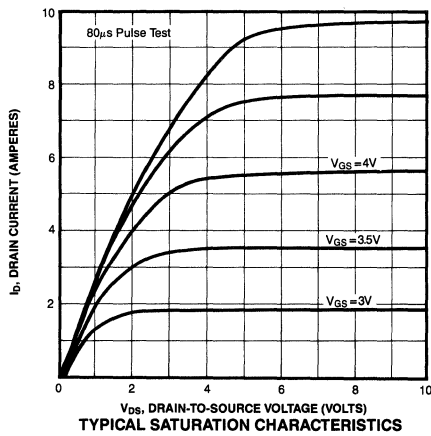
TYPICAL GATE CHARGE V_S , GATE-TO-SOURCE VOLTAGE



MAXIMUM SAFE OPERATING AREA



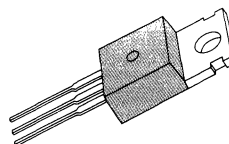
POWER V_S , TEMPERATURE DERATING CURVE



FEATURES

- Lower $R_{DS(on)}$
- Excellent voltage stability
- Fast switching speeds
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability
- TO-220 Package

TO-220



1. Gate 2. Drain 3. Source

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	$I_{D(on)}$
IRLZ14	60V	0.30 Ω	6.7A
IRLZ10	50V	0.30 Ω	6.7A

MAXIMUM RATINGS

Characteristic	Symbol	IRLZ14	IRLZ10	Units
Drain-Source Voltage (1)	V_{DSS}	60	50	Vdc
Drain-Gate Voltage ($R_{GS} = 1.0M \Omega$) (1)	V_{DGR}	60	50	Vdc
Gate-Source Voltage	V_{GS}	± 15		Vdc
Continuous Drain Current $T_C = 25^\circ C$	I_D	6.7	6.7	Adc
Continuous Drain Current $T_C = 100^\circ C$	I_D	4.2	4.2	Adc
Drain Current—Pulsed (3)	I_{DM}	27	27	Adc
Total Power Dissipation @ $T_C = 25^\circ C$ Derate above $25^\circ C$	P_D	30 0.20		Watts W/ $^\circ C$
Operation and Storage Junction Temperature Range	T_J, T_{stg}	- 55 to 175		$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300		$^\circ C$

Notes: (1) $T_J = 25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse width limited by max. junction temperature

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic		Min	Typ	Max	Units	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage	IRLZ14 IRLZ10	60 50	— —	— —	V	$V_{GS} = 0V$ $I_D = 250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage		1.0	—	2.0	V	$V_{DS} = V_{GS}$, $I_D = 1.0mA$
I_{GSS}	Gate-Source Leakage Forward		—	—	100	nA	$V_{GS} = 15V$
I_{GSS}	Gate-Source Leakage Reverse		—	—	-100	nA	$V_{GS} = -15V$
I_{DSS}	Zero Gate Voltage Drain Current		—	—	250	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0V$
			—	—	1.0	mA	$V_{DS} = \text{Max. Rating} \times 0.8$, $V_{GS} = 0V$, $T_C = 125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2)		6.7	—	—	A	$V_{DS} \geq I_{D(on)} \times R_{DS(on)max}$, $V_{GS} = 5.0V$
$R_{DS(on)}$	Static Drain-Source On-State Resistance (2)		—	0.18	0.30	Ω	$V_{GS} = 5.0V$, $I_D = 4.0A$
g_{fs}	Forward Transconductance (2)		4.0	—	—	Ω	$V_{DS} \geq 15V$, $I_D = 4.0A$
C_{iss}	Input Capacitance		—	400	—	pF	$V_{GS} = 0V$, $V_{DS} = 25V$, $f = 1.0MHz$
C_{oss}	Output Capacitance		—	150	—	pF	
C_{rss}	Reverse Transfer Capacitance		—	50	—	pF	
$t_{d(on)}$	Turn-On Delay Time		—	12	20	ns	$V_{DD} = 0.5BV_{DSS}$, $I_D = 4.0A$, $Z_\theta = 50\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time		—	35	50	ns	
$t_{d(off)}$	Turn-Off Delay Time		—	35	50	ns	
t_f	Fall Time		—	30	40	ns	
Q_g	Total Gate Charge		—	—	10	nC	$V_{GS} = 5V$, $I_D = 6.7A$, $V_{DS} = 0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature)
Q_{gs}	Gate-Source Charge		—	7	—	nC	
Q_{gd}	Gate-Drain Charge		—	1.5	—	nC	

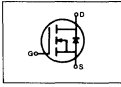
THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	—	—	5.0	K/W	
R_{thCS}	Case-to-Sink	—	0.5	—	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	—	—	80	K/W	Free Air Operation

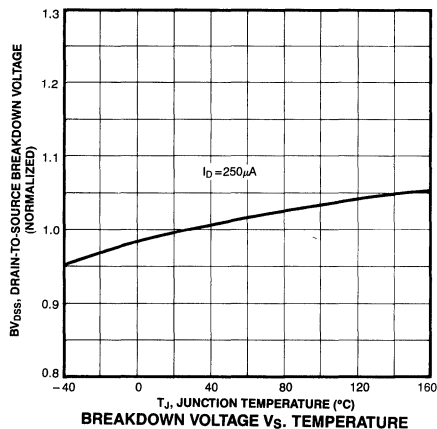
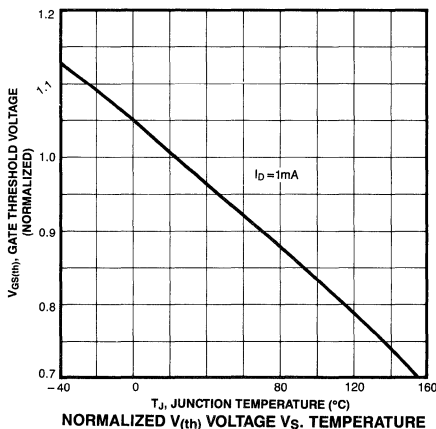
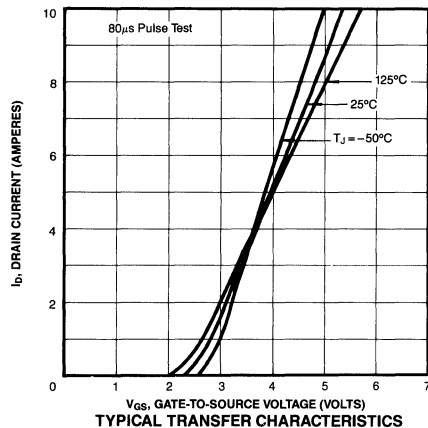
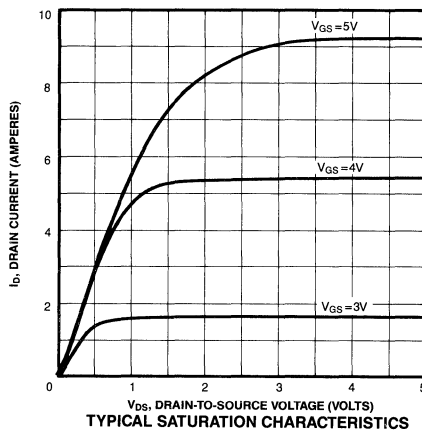
Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

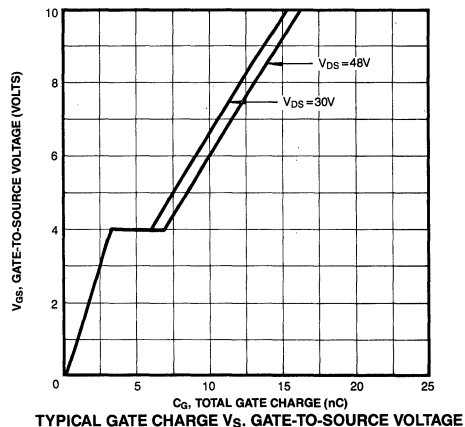
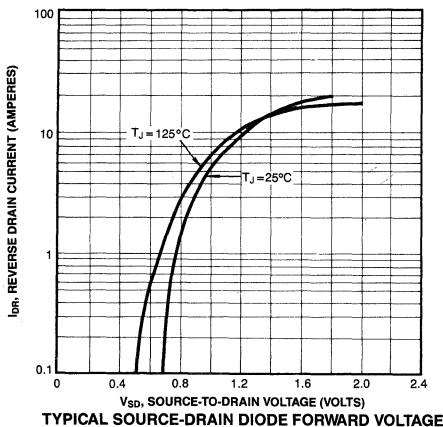
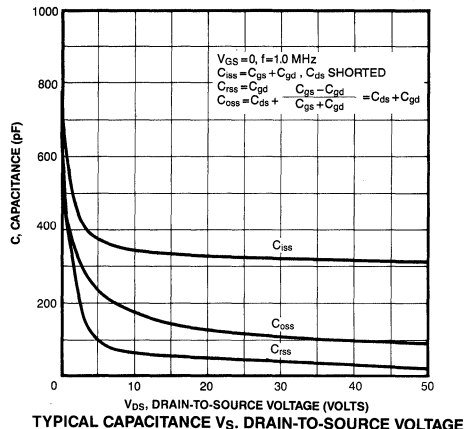
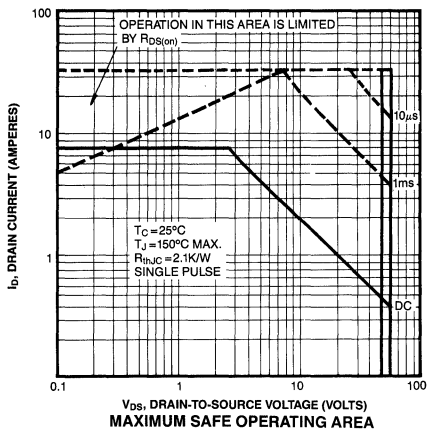
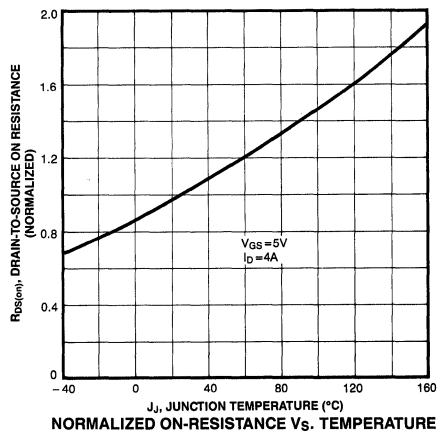
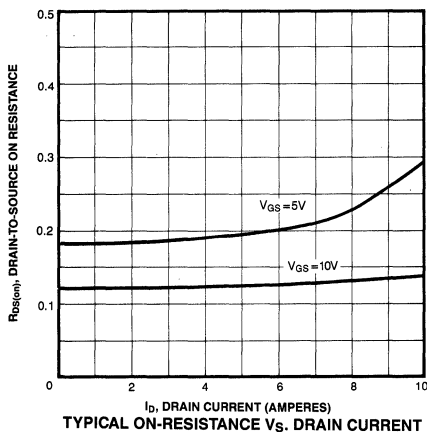
(3) Repetitive rating: Pulse width limited by max. junction temperature

SOURCE-DRAIN DIODE RATING AND CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
I_S	Continuous Source Current (Body Diode)	—	—	6.7	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier 
I_{SM}	Pulse Source Current (Body Diode) (3)	—	—	27	A	
V_{SD}	Diode Forward Voltage (2)	—	—	1.8	V	$T_C = 25^\circ\text{C}$, $I_S = 6.7\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	—	300	ns	$T_J = 25^\circ\text{C}$, $I_F = 6.7\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$

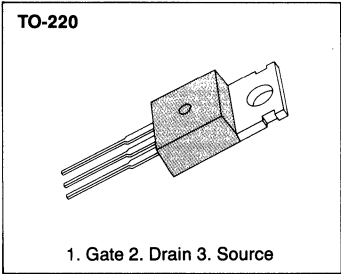
Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C
(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse width limited by max. junction temperature





FEATURES

- Lower $R_{DS(on)}$
- Excellent voltage stability
- Fast switching speeds
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability
- TO-220 Package



PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	$I_{D(on)}$
IRLZ24	60V	0.15Ω	14A
IRLZ20	50V	0.15Ω	14A

MAXIMUM RATINGS

Characteristic	Symbol	IRLZ24	IRLZ20	Units
Drain-Source Voltage (1)	V_{DSS}	60	50	Vdc
Drain-Gate Voltage ($R_{GS}=1.0M\ \Omega$) (1)	V_{DGR}	60	50	Vdc
Gate-Source Voltage	V_{GS}	± 15		Vdc
Continuous Drain Current $T_C=25^{\circ}C$	I_D	14.0	14.0	Adc
Continuous Drain Current $T_C=100^{\circ}C$	I_D	8.7	8.7	Adc
Drain Current—Pulsed (3)	I_{DM}	52	52	Adc
Total Power Dissipation @ $T_C=25^{\circ}C$ Derate above $25^{\circ}C$	P_D	50 0.33		Watts W/ $^{\circ}C$
Operation and Storage Junction Temperature Range	T_J, T_{stg}	- 55 to 175		$^{\circ}C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300		$^{\circ}C$

Notes: (1) $T_J=25^{\circ}C$ to $150^{\circ}C$
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse width limited by max. junction temperature

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage	IRLZ24 60 IRLZ20 50	— —	— —	V	$V_{GS} = 0V$ $I_D = 250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	$V_{DS} = V_{GS}$, $I_D = 1.0mA$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS} = 15V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	- 100	nA	$V_{GS} = -15V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0V$
		—	—	1.0	mA	$V_{DS} = \text{Max. Rating} \times 0.8$, $V_{GS} = 0V$, $T_C = 125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2)	14.0	—	—	A	$V_{DS} \geq I_{D(on)} \times R_{DS(on)max}$, $V_{GS} = 5.0V$
$R_{DS(on)}$	Static Drain-Source On-State Resistance (2)	—	0.10	0.15	Ω	$V_{GS} = 5.0V$, $I_D = 7A$
g_{fs}	Forward Transconductance (2)	2.0	—	—	S	$V_{DS} \geq 15V$, $I_D = 8.0A$
C_{iss}	Input Capacitance	—	750	—	pF	$V_{GS} = 0V$, $V_{DS} = 25V$, $f = 1.0MHz$
C_{oss}	Output Capacitance	—	250	—	pF	
C_{rss}	Reverse Transfer Capacitance	—	120	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	—	40	ns	$V_{DD} = 0.5BV_{DSS}$, $I_D = 8.0A$, $Z_O = 50\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	—	260	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	—	200	ns	
t_f	Fall Time	—	—	200	ns	
Q_g	Total Gate Charge	—	—	22	nC	$V_{GS} = 5V$, $I_D = 14A$, $V_{DS} = 0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature)
Q_{gs}	Gate-Source Charge	—	7	—	nC	
Q_{gd}	Gate-Drain Charge	—	7	—	nC	

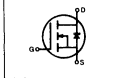
THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	—	—	3.0	K/W	
R_{thCS}	Case-to-Sink	—	0.5	—	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	—	—	80	K/W	Free Air Operation

Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

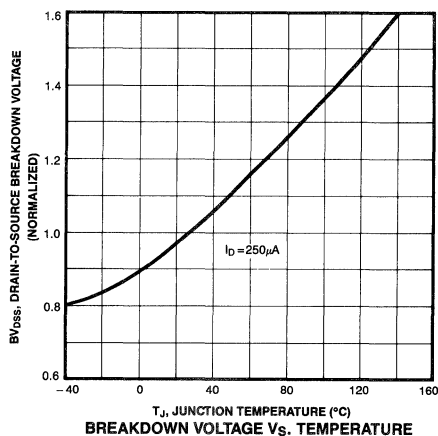
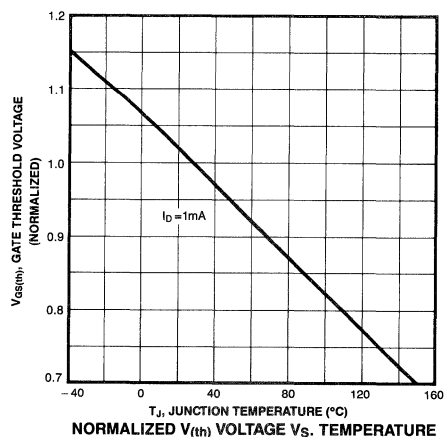
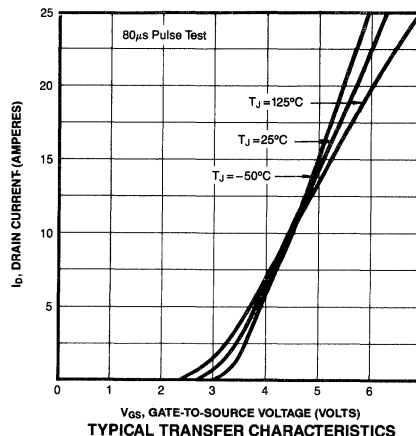
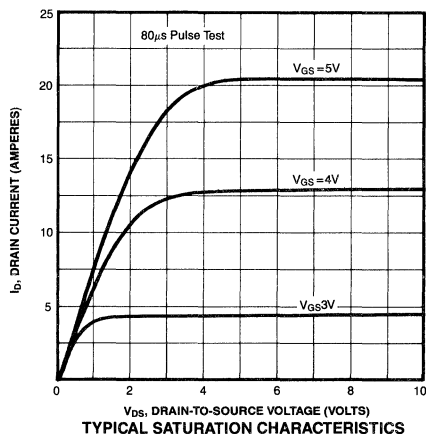
(3) Repetitive rating: Pulse width limited by max. junction temperature

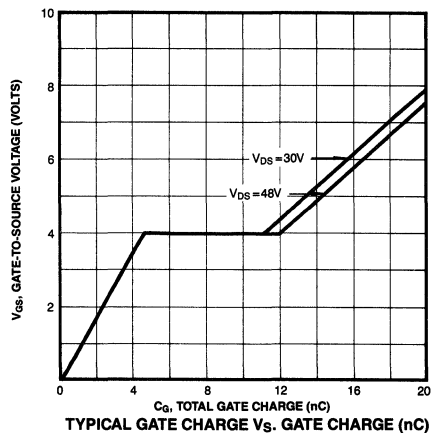
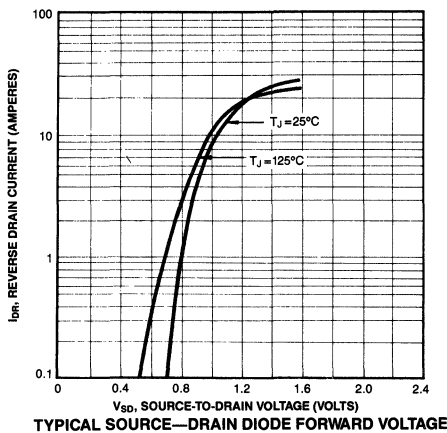
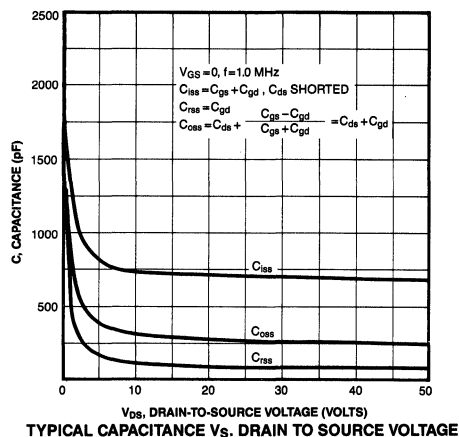
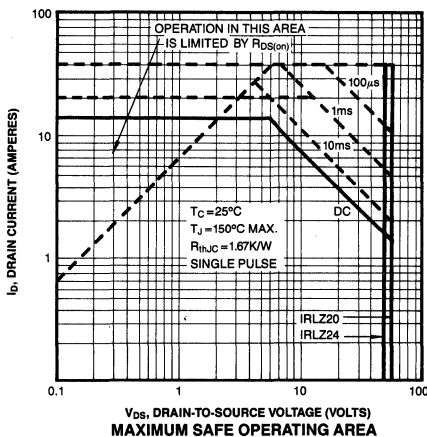
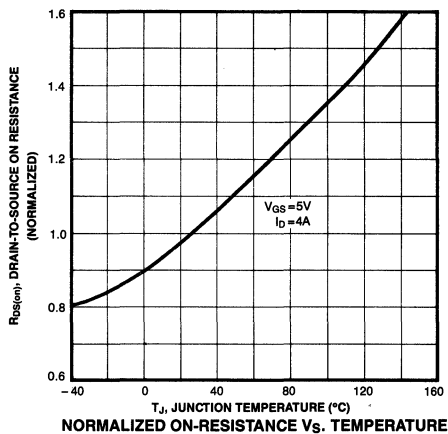
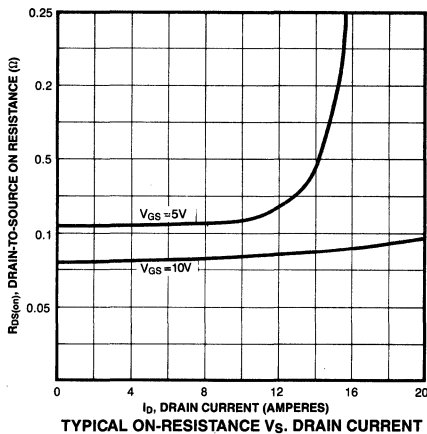
SOURCE-DRAIN DIODE RATING AND CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
I_S	Continuous Source Current (Body Diode)	—	—	14	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier 
I_{SM}	Pulse Source Current (Body Diode) (3)	—	—	52	A	
V_{SD}	Diode Forward Voltage (2)	—	—	1.8	V	$T_C = 25^\circ\text{C}$, $I_S = 14.0\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	300	—	ns	$T_J = 25^\circ\text{C}$, $I_F = 14.0\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$

- Notes:** (1) $T_J = 25^\circ\text{C}$ to 150°C
 (2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
 (3) Repetitive rating: Pulse width limited by max. junction temperature

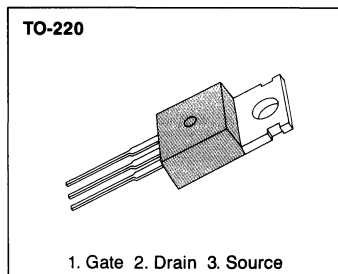
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FEATURES

- Lower $R_{DS(on)}$
- Excellent voltage stability
- Fast switching speeds
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability
- TO-220 Package



PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	$I_{D(on)}$
IRLZ34	60V	0.07Ω	25A
IRLZ30	50V	0.07Ω	25A

MAXIMUM RATINGS

Characteristic	Symbol	IRLZ34	IRLZ30	Units
Drain-Source Voltage (1)	V_{DS}	60	50	Vdc
Drain-Gate Voltage ($R_{GS} = 1.0M\Omega$) (1)	V_{DGR}	60	50	Vdc
Gate-Source Voltage	V_{GS}	± 15		Vdc
Continuous Drain Current $T_C = 25^\circ C$	I_D	25.0	25.0	Adc
Continuous Drain Current $T_C = 100^\circ C$	I_D	18.7	18.7	Adc
Drain Current—Pulsed (3)	I_{DM}	80	80	Adc
Total Power Dissipation @ $T_C = 25^\circ C$ Derate above $25^\circ C$	P_D	90 0.60		Watts W/ $^\circ C$
Operation and Storage Junction Temperature Range	T_J, T_{stg}	- 55 to 175		$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300		$^\circ C$

Notes: (1) $T_J = 25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse width limited by max. junction temperature

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic		Min	Typ	Max	Units	Test Condition
BV_{DS}	Drain-Source Breakdown Voltage	IRLZ34 IRLZ30	60 50	— —	— —	V	$V_{GS} = 0V$ $I_D = 250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage		1.0	—	2.0	V	$V_{DS} = V_{GS}$, $I_D = 1mA$
I_{GSS}	Gate-Source Leakage Forward		—	—	100	nA	$V_{GS} = 15V$
I_{GSS}	Gate-Source Leakage Reverse		—	—	- 100	nA	$V_{GS} = -15V$
I_{DSS}	Zero Gate Voltage Drain Current		—	—	250	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0V$
			—	—	1.0	mA	$V_{DS} = \text{Max. Rating} \times 0.8$, $V_{GS} = 0V$, $T_C = 125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2)		25.0	—	—	A	$V_{DS} \geq I_{D(on)} \times R_{DS(on)max}$, $V_{GS} = 5.0V$
$R_{DS(on)}$	Static Drain-Source On-State Resistance (2)		—	0.06	0.07	Ω	$V_{GS} = 5.0V$, $I_D = 13A$
g_{fs}	Forward Transconductance (2)		9.0	—	—	S	$V_{DS} \geq 15V$, $I_D = 13A$
C_{iss}	Input Capacitance		—	1400	—	pF	$V_{GS} = 0V$, $V_{DS} = 25V$, $f = 1.0MHz$
C_{oss}	Output Capacitance		—	500	—	pF	
C_{rss}	Reverse Transfer Capacitance		—	200	—	pF	
$t_{d(on)}$	Turn-On Delay Time		—	25	40	ns	$V_{DD} = 0.5BV_{DS}$, $I_D = 13A$, $Z_O = 50\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time		—	35	50	ns	
$t_{d(off)}$	Turn-Off Delay Time		—	130	150	ns	
t_f	Fall Time		—	100	120	ns	
Q_g	Total Gate Charge		—	—	36	nC	$V_{GS} = 5V$, $I_D = 25A$, $V_{DS} = 0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature)
Q_{gs}	Gate-Source Charge		—	25	—	nC	
Q_{gd}	Gate-Drain Charge		—	11	—	nC	

THERMAL RESISTANCE

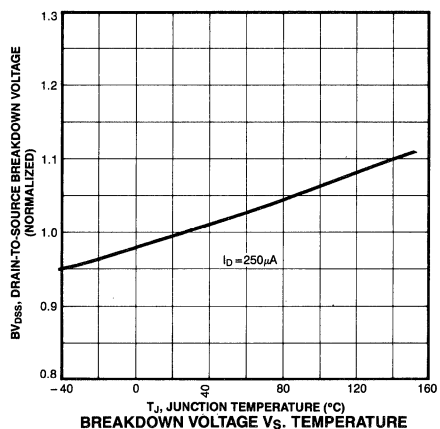
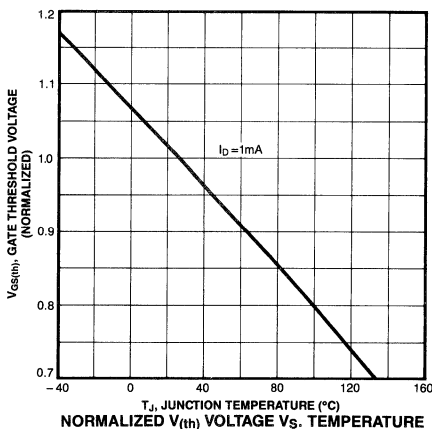
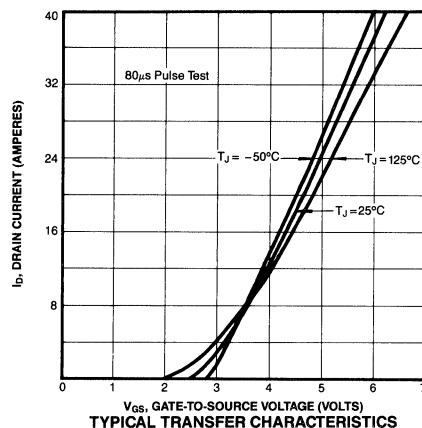
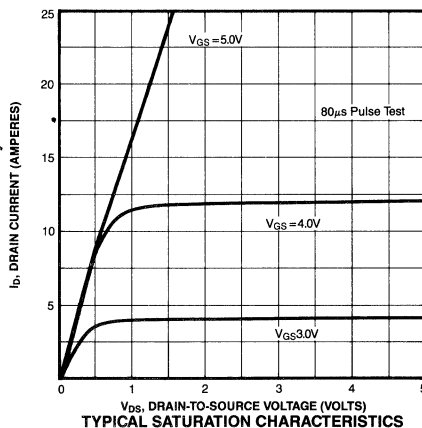
R_{thJC}	Junction-to-Case	—	—	1.7	K/W	
R_{thCS}	Case-to-Sink	—	0.5	—	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	—	—	80	K/W	Free Air Operation

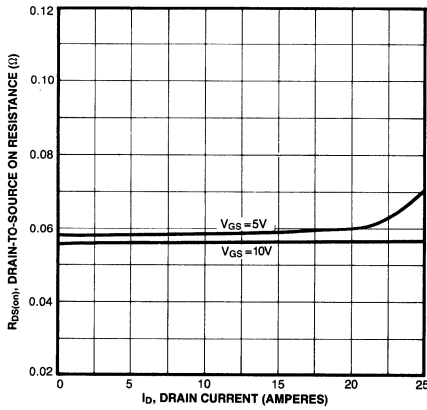
Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C
 (2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
 (3) Repetitive rating: Pulse width limited by max. junction temperature

SOURCE-DRAIN DIODE RATING AND CHARACTERISTICS

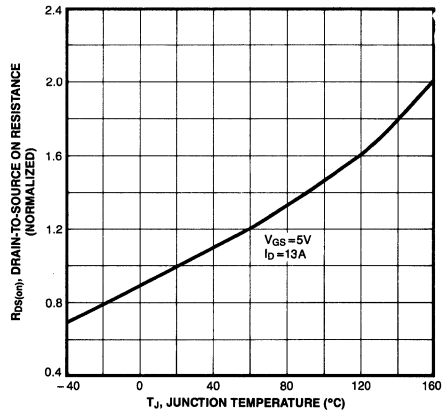
Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
I_S	Continuous Source Current (Body Diode)	—	—	25.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier
I_{SM}	Pulse Source Current (Body Diode) (3)	—	—	80	A	
V_{SD}	Diode Forward Voltage (2)	—	1.2	2.5	V	$T_C = 25^\circ\text{C}$, $I_S = 25.0\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	—	500	ns	$T_J = 25^\circ\text{C}$, $I_F = 25.0\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$

- Notes:** (1) $T_J = 25^\circ\text{C}$ to 150°C
(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse width limited by max. junction temperature

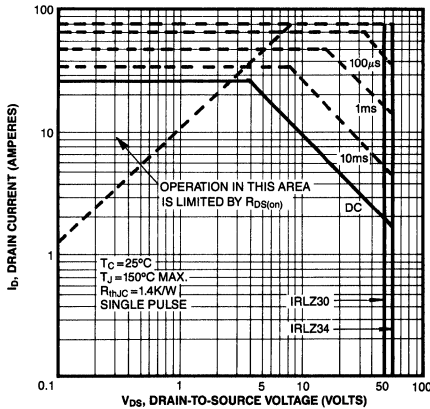




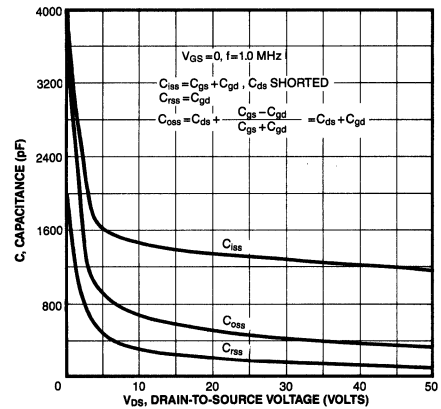
TYPICAL ON-RESISTANCE V_S . DRAIN CURRENT



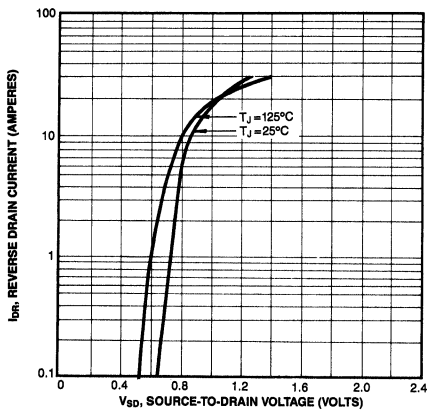
NORMALIZED ON-RESISTANCE V_S . TEMPERATURE



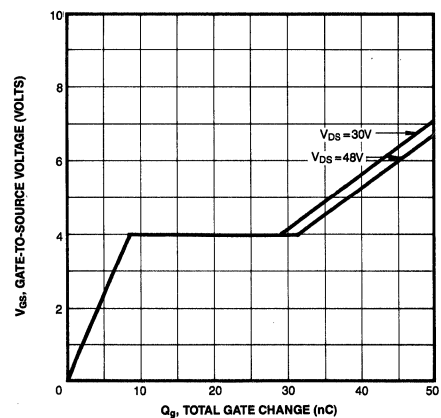
MAXIMUM SAFE OPERATING AREA



TYPICAL CAPACITANCE V_S . DRAIN-TO-SOURCE VOLTAGE



TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

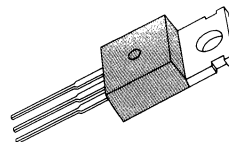


TYPICAL GATE CHARGE V_S . GATE-TO-SOURCE VOLTAGE

FEATURES

- Lower $R_{DS(on)}$
- Excellent voltage stability
- Fast switching speeds
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability
- TO-220 Package

TO-220



1. Gate 2. Drain 3. Source

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	$I_{D(on)}$
IRLZ44	60V	0.04 Ω	35.0A
IRLZ40	50V	0.04 Ω	35.0A

MAXIMUM RATINGS

Characteristic	Symbol	IRLZ44	IRLZ40	Units
Drain-Source Voltage (1)	V_{DSS}	60	50	Vdc
Drain-Gate Voltage ($R_{GS} = 1.0M\ \Omega$) (1)	V_{DGR}	60	50	Vdc
Gate-Source Voltage	V_{GS}	± 15		Vdc
Continuous Drain Current $T_C = 25^\circ C$	I_D	35.0	35.0	Adc
Continuous Drain Current $T_C = 100^\circ C$	I_D	27.0	27.0	Adc
Drain Current—Pulsed (3)	I_{DM}	110	110	Adc
Total Power Dissipation @ $T_C = 25^\circ C$ Derate above $25^\circ C$	P_D	150 1.0		Watts W/ $^\circ C$
Operation and Storage Junction Temperature Range	T_J, T_{stg}	- 55 to 175		$^\circ C$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300		$^\circ C$

Notes: (1) $T_J = 25^\circ C$ to $150^\circ C$

(2) Pulse test: Pulse width $\leq 300\ \mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse width limited by max. junction temperature

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic		Min	Typ	Max	Units	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage	IRLZ44 IRLZ40	60 50	— —	— —	V	$V_{GS} = 0V$ $I_D = 250\mu A$
V_{th}	Gate Threshold Voltage		1.0	—	2.0	V	$V_{DS} = V_{GS}$, $I_D = 1.0mA$
I_{GSS}	Gate-Source Leakage Forward		—	—	100	nA	$V_{GS} = 15V$
I_{GSS}	Gate-Source Leakage Reverse		—	—	- 100	nA	$V_{GS} = -15V$
I_{DSS}	Zero Gate Voltage Drain Current		—	—	250	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0V$
			—	—	1.0	mA	$V_{DS} = \text{Max. Rating} \times 0.8$, $V_{GS} = 0V$, $T_C = 125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2)		35.0	—	—	A	$V_{DS} \geq I_{D(on)} \times R_{DS(on)max}$, $V_{GS} = 5.0V$
$R_{DS(on)}$	Static Drain-Source On-State Resistance (2)		—	0.03	0.04	Ω	$V_{GS} = 5.0V$, $I_D = 18.0A$
g_{fs}	Forward Transconductance (2)		15.0	—	—	S	$V_{DS} \geq 15V$, $I_D = 18.0A$
C_{iss}	Input Capacitance		—	2400	—	pF	$V_{GS} = 0V$, $V_{DS} = 25V$, $f = 1.0MHz$
C_{oss}	Output Capacitance		—	795	—	pF	
C_{rss}	Reverse Transfer Capacitance		—	390	—	pF	
$t_{d(on)}$	Turn-On Delay Time		—	25	40	ns	$V_{DD} = 0.5BV_{DSS}$, $I_D = 18A$, $Z_O = 50\Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time		—	65	85	ns	
$t_{d(off)}$	Turn-Off Delay Time		—	350	400	ns	
t_f	Fall Time		—	180	200	ns	
Q_g	Total Gate Charge		—	—	80	nC	$V_{GS} = 5V$, $I_D = 35A$, $V_{DS} = 0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature)
Q_{gs}	Gate-Source Charge		—	58	—	nC	
Q_{gd}	Gate-Drain Charge		—	22	—	nC	

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	—	—	1.0	K/W	
R_{thCS}	Case-to-Sink	—	0.5	—	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	—	—	80	K/W	Free Air Operation

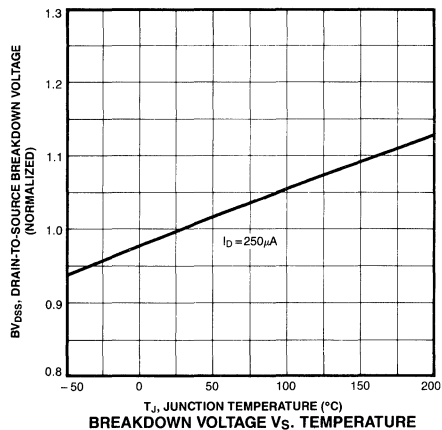
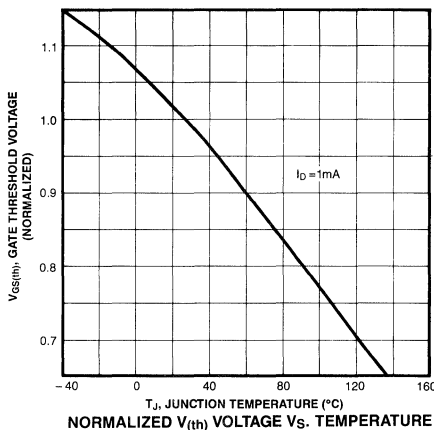
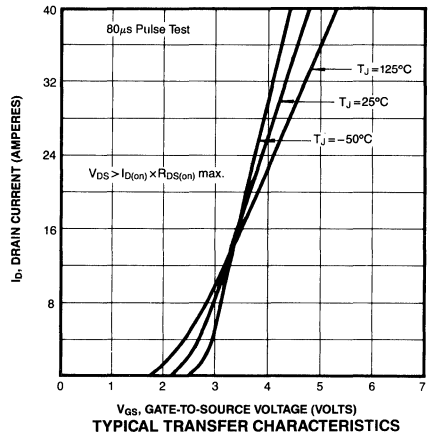
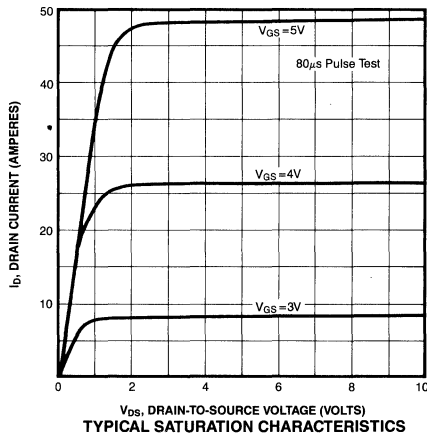
Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse width limited by max. junction temperature

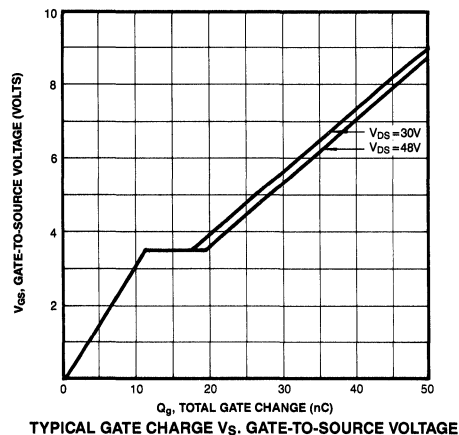
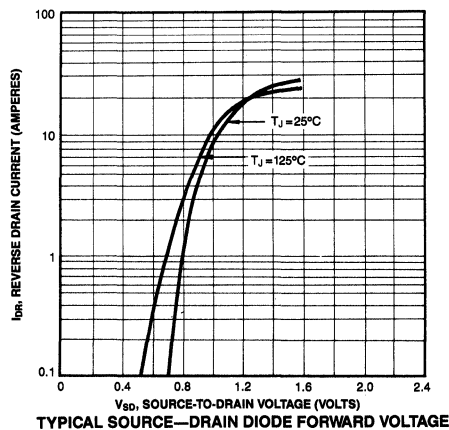
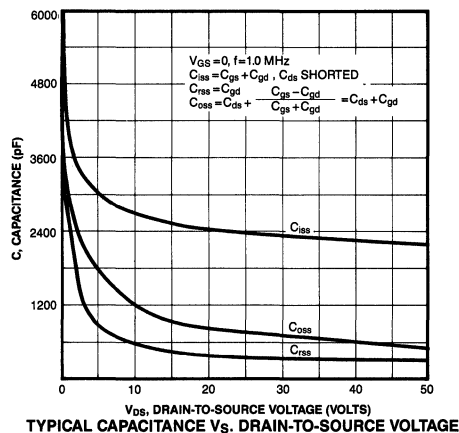
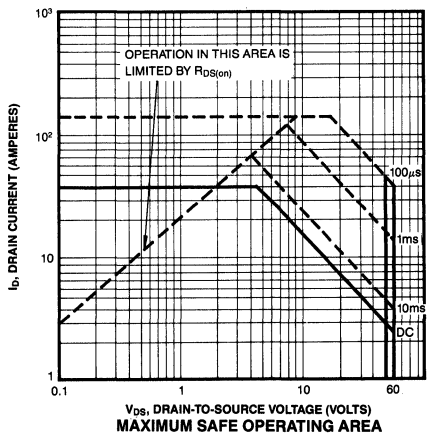
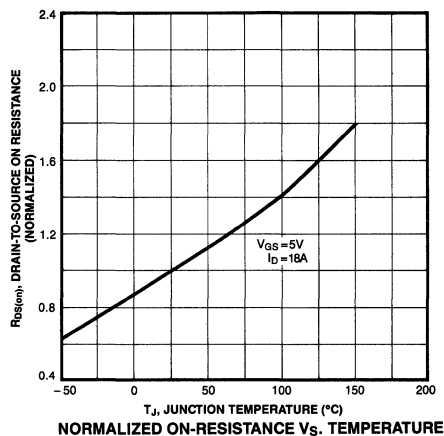
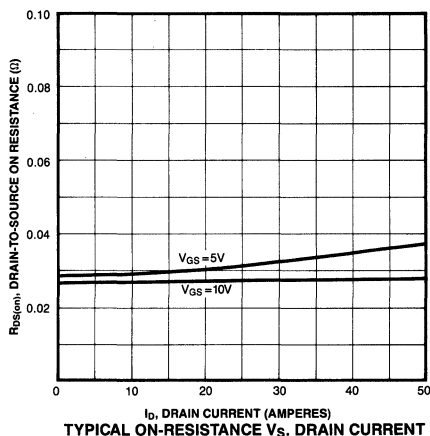
SOURCE-DRAIN DIODE RATING AND CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
I_S	Continuous Source Current (Body Diode)	—	—	35.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier
I_{SM}	Pulse Source Current (Body Diode) (3)	—	—	110	A	
V_{SD}	Diode Forward Voltage (2)	—	1.3	2.5	V	$T_C = 25^\circ\text{C}$, $I_S = 35.0\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	—	600	ns	$T_J = 25^\circ\text{C}$, $I_F = 35.0\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{s}$

Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C
(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse width limited by max. junction temperature

2

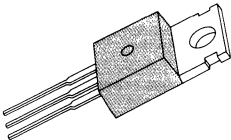




FEATURES

- Lower $R_{DS(on)}$
- Excellent voltage stability
- Fast switching speeds
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability
- TO-220 Package

TO-220



1. Gate 2. Drain 3. Source

PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	$I_{D(on)}$
SSP3055L	60V	0.18 Ω	12A

MAXIMUM RATINGS

Characteristic	Symbol	SSP3055L	Units
Drain-Source Voltage (1)	V_{DSS}	60	Vdc
Drain Gate Voltage ($R_{GS}=1.0M\Omega$) (1)	V_{DGR}	60	Vdc
Gate Source Voltage	V_{GS}	± 15	Vdc
Continuous Drain Current $T_C=25^{\circ}C$	I_D	12	Adc
Continuous Drain Current $T_C=100^{\circ}C$	I_D	8.4	Adc
Drain Current — Pulsed (3)	I_{DM}	26	Adc
Total Power Dissipation @ $T_C=25^{\circ}C$ Derate above $25^{\circ}C$	P_D	40 0.32	Watts W/ $^{\circ}C$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150	$^{\circ}C$
Maximum Lead Temp for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300	$^{\circ}C$

Notes: (1) $T_J = 25^{\circ}C$ to $150^{\circ}C$
(2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse width limited by max. junction temperature

Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
BV_{DSS}	Drain Source Breakdown Voltage	60	—	—	V	$V_{GS}=0V$ $I_D=250\mu A$
$V_{(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	$V_{DS}=V_{GS}$, $I_D=1.0mA$
I_{GSS}	Gate Source Leakage Forward	—	—	100	nA	$V_{GS}=15V$
I_{GSS}	Gate Source Leakage Reverse	—	—	-100	nA	$V_{GS}=-15V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS}=\text{Max. Rating}$, $V_{GS}=0V$
		—	—	1.0	μA	$V_{DS}=\text{Max. Rating} \times 0.8$, $V_{GS}=0V$, $T_C=125^\circ C$
$I_{D(on)}$	On static Drain Source Current (2)	12	—	—	A	$V_{DS}>R_{DS(on)} \text{ max.}$, $V_{GS}=5V$
$R_{DS(on)}$	Static Drain Source On State Resistance (2)	—	0.13	0.18	Ω	$V_{GS}=5.0V$, $I_D=6.0A$
g_{fs}	Forward Transconductance (2)	5.0	—	—	Ω	$V_{DS}<15V$, $I_D=6.0A$
C_{iss}	Input Capacitance	—	440	—	pF	$V_{GS}=0V$, $V_{DS}=25V$, $f=1.0MHz$
C_{oss}	Output Capacitance	—	190	—	pF	
C_{rss}	Reverse Transfer Capacitance	—	50	—	pF	
$t_{d(on)}$	Turn On Delay Time	—	15	—	ns	$V_{DD}=0.5 BV_{DSS}$, $I_D=6.0A$, $Z_O=50 \text{ Ohms}$, (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	—	25	—	ns	
$t_{d(off)}$	Turn Off Delay Time	—	40	—	ns	
t_f	Fall Time	—	25	—	ns	
Q_g	Total Gate Charge	—	—	17	nC	$V_{GS}=5V$, $I_D=12A$, $V_{DS}0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature)
Q_{gs}	Gate Source Charge	—	6	—	nC	
Q_{gd}	Gate Drain Charge	—	5	—	nC	

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	—	—	3.12	K/W	
R_{thCS}	Case-to-Sink	—	0.5	—	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	—	—	80	K/W	Free Air Operation

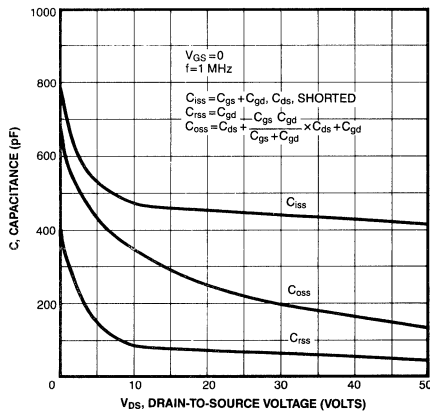
Notes: (1) $T_J=25^\circ C$ to $150^\circ C$ (2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive: Pulse width limited by max. junction temperature

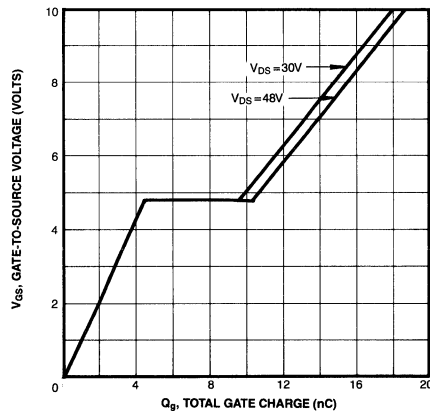
SOURCE DRAIN DIODE RATING AND CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
I_S	Continuous Source Current (Body Diode)	—	—	12	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier
I_{SM}	Pulse Source Current (Body Diode) (3)	—	—	26	A	
V_{SD}	Diode Forward Voltage (2)	—	—	3.8	V	$T_C = 25^{\circ}\text{C}$, $I_S = 12\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	110	—	ns	$T_J = 25^{\circ}\text{C}$, $I_F = 12\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$

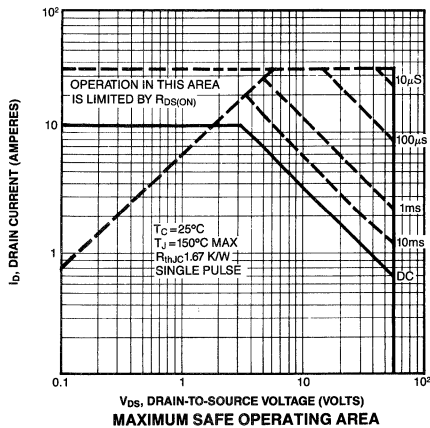
- Notes: (1) $T_J = 25^{\circ}\text{C}$ to 150°C
(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse width limited by max. junction temperature



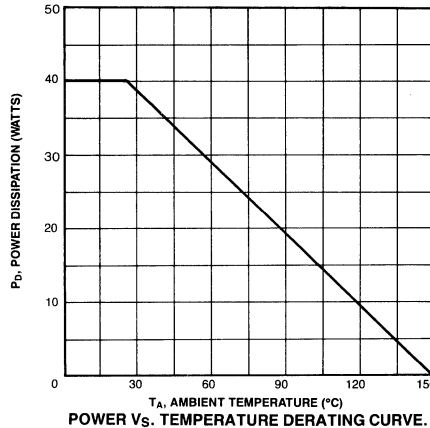
TYPICAL CAPACITANCE VS. DRAIN TO SOURCE VOLTAGE



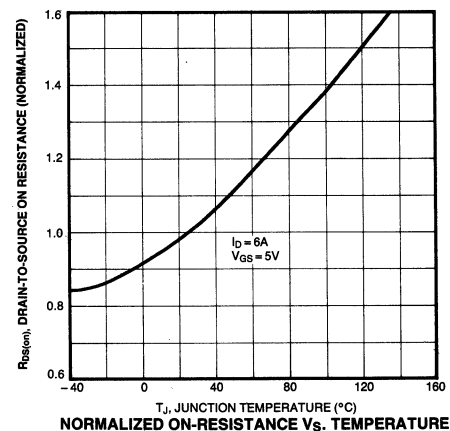
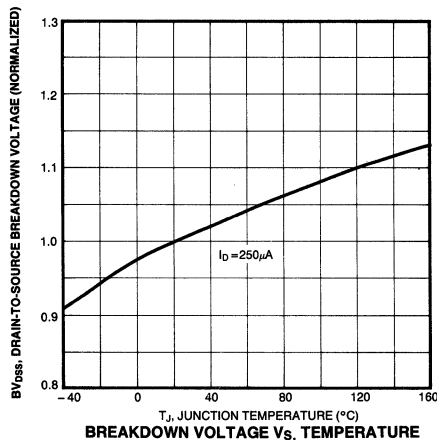
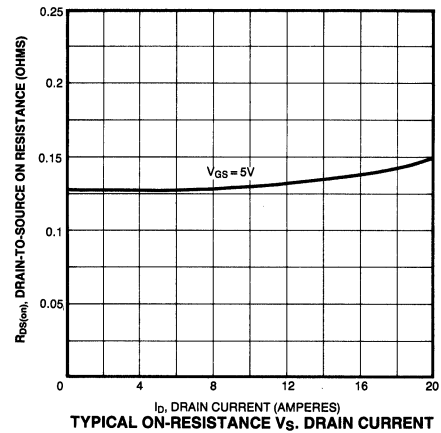
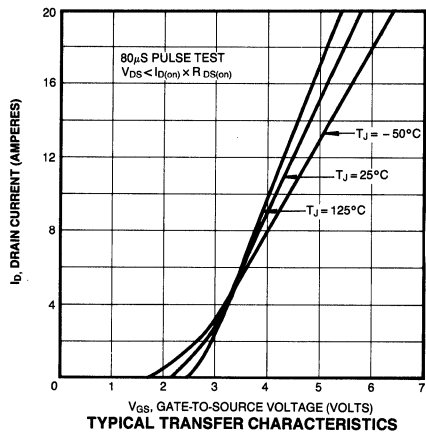
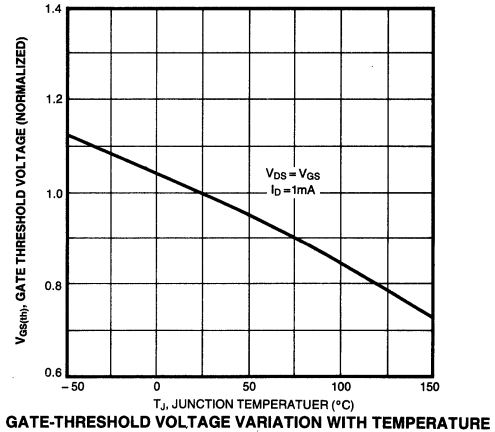
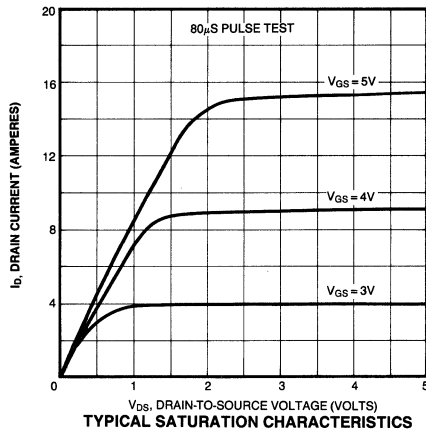
TYPICAL GATE CHARGE VS. GATE-TO-SOURCE VOLTAGE



MAXIMUM SAFE OPERATING AREA



POWER VS. TEMPERATURE DERATING CURVE.

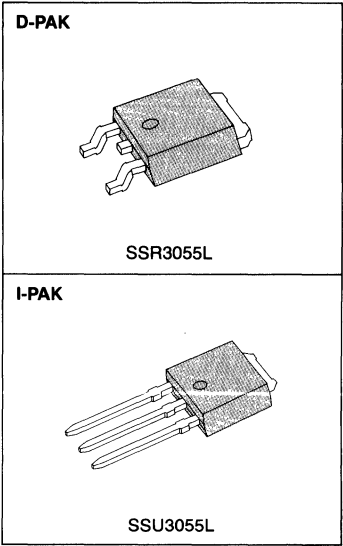


FEATURES

- Lower Rps (ON)
- Excellent voltage stability
- Fast switching speeds
- Rugged polysilicon gate cell structure
- Lower input capacitance
- Extended safe operating area
- Improved high temperature reliability
- D-PAK/I-PAK

PRODUCT SUMMARY

Part Number	VDS	RDS(on)	ID(on)
SSR3055L/SSU3055L	60V	0.18Ω	12A



MAXIMUM RATINGS

Characteristic	Symbol	SSR3055L/U3055L	Units
Drain-Source Voltage (1)	V _{DSS}	60	V _{dc}
Drain Gate Voltage (R _{GS} =1.0MΩ) (1)	V _{DGR}	60	V _{dc}
Gate-Source Voltage	V _{GS}	± 15	V _{dc}
Continuous Drain Current T _C =25°C	I _D	12	A _{dc}
Continuous Drain Current T _C =100°C	I _D	8.4	A _{dc}
Drain Current—Pulsed (3)	I _{DM}	36	A _{dc}
Total Power Dissipation @ T _C =25°C Derate above 25°C	P _D	42 0.33	Watts W/°C
Operating and Storage Junction Temperature Range	T _J , T _{slg}	–55 to 150	°C
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T _L	300	°C

Notes: (1) T_J = 25°C to 150°C
(2) Pulse test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
(3) Repetitive rating: Pulse width limited by max. junction temperature

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
BV_{DSS}	Drain Source Break Voltage	60	—	—	V	$V_{GS} = 0V$ $I_D = 250\mu A$
V_{th}	Gate Threshold Voltage	1.0	—	2.0	V	$V_{DS} = V_{GS}$, $I_D = 1.0mA$
I_{GSS}	Gate-Source Leakage Forward	—	—	100	nA	$V_{GS} = 15V$
I_{GSS}	Gate-Source Leakage Reverse	—	—	- 100	nA	$V_{GS} = - 15V$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	$V_{DS} = \text{Max. Rating}$ $V_{GS} = 0V$
		—	—	1.0	mA	$V_{DS} = \text{Max. Rating} \times 0.8$, $V_{GS} = 0V$, $T_C = 125^\circ\text{C}$
$I_{D(on)}$	On-State Drain-Source Current (2)	12	—	—	A	$V_{DS} \geq I_{D(on)} \times R_{DS(on)max}$. $V_{GS} = 5V$
$R_{DS(on)}$	Static Drain-Source On-State Resistance (2)	—	0.13	0.18	Ω	$V_{GS} = 5.0V$, $I_D = 6.0A$
g_{fs}	Forward Transconductance (2)	5.0	—	—	S	$V_{DS} \geq 15V$, $I_D = 6.0A$
C_{iss}	Input Capacitance	—	400	—	pF	$V_{GS} = 0V$, $V_{DS} = 25V$, $f = 1.0MHz$
C_{oss}	Output Capacitance	—	175	—	pF	
C_{rss}	Reverse Transfer Capacitance	—	50	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	15	—	ns	$V_{DD} = 0.5BV_{DSS}$, $I_D = 6.0A$, $Z_{\theta} 50 \Omega$ (MOSFET switching times are essentially independent of operating temperature)
t_r	Rise Time	—	25	—	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	40	—	ns	
t_f	Fall Time	—	25	—	ns	$V_{GS} = 5V$, $I_D = 12A$, $V_{DS} = 0.8 \text{ Max. Rating}$ (Gate charge is essentially independent of operating temperature)
Q_g	Total Gate Charge	—	—	17	nC	
Q_{gs}	Gate-Source Charge	—	2	—	nC	
Q_{gd}	Gate-Drain Charge	—	4	—	nC	

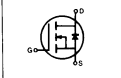
THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	—	—	3.0	K/W	
R_{thCS}	Case-to-Sink	—	1.7	—	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	—	—	110	K/W	Free Air Operation

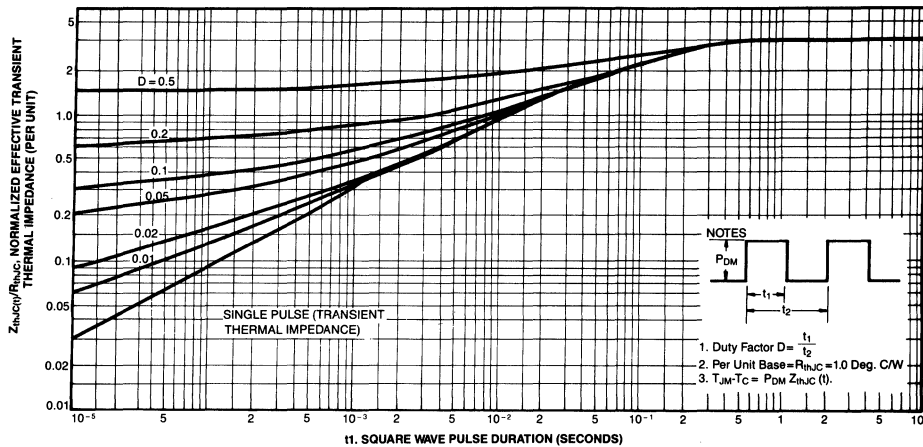
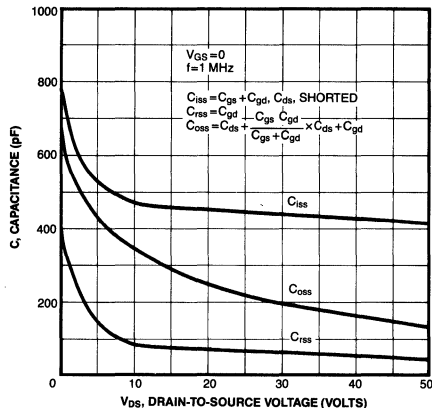
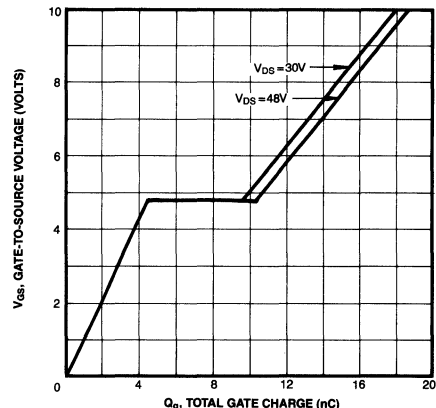
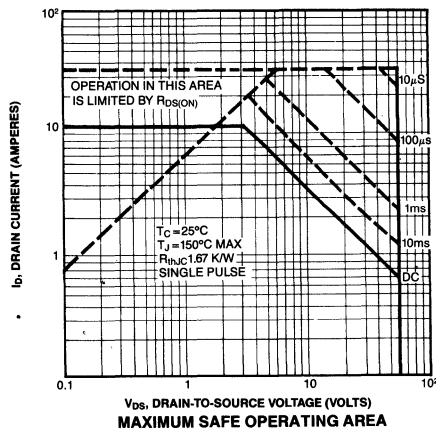
Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C (2) Pulse test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

(3) Repetitive rating: Pulse width limited by max. junction temperature

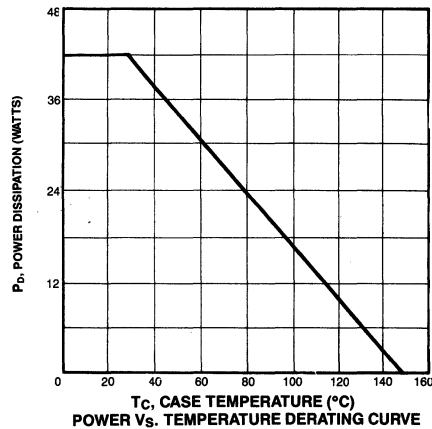
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Units	Test Condition
I_S	Continuous Source Current (Body Diode)	—	—	12	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier 
I_{SM}	Pulse-Source Current (Body Diode)	—	—	36	A	
V_{SD}	Diode Forward Voltage (2)	—	—	2.0	V	$T_C = 25^\circ\text{C}$, $I_S = 12\text{A}$, $V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	55	—	ns	$T_J = 25^\circ\text{C}$, $I_F = 12\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{S}$

Notes: (1) $T_J = 25^\circ\text{C}$ to 150°C
(2) Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
(3) Repetitive rating: Pulse width limited by max. junction temperature


MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE JUNCTION-TO-CASE V_S , PULSE DURATION

TYPICAL CAPACITANCE V_S , DRAIN TO SOURCE VOLTAGE

TYPICAL GATE CHARGE V_S , GATE-TO-SOURCE VOLTAGE


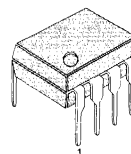
MAXIMUM SAFE OPERATING AREA


POWER V_S , TEMPERATURE DERATING CURVE

LOW POWER CONSUMPTION EARTH LEAKAGE DETECTOR

The KA2808 is a low power controller for AC outlet ground fault interrupters. This device detects hazardous grounding conditions and open circuits the AC line before a harmful or lethal shock occurs. Also contained internally is a 26(V) zener shunt regulator, and op amp, and a SCR driver. With the addition of two sense coils, a bridge rectifier, a SCR, and a relay, the KA2808 will detect and protect against both hot wire to ground and neutral wire to ground faults.

8 DIP



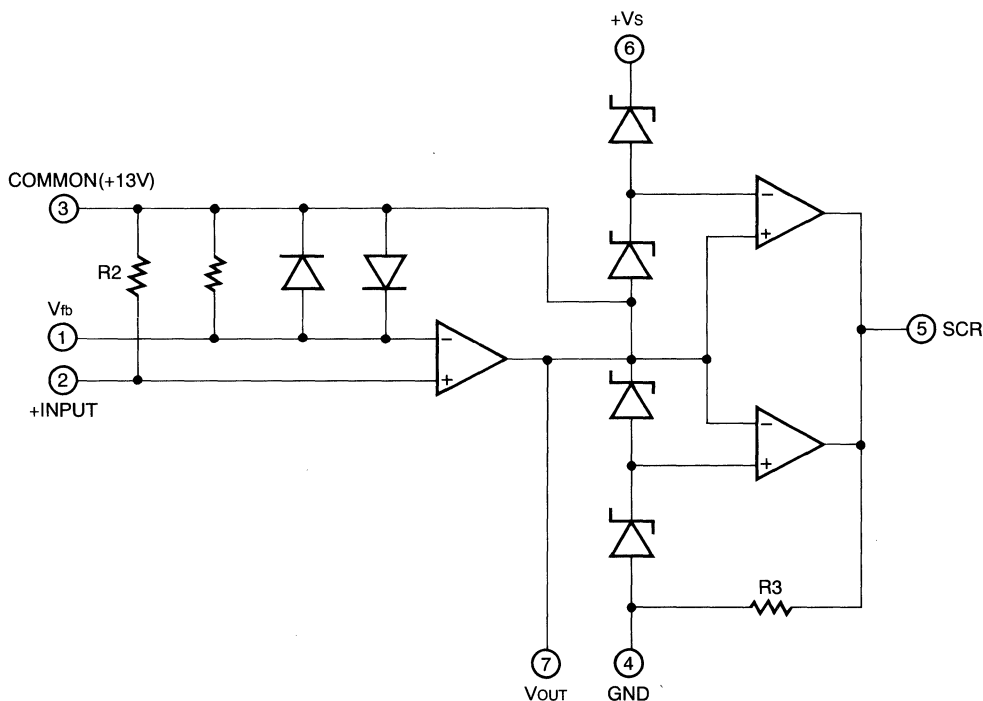
FEATURES

- Supply Voltage Drived from AC Line : 26(V)
- Quiescent Current : 450(μ A)
- Use for 120(V) or 220(V) Systems
- Meets U.L 943 Condition
- Direct Interface to SCR
- Grounded Neutral Fault Detection
- No Potentiometer Required
- Adjustable Sensitivity

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2808	8 DIP	0 ~+70°C

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Characteristic	Symbol	Value	Units
Supply Current	I _{CC}	18	mA
Power Dissipation	P _D	500	mW
Storage Temperature Range	T _{STG}	- 65 ~ 150	°C
Operating Temperature Range	T _{OPR}	- 35 ~ 80	°C
Lead Temperature Soldering = 60 sec	T _{LEAD}	300, DIP	°C

ELECTRICAL CHARACTERISTICS (T = 25°C, I_S = 1.5mA)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Zener Voltage		V _Z	Pin6 to Pin4	25	26	29	V
Reference Voltage		V _{REF}	Pin3 to Pin4	12.5	13	14.5	V
Quiescent Current		V _Q	+V _S =24(V)	—	400	750	μA
OPamp	Offset Voltage	V _{OS}	Pin2 to Pin3	-3.0	0	+3.0	mV
	+Output Voltage Swing	V _{OH}	Pin7 to Pin3	7	7.2	7.8	V
	- Output Voltage Swing	V _{OL}	Pin7 to Pin3	10.5	11.2	12.5	V
	+Output Source Current	I _O (SOURCE)	Pin7 to Pin3	—	650	—	μA
	- Output Source Current	I _O (SINK)	Pin7 to Pin3	—	1	—	mA
	Gain Bandwidth Product	GBW	F=50(KHz)	1.0	1.8	—	MHz
Detector Reference Voltage		V _{REF} (DET)	Pin7 to Pin3	7	7.2	7.8	V
R1 Resistor(I _S =0)		R1	Pin2 to Pin3	—	10	—	KOhm
R2 Resistor(I _S =0)		R2	Pin1 to Pin3	—	10	—	KOhm
R3 Resistor(I _S =0)		R3	Pin5 to Pin4	3.5	4.7	5.9	KOhm
SCR Trigger Detector on Voltage		V _{ON} (SCR)	Pin5 to Pin4	1.5	2.8	—	V
SCR Trigger Detector off Voltage		V _{OFF} (SCR)	Pin5 to Pin4	0	1	10	mV

ELECTRICAL CHARACTERISTICS ($I_s = 1.5\text{mA}$, over specified temperature range)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Zener Voltage		V_Z	Pin6 to Pin4	24	26	30	V
Reference Voltage		V_{REF}	Pin3 to Pin4	12	13	15	V
Quiescent Current		I_Q	$+V_S=24(V)$	—	500	800	μA
OPamp	Offset Voltage	V_{OS}	Pin2 to Pin3	-5.0	0	+5.0	mV
	+Output Voltage Swing	V_{OH}	Pin7 to Pin3	6.5	7.2	8.3	V
	- Output Voltage Swing	V_{OL}	Pin7 to Pin3	-9	11.2	-14	V
	Gain Bandwidth Product	GBW	$F=50(\text{KHz})$	—	1.8	—	MHz
Detector Reference Voltage		$V_{REF(DET)}$	Pin7 to Pin3	6.5	7.2	8.3	V
R1 Resistor($I_s=0$)		R1	Pin2 to Pin3	—	10	—	KOhm
R2 Resistor($I_s=0$)		R2	Pin1 to Pin3	—	10	—	KOhm
R3 Resistor($I_s=0$)		R3	Pin5 to Pin4	3.4	4.7	5.9	KOhm
SCR Trigger Detector on Voltage		$V_{ON(SCR)}$	Pin5 to Pin4	1.3	2.8	—	V
SCR Trigger Detector off Voltage		$V_{OFF(SCR)}$	Pin5 to Pin4	0	3	50	mV

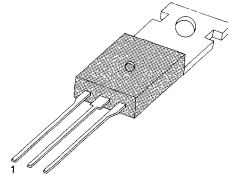
3-TERMINAL 1A POSITIVE ADJUSTABLE REGULATOR

This monolithic integrated circuit is an adjustable 3-terminal positive voltage regulator designed to supply more than 1.5A of load current with an output voltage adjustable over a 1.2 to 37V. It employs internal current limiting, thermal shut-down and safe area compensation.

FEATURES

- Output Current In Excess of 1.5A
- Output Adjustable Between 1.2V and 37V
- Internal Thermal-Overload Protection
- Internal Short-Circuit Current-Limiting
- Output Transistor Safe-Area Compensation

TO-220

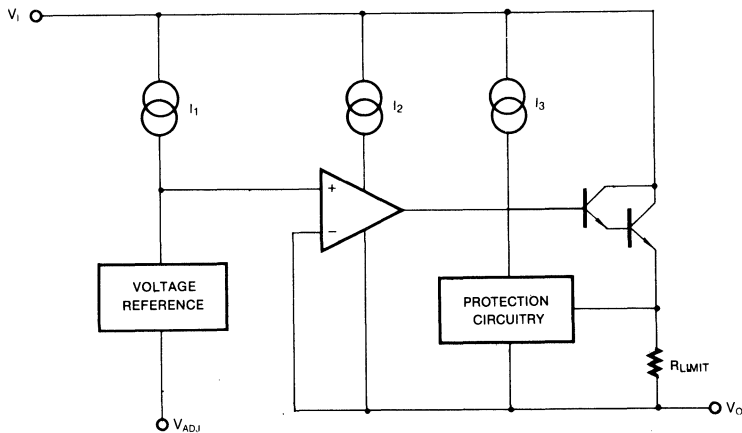


1: Adj 2: Output 3: Input

ORDERING INFORMATION

Device	Package	Operating Temperature
KA317	TO-220	0°C ~ 125°C

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise specified)

Characteristic	Symbol	Value	Unit
Input-Output Voltage Differential	$V_i - V_o$	40	V
Lead Temperature	T_{LEAD}	230	$^\circ\text{C}$
Power Dissipation	P_D	Internally limited	—
Operating Temperature Range	T_{OPR}	$0 \sim +125$	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	$-65 \sim +150$	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS

($V_i - V_o = 5\text{V}$, $I_o = 0.5\text{A}$, $0^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$, $I_{\text{MAX}} = 1.5\text{A}$, $P_{\text{MAX}} = 20\text{W}$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Line Regulation	ΔV_o	$T_A = 25^\circ\text{C}$ $3\text{V} \leq V_i - V_o \leq 40\text{V}$		0.01	0.04	%/V
		$3\text{V} \leq V_i - V_o \leq 40\text{V}$		0.02	0.07	%/V
Load Regulation	ΔV_o	$T_A = 25^\circ\text{C}$, $10\text{mA} \leq I_o \leq I_{\text{MAX}}$ $V_o \leq 6\text{V}$ $V_o \geq 5\text{V}$		18 0.4	25 0.5	mV %/V _o
		$10\text{mA} \leq I_o \leq I_{\text{MAX}}$ $V_o \leq 5\text{V}$ $V_o \geq 5\text{V}$		40 0.8	70 1.5	mV %/V _o
Adjustable Pin Current	I_{ADJ}			46	100	μA
Adjustable Pin Current Change	ΔI_{ADJ}	$2.5\text{V} \leq V_i - V_o \leq 40\text{V}$ $10\text{mA} \leq I_o \leq I_{\text{MAX}}$ $P \leq P_{\text{MAX}}$		2.0	5	μA
Reference Voltage	V_{REF}	$3\text{V} \leq V_{\text{IN}} - V_{\text{OUT}} \leq 40\text{V}$ $10\text{mA} \leq I_o \leq I_{\text{MAX}}$ $P_D \leq P_{\text{MAX}}$	1.20	1.25	1.30	V
Temperature Stability	ST_T			0.7		%/V _o
Minimum Load Current to Maintain Regulation	$I_{\text{L (MIN)}}$	$V_i - V_o = 40\text{V}$		3.5	10	mA
Maximum Output Current	$I_o (\text{MAX})$	$V_i - V_o \leq 15\text{V}$, $P_D \leq P_{\text{MAX}}$ $V_i - V_o \leq 15\text{V}$, $P_D \leq P_{\text{MAX}}$, $T_A = 25^\circ\text{C}$	1.5 0.15	2.2 0.4		A
RMS Noise, % of V_{OUT}	e_N	$T_A = 25^\circ\text{C}$, $10\text{Hz} \leq f \leq 10\text{KHz}$		0.003	0.01	%/V _o
Ripple Rejection	RR	$V_o = 10\text{V}$, $f = 120\text{Hz}$ without C_{ADJ} $C_{\text{ADJ}} = 10\mu\text{F}$	66	60 75		dB
Long-Term Stability, $T_J = T_{\text{HIGH}}$	ST	$T_A = 25^\circ\text{C}$ for end point measurements, 100HR		0.3	1	%
Thermal Resistance Junction to Case	$R_{\theta\text{JC}}$			5		$^\circ\text{C/W}$

* Load and line regulation are specified at constant junction temperature. Change in V_o due to heating effects must be taken into account separately. Pulse testing with low duty is used. ($P_{\text{MAX}} \leq 20\text{W}$)

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1 LOAD REGULATION

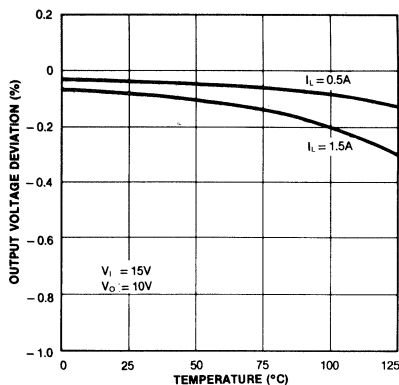


Fig. 2 ADJUSTMENT CURRENT

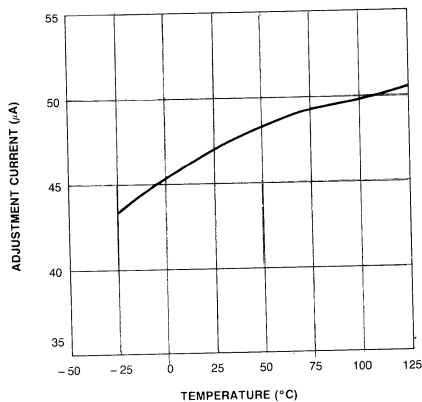


Fig. 3 DROPOUT VOLTAGE

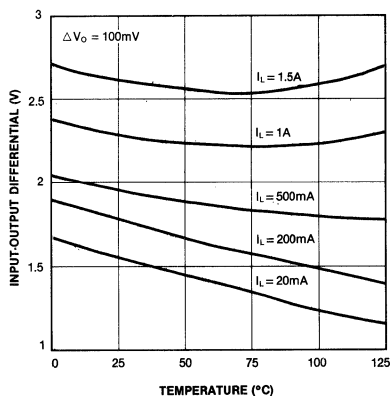
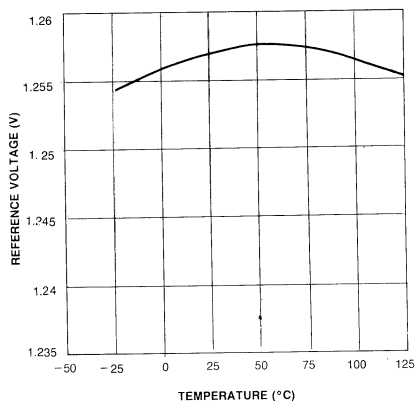
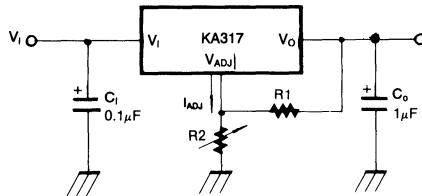


Fig. 4 REFERENCE VOLTAGE



TYPICAL APPLICATIONS

Fig. 5 Programmable Regulator



$$V_O = 1.25V \left(1 + \frac{R_2}{R_1}\right) + I_{ADJ} R_2$$

C_I is required when regulator is located an appreciable distance from power supply filter. C_O is not needed for stability, however, it does improve transient response.

Since I_{ADJ} is controlled to less than $100\mu A$, the error associated with this term is negligible in most applications.

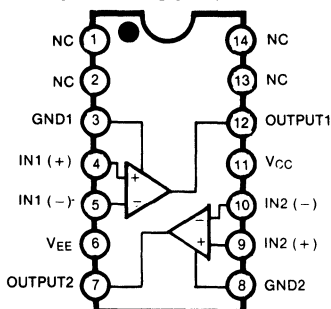
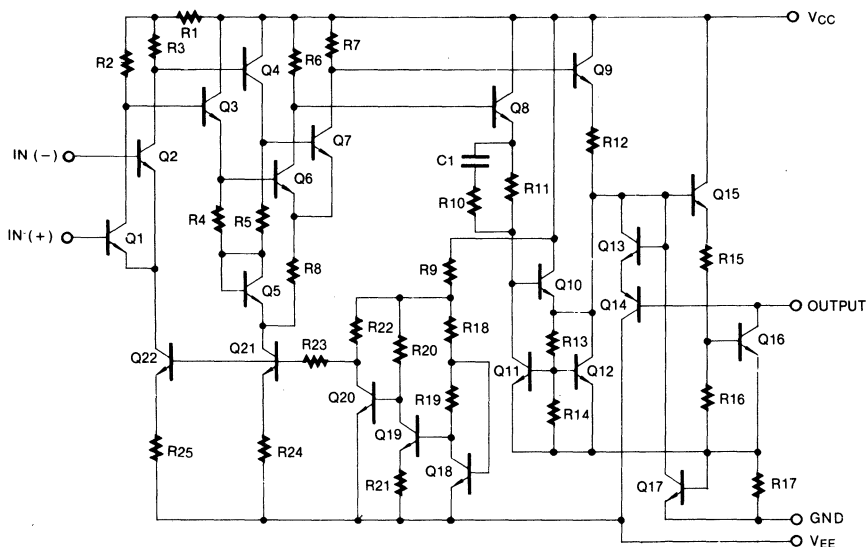
DUAL HIGH SPEED VOLTAGE COMPARATOR

The KA219 is a dual high speed voltage comparator designed to operate from a single +5V supply up to $\pm 15V$ dual supplies.

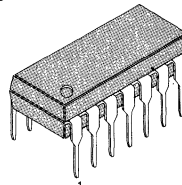
Open collector of the output stage makes the KA219 compatible with RTL, DTL and TTL as well as capable of driving lamps and relays at currents up to 25mA. Typical response time of 80ns with $\pm 15V$ power supplies makes the KA219 ideal for application in fast A/D converts, level shifters, oscillators, and multivibrators.

FEATURES

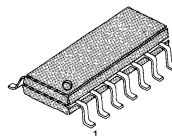
- Operates from a single 5V supply
- Typically 80ns response time at $\pm 15V$
- Open collector outputs: up to +35V
- High output drive current: 25mA
- Inputs and outputs can be isolated from system ground
- Minimum fan-out of 2 (each side)
- Two independent comparators

BLOCK DIAGRAM**SCHEMATIC DIAGRAM**

14 DIP



14 SOP

**ORDERING INFORMATION**

Device	Package	Operating Temperature
KA319	14 DIP	0 ~ +70°C
KA319D	14 SOP	
KA219	14 DIP	-25 ~ +85°C
KA219D	14 SOP	

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	36	V
Output to Negative Supply Voltage	$V_O - V_{EE}$	36	V
Ground to Negative Supply Voltage	V_{EE}	25	V
Ground to Positive Supply Voltage	V_{CC}	18	V
Differential Input Voltage	$V_{I(DIFF)}$	± 5	V
Input Voltage	V_I	± 15	V
Output Short Circuit Duration		10	sec
Power Dissipation	P_D	500	mW
Operating Temperature Range KA219	T_{OPR}	$-25 \sim +85$	$^{\circ}\text{C}$
KA319		$0 \sim +70$	
Storage Temperature Range	T_{STG}	$-65 \sim +150$	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS

(V_{CC} = +15V, V_{EE} = -15V, T_A = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	KA219			KA319			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 1)	V_{IO}	$R_S \leq 5K\Omega$		0.7	4.0		2.0	8.0	mV
		Note 3			7.0			10	
Input Offset Current (Note 1)	I_{IO}			10	75		10	200	nA
		Note 3			100			300	
Input Bias Current	I_{BIAS}			150	500		250	1000	nA
		Note 3			1000			1200	
Voltage Gain	G_V		10	40		8	40		V/mV
Response Time (Note 2)	t_{RES}	$V_{CC} = \pm 15V$		80			80		ns
Saturation Voltage	V_{SAT}	$V_I \leq -5mV, I_O = 25mA$		0.6	1.5				V
		$V_I \leq -10mV, I_O = 25mA$					0.6	1.5	V
		$V_{CC} \geq 4.5V, V_{EE} = 0V$							
		$V_I \leq -6mV, I_{SINK} \leq 3.2mA$		0.23	0.4				V
		$V_{CC} \geq 4.5V, V_{EE} = 0V$ $V_I \leq -10mV, I_{SINK} \leq 3.2mA$					0.3	0.4	V
Output Leakage Current	$I_{O(LKG)}$	$V_I \geq 5mV, V_{O(P)} = 35V$		0.2	2				μA
		Note 3		1	10				
		$V_I \geq 10mV, V_{O(P)} = 35V$					0.2	10	μA
Input Voltage Range	$V_{I(R)}$	Note 3							V
		$V_{CC} = \pm 15V$		± 13			± 13		
		$V_{CC} = 5V, V_{EE} = 0V$	1		3	1		3	

ELECTRICAL CHARACTERISTICS(V_{CC} = +15V, V_{EE} = -15V, T_A = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	KA219			KA319			Unit
			Min	Typ	Max	Min	Typ	Max	
Differential Input Voltage	V _{I(DIFF)}		± 5			± 5			V
Positive Supply Current	I _{CC1}	V _{CC} = 5V, V _{EE} = 0V		3.6			3.6		mA
Positive Supply Current	I _{CC2}	V _{CC} = ± 15V		7.5	11.5		7.5	12.5	mA
Negative Supply Current	I _{EE}	V _{CC} = ± 15V		3	4.5		3	5	mA

Note 1. The offset voltage and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

2. The response time specified is for a 100mV input step with 5mV overdrive.

3. KA319: 0 ≤ T_A ≤ +70°C

KA219: -25 ≤ T_A ≤ +85°C

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1 INPUT CURRENT

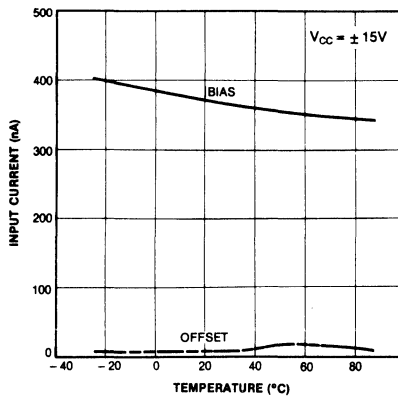


Fig. 2 OUTPUT SATURATION VOLTAGE

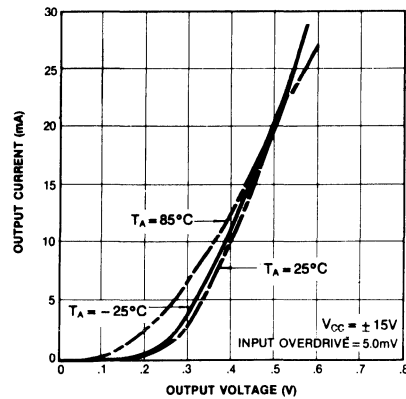


Fig. 3 TRANSFER FUNCTION

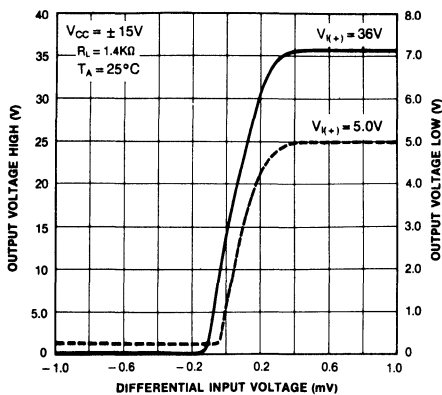


Fig. 4 RESPONSE TIME FOR VARIOUS INPUT OVERDRIVE

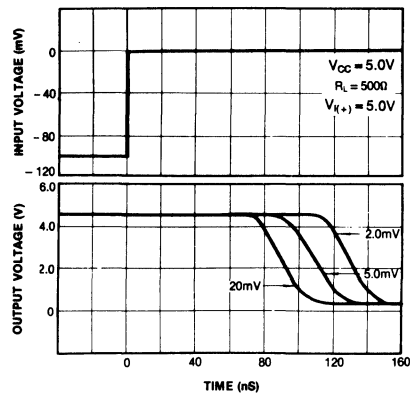


Fig. 5 RESPONSE TIME FOR VARIOUS INPUT OVERDRIVER

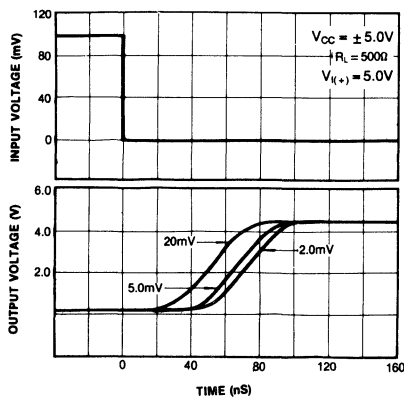


Fig. 6 INPUT CHARACTERISTICS

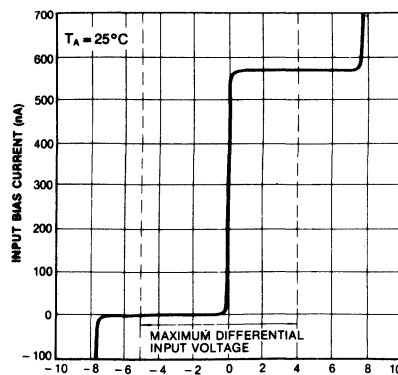


Fig. 7 RESPONSE TIME FOR VARIOUS INPUT OVERDRIVER

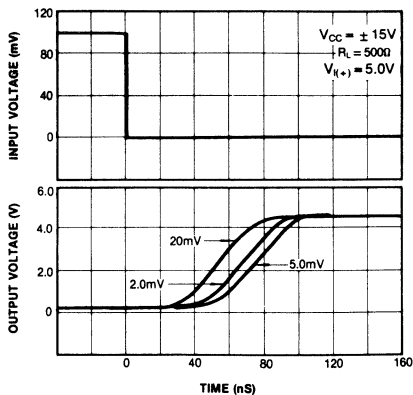


Fig. 8 RESPONSE TIME FOR VARIOUS INPUT OVERDRIVER

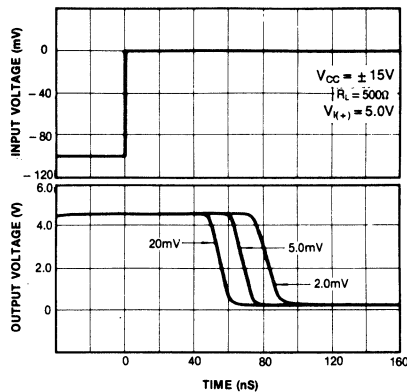


Fig. 9 SUPPLY CURRENT

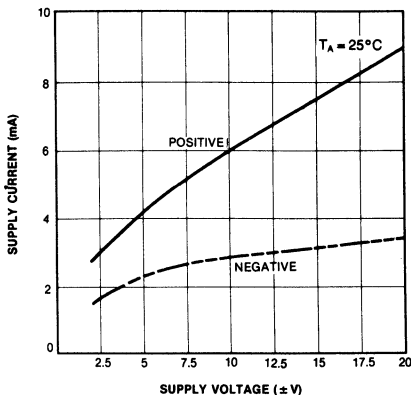


Fig. 10 SUPPLY CURRENT

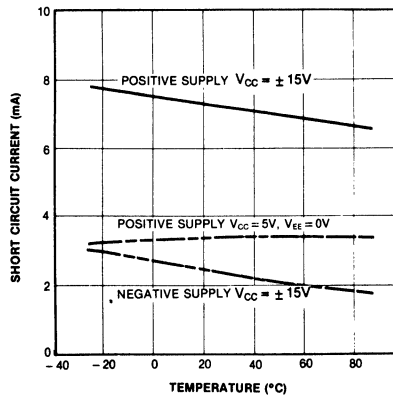


Fig. 11 COMMON MODE LIMITS

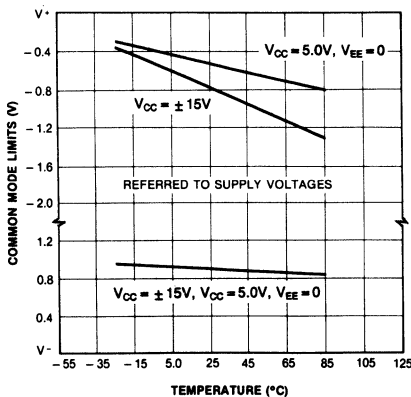
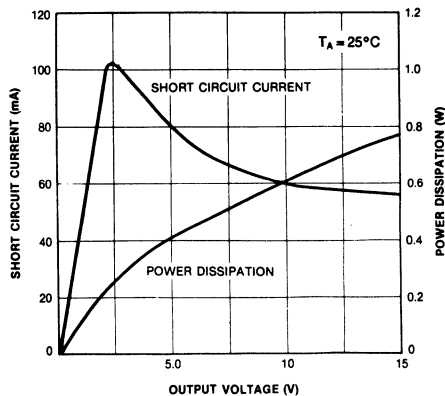


Fig. 12 OUTPUT LIMITING CHARACTERISTICS



QUAD OPERATIONAL AMPLIFIERS

The KA224 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide voltage range.

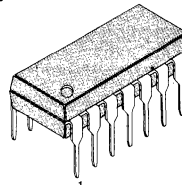
Operation from split power supplies is also possible so long as the difference between the two supplies is 3 volts to 32 volts. voltage.

Application areas include transducer amplifier, DC gain blocks and all the conventional OP amp circuits which now can be easily implemented in single power supply systems.

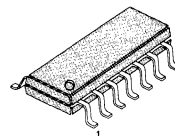
FEATURES

- Internally frequency compensated for unity gain
- Large DC voltage gain: 100dB
- Wide power supply range: KA224/A, KA324/A: 3V ~ 32V (or $\pm 1.5 \sim 15V$)
KA2902: 3V ~ 26V (or $\pm 1.5V \sim 13V$)
- Input common-mode voltage range includes ground
- Large output voltage swing: 0V DC to $V_{CC}-1.5V$ DC
- Power drain suitable for battery operation.

14 DIP

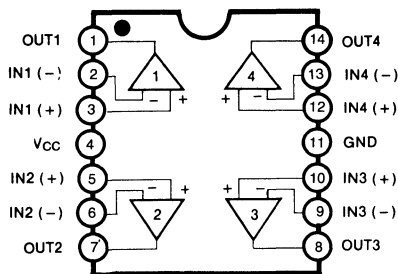


14 SOP

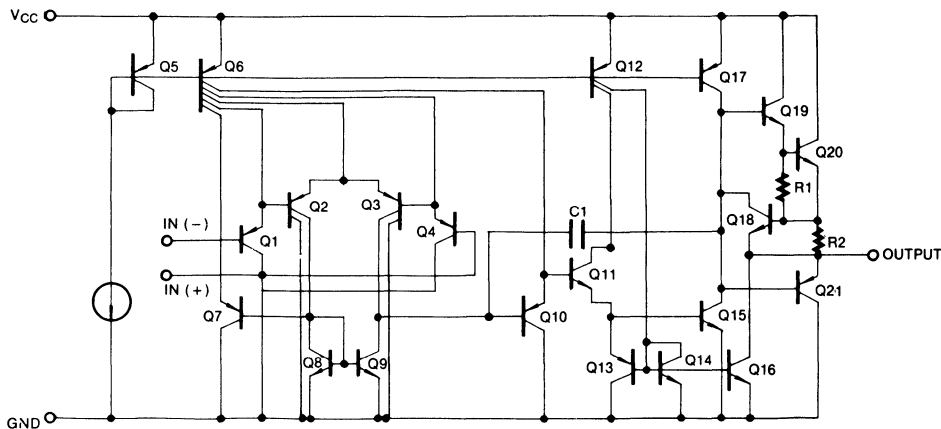


2

BLOCK DIAGRAM



SCHEMATIC DIAGRAM (One Section Only)



ORDERING INFORMATION

Device	Package	Operating Temperature
KA324 KA324A	14 DIP	0 ~ +70°C
KA324D KA324AD	14 SOP	
KA224 KA224A	14 DIP	-25 ~ +85°C
KA224D KA224AD	14 SOP	
KA2902	14 DIP	-40 ~ +85°C
KA2902D	14 SOP	

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	KA224/KA224A	KA324/KA324A	KA2902	Unit
Power Supply Voltage	V_{CC}	± 18 or 32	± 18 or 32	± 13 or 26	V
Differential Input Voltage	$V_{I(DIFF)}$	32	32	26	V
Input Voltage	V_I	-0.3 to +32	-0.3 to +32	-0.3 to +26	V
Output Short Circuit to GND $V_{CC} \leq 15V$ $T_A = 25^\circ C$ (One Amp)		Continuous	Continuous	Continuous	
Power Dissipation	P_D	570	570	570	mW
Operating Temperature Range	T_{OPR}	-25 ~ +85	0 ~ +70	-40 ~ +85	$^\circ C$
Storage Temperature Range	T_{STG}	-65 ~ +150	-65 ~ +150	-65 ~ +150	$^\circ C$

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V, V_{EE} = GND, T_A = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	KA224			KA324			KA2902			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	$V_{CM} = 0V$ to $V_{CC} - 1.5V$ $V_{O(P)} = 1.4V$, $R_S = 0\Omega$		1.5	5.0		1.5	7.0		1.5	7.0	mV
Input Offset Current	I_{IO}			2.0	30		3.0	50		3.0	50	nA
Input Bias Current	I_{BIAS}			40	150		40	250		40	250	nA
Input Common-Mode Voltage Range	$V_{I(R)}$	$V_{CC} = 30V$ ($V_{CC} = 26V$ for KA2902)	0		$V_{CC} - 1.5$	0	$V_{CC} - 1.5$		0		$V_{CC} - 1.5$	V
Supply Current	I_{CC}	$R_L = \infty$, $V_{CC} = 30V$ (all Amps) ($V_{CC} = 26V$ for KA2902)		1.0	3		1.0	3		1.0	3	mA
		$R_L = \infty$, $V_{CC} = 5V$ (all Amps)		0.7	1.2		0.7	1.2		0.7	1.2	mA
Large Signal Voltage Gain	G_V	$V_{CC} = 15V$, $R_L \geq 2K\Omega$ $V_{O(P)} = 1V$ to $11V$	50	100		25	100			100		V/mV
Output Voltage Swing	$V_{O(H)}$	$V_{CC} = 30V$ $V_{CC} = 26V$ for 2902	$R_L = 2K\Omega$	26		26			22			V
			$R_L = 10K\Omega$	27	28		27	28		23	24	V
	$V_{O(L)}$	$V_{CC} = 5V$, $R_L \geq 10K\Omega$		5	20		5	20		5	100	mV
Common-Mode Rejection Ratio	CMRR		70	85		65	75		50	75		dB
Power Supply Rejection Ratio	PSRR		65	100		65	100		50	100		dB
Channel Separation	CS	$f = 1KHz$ to $20KHz$		120			120			120		dB
Short Circuit to GND	I_{SC}			40	60		40	60		40	60	mA
Output Current	I_{SOURCE}	$V_{I(+)} = 1V$, $V_{I(-)} = 0V$ $V_{CC} = 15V$, $V_{O(P)} = 2V$	20	40		20	40		20	40		mA
	I_{SINK}	$V_{I(+)} = 0V$, $V_{I(-)} = 1V$ $V_{CC} = 15V$, $V_{O(P)} = 2V$	10	13		10	13		10	13		mA
		$V_{I(+)} = 0V$, $V_{I(-)} = 1V$ $V_{CC} = 15V$, $V_{O(P)} = 200mV$	12	45		12	45					μA
Differential Input Voltage	$V_{I(DIFF)}$				V_{CC}			V_{CC}			V_{CC}	V

ELECTRICAL CHARACTERISTICS(V_{CC} = 5.0V, V_{EE} = GND, unless otherwise specified)The following specification apply over the range of -25°C ≤ T_A ≤ +85°C for the KA224; and the 0°C ≤ T_A + 70°C for the KA324; and the -40°C ≤ T_A ≤ +85°C for the KA2902

Characteristic	Symbol	Test Conditions	KA224			KA324			KA2902			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V _{IO}	V _{ICM} = 0V to V _{CC} - 1.5V V _{O(P)} = 1.4V, R _S = 0Ω			7.0			9.0			10.0	mV
Input Offset Voltage Drift	ΔV _{IO} /ΔT			7.0			7.0			7.0		μV/°C
Input Offset Current	I _{IO}				100			150			200	nA
Input Offset Current Drift	ΔI _{IO} /ΔT			10			10			10		pA/°C
Input Bias Current	I _{BIAS}				300			500			500	nA
Input Common-Mode Voltage Range	V _{IC(R)}	V _{CC} = 30V (V _{CC} = 26V for LM2902)	0		V _{CC} - 2.0	0		V _{CC} - 2.0	0		V _{CC} - 2.0	V
Large Signal Voltage Gain	G _V	V _{CC} = 15V, R _L ≥ 2.0KΩ V _{O(P)} = 1V to 11V	25			15			15			V/mV
Output Voltage Swing	V _{O(H)}	V _{CC} = 30V V _{CC} = 26V for 2902	R _L = 2KΩ 26			26			22			V
	V _{O(L)}		R _L = 10KΩ 27	28		27	28		23	24		V
Output Current	I _{SOURCE}	V _{I(+)} = 1V, V _{I(-)} = 0V V _{CC} = 15V, V _{O(P)} = 2V	10	20		10	20		10	20		mA
	I _{SINK}	V _{I(+)} = 0V, V _{I(-)} = 1V V _{CC} = 15V, V _{O(P)} = 2V	10	13		5	8		5	8		mA
Differential Input Voltage	V _{I(DIFS)}				V _{CC}			V _{CC}			V _{CC}	V

ELECTRICAL CHARACTERISTICS(V_{CC} = 5.0V, V_{EE} = GND, T_A = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	KA224A			KA324A			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V _{IO}	V _{CM} = 0V to V _{CC} - 1.5V V _{O(P)} = 1.4V, R _S = 0		1.0	3.0		1.5	3.0	mV
Input Offset Current	I _{IO}			2	15		3.0	30	nA
Input Bias Current	I _{BIAS}			40	80		40	100	nA
Input Common-Mode Voltage Range	V _{I(R)}	V _{CC} = 30V	0		V _{CC} - 1.5	0		V _{CC} - 1.5	V
Supply Current (All Amps)	I _{CC}	V _{CC} = 30V		1.5	3		1.5	3	mA
		V _{CC} = 5V		0.7	1.2		0.7	1.2	mA
Large Signal Voltage Gain	G _V	V _{CC} = 15V, R _L ≥ 2KΩ V _{O(P)} = 1V to 11V	50	100		25	100		V/mV
Output Voltage Swing	V _{O(H)}	V _{CC} = 30V V _{CC} = 26V for 2902	R _L = 2KΩ 26			26			V
			R _L = 10KΩ 27	28		27	28		V
	V _{O(L)}	V _{CC} = 5V, R _L ≥ 10KΩ		5	20		5	20	mV
Common-Mode Rejection Ratio	CMRR		70	85		65	85		dB
Power Supply Rejection Ratio	PSRR		65	100		65	100		dB
Channel Separation	CS	f = 1KHz to 20KHz		120			120		dB
Short Circuit to GND	I _{SC}			40	60		40	60	mA
Output Current	I _{SOURCE}	V _{I(+)} = 1V, V _{I(-)} = 0V V _{CC} = 15V	20	40		20	40		mA
	I _{SINK}	V _{I(+)} = 0V, V _{I(-)} = 1V V _{CC} = 15V, V _{O(P)} = 2V	10	20		10	20		mA
		V _{I(+)} = 0V, V _{I(-)} = 1V V _{CC} = 15V, V _{O(P)} = 200mV	12	50		12	50		μA
Differential Input Voltage	V _{I(DIFF)}				V _{CC}			V _{CC}	V

ELECTRICAL CHARACTERISTICS(V_{CC} = 5.0V, V_{EE} = GND, unless otherwise specified)The following specification apply over the range of -25°C ≤ T_A + 85°C for the KA224A; and the 0°C ≤ T_A ≤ +70°C for the KA324A

Characteristic	Symbol	Test Conditions	KA224A			KA324A			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V _{IO}	V _{CM} = 0V to V _{CC} -1.5V V _{O(P)} = 1.4V R _S = 0Ω			4.0			5.0	mV
Input Offset Voltage Drift	ΔV _{IO} /ΔT			7.0	20		7.0	30	μV/°C
Input Offset Current	I _{IO}				30			75	nA
Input Offset Current Drift	ΔI _{IO} /ΔT			10	200		10	300	pA/°C
Input Bias Current	I _{BIAS}			40	100		40	200	nA
Input Common-Mode Voltage Range	V _{I(R)}	V _{CC} = 30V	0		V _{CC} -2.0	0		V _{CC} -2.0	V
Large Signal Voltage Gain	G _V	V _{CC} = 15V R _L ≥ 2.0KΩ	25			15			V/mV
Output Voltage Swing	V _{O(P-P)}	V _{CC} = 30V R _L = 2KΩ	26			26			V
		R _L = 10KΩ	27	28		27	28		
		V _{CC} = 5V R _L ≤ 10KΩ		5	20		5	20	mV
Output Current	I _{SOURCE}	V _{I(+)} = 1V V _{I(-)} = 0V V _{CC} = 15V	10	20		10	20		mA
	I _{SINK}	V _{I(+)} = 0V V _{I(-)} = 1V V _{CC} = 15V	5	8		5	8		mA
Differential Input Voltage	V _{I(DIFF)}				V _{CC}			V _{CC}	V

Fig. 1 INPUT VOLTAGE RANGE

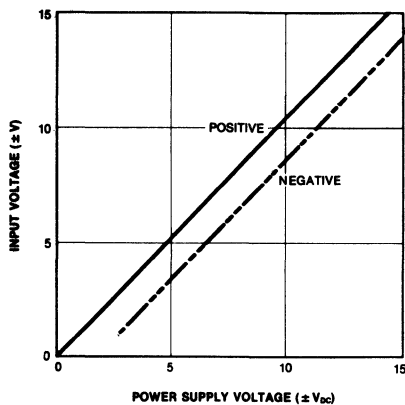


Fig. 2 INPUT CURRENT

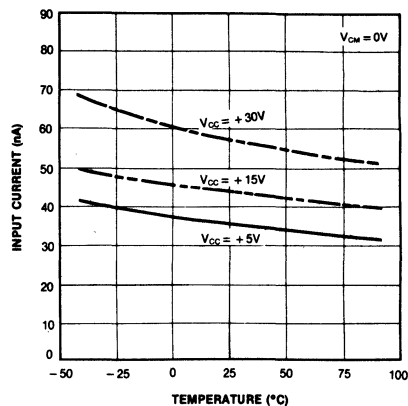


Fig. 3 SUPPLY CURRENT

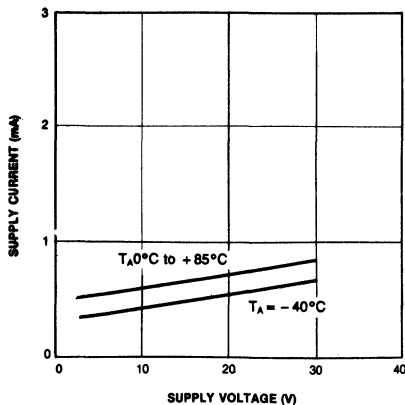


Fig. 4 VOLTAGE GAIN

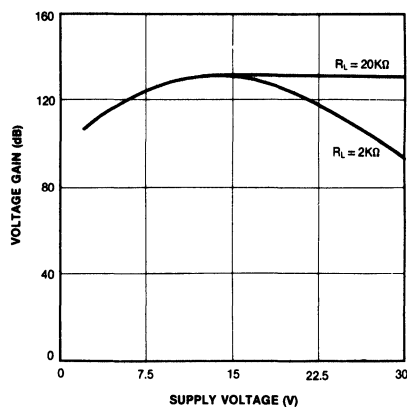


Fig. 5 OPEN LOOP FREQUENCY RESPONSE

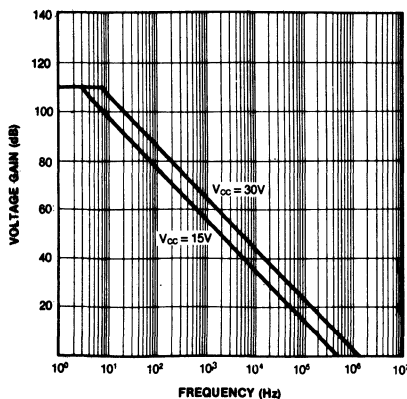
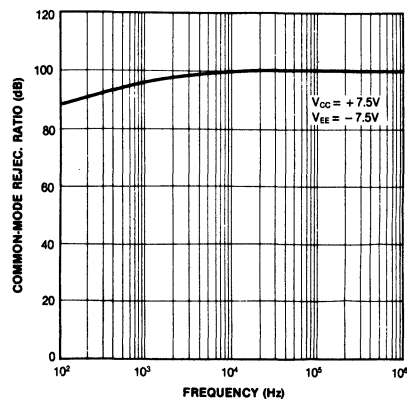


Fig. 6 COMMON-MODE REJECTION RATIO



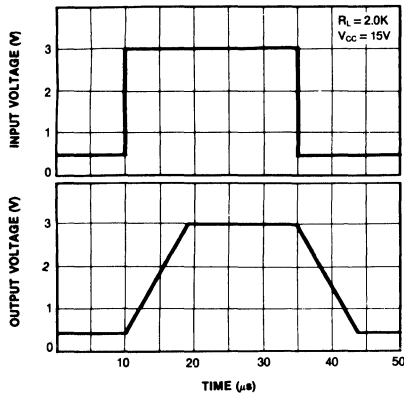


Fig. 9 LARGE SIGNAL FREQUENCY RESPONSE

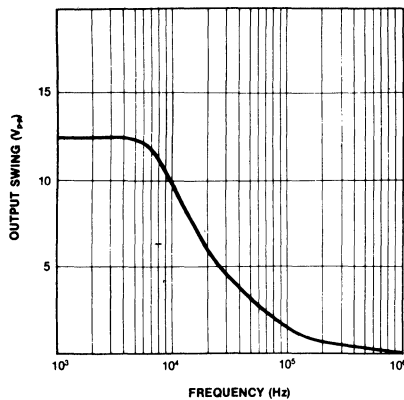


Fig. 11 OUTPUT CHARACTERISTICS CURRENT SINKING

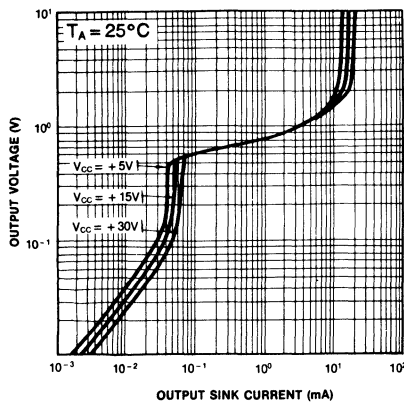


Fig. 8 VOLTAGE FOLLOWER PULSE RESPONSE (SMALL SIGNAL)

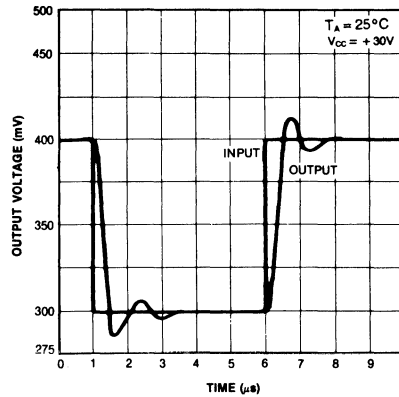


Fig. 10 OUTPUT CHARACTERISTICS CURRENT SOURCING

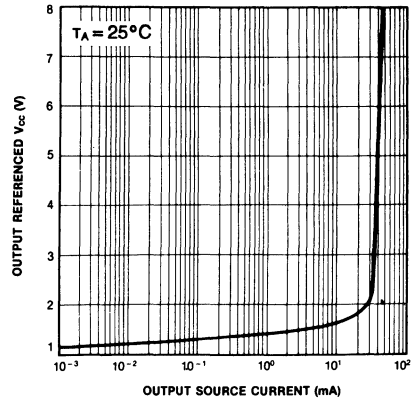
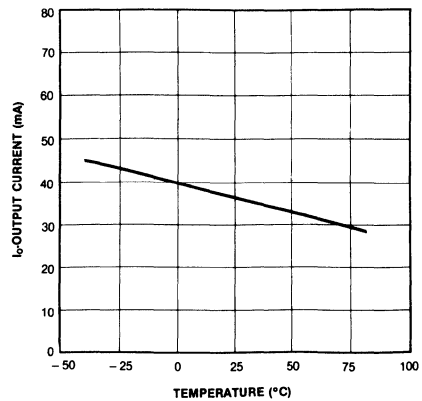


Fig. 12 CURRENT LIMITING

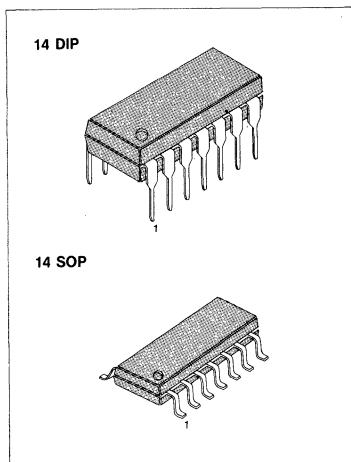


QUAD DIFFERENTIAL COMPARATOR

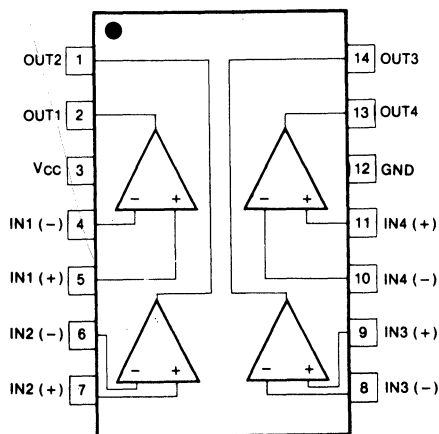
The KA239 series consists of four independent voltage comparators designed to operate from single power supply over a wide voltage range.

FEATURES

- Single or dual supply operation
- Wide range of supply voltages KA239/A, KA339/A: 2 ~ 36V
KA2901 (or $\pm 1 \sim \pm 18V$)
KA3302: 2 ~ 28V
(or $\pm 1 \sim \pm 14V$)
- Low supply current drain 800 μ A Typ.
- Open collector outputs for wired and connectors
- Low input bias current 25nA Typ.
- Low input offset current $\pm 2.3nA$ Typ.
- Low input offset voltage $\pm 1.4mV$ Typ.
- Common mode input voltage range includes ground.
- Low output saturation voltage
- Output compatible with TTL, DTL and MOS logic system



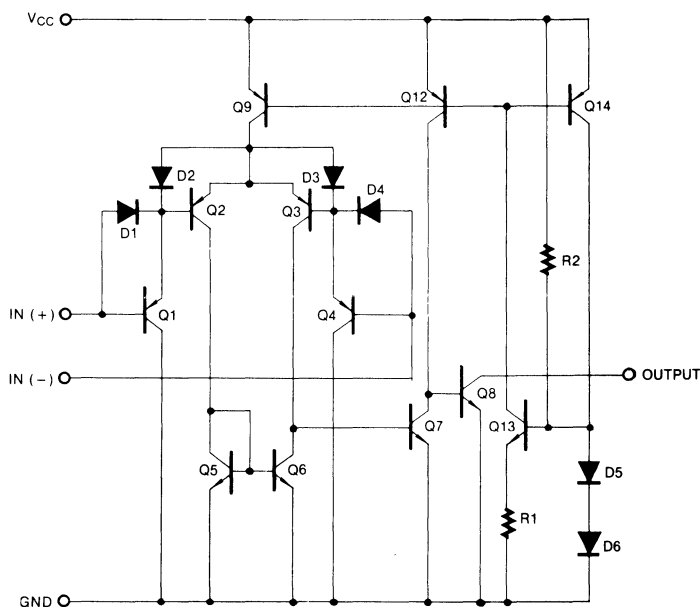
BLOCK DIAGRAM



ORDERING INFORMATION

Device	Package	Operating Temperature
KA339 KA339A	14 DIP	0 ~ 70°C
KA339D KA339AD	14 SOP	
KA239 KA239A	14 DIP	- 25 ~ + 85°C
KA239D KA239AD	14 SOP	
KA2901 KA2901D KA3302N KA3302D	14 DIP 14 SOP 14 DIP 14 SOP	0 ~ + 85°C

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	± 18 or 36	V
Supply Voltage Only KA3302	V_{CC}	± 14 or 28	V
Differential Input Voltage	$V_{I(DIFF)}$	36	V
Differential Input Voltage Only KA3302	$V_{I(DIFF)}$	28	V
Input Voltage	V_I	-0.3 to $+36$	V
Input Voltage Only KA3302	V_I	-0.3 to $+28$	V
Output Short Circuit to GND		Continuous	
Power Dissipation	P_D	570	mW
Operating Temperature KA239/KA239A		$0 \sim +70$	$^{\circ}\text{C}$
KA339/KA339A	T_{OPR}	$-25 \sim +85$	$^{\circ}\text{C}$
KA2901/KA3302		$-40 \sim +85$	$^{\circ}\text{C}$
Storage Temperature	T_{STG}	$-65 \sim +150$	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, T_A = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	KA239A/KA339A			KA239/KA339			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V _{IO}	V _{CM} = 0V to V _{CC} - 1.5V		±1	±2		±1.4	±5	mV
		V _{O(P)} = 1.4V, R _S = 0 NOTE 1			±4.0			±9.0	
Input Offset Current	I _{IO}			±2.3	±50		±2.3	±50	nA
		NOTE 1			±150			±150	
Input Bias Current	I _{BIAS}			57	250		57	250	nA
		NOTE 1			400			400	
Input Common Mode Voltage Range	V _{I(R)}		0		V _{CC} -1.5	0		V _{CC} -1.5	V
		NOTE 1	0		V _{CC} -2	0		V _{CC} -2	
Supply Current	I _{CC}	R _L = ∞		1.1	2.0		1.1	2.0	mA
Voltage Gain	G _V	V _{CC} = 15V, R _L ≥ 15KΩ (for large swing)	50	200		50	200		V/mV
Large Signal Response Time	t _{RES}	V _I = TTL Logic Swing V _{REF} = 1.4V, V _{RL} = 5V, R _L = 5.1KΩ		350			350		ns
Response Time	t _{RES}	V _{RL} = 5V, R _L = 5.1KΩ		1.4			1.4		μs
Output Sink Current	I _{SINK}	V _{I(-)} ≥ 1V, V _{I(+)} = 0V, V _{O(P)} ≤ 1.5V	6	18		6	18		mA
Output Saturation Voltage	V _{SAT}	V _{I(-)} ≥ 1V, V _{I(+)} = 0V		140	400		140	400	mV
		I _{SINK} = 4mA NOTE 1			700			700	
Output Leakage Current	I _{O(LKG)}	V _{I(-)} = 0		0.1			0.1		nA
		V _{I(+)} = 1V			1.0			1.0	μA
Differential Voltage	V _{I(DIFF)}	NOTE 1			36			36	V

* NOTE 1

KA339/A: 0 ≤ T_A ≤ +70°CKA239/A: -25 ≤ T_A ≤ +85°CKA2901/3302: -40 ≤ T_A < +85°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, T_A = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	KA2901			KA3302			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V _{IO}	V _{CM} = 0V to V _{CC} - 1.5V		2	7		2	20	mV
		V _{O(P)} = 1.4V, R _S = 0 NOTE 1		9	15			40	
Input Offset Current	I _{IO}			2.3	50		3	100	nA
		NOTE 1		50	200			300	
Input Bias Current	I _{BIAS}			57	250		57	250	nA
		NOTE 1		200	500			1000	
Input Common Mode Voltage Range	V _{IC(R)}		0		V _{CC} -1.5	0		V _{CC} -1.5	V
		NOTE 1	0		V _{CC} -2	0		V _{CC} -2	
Supply Current	I _{CC}	R _L = ∞ ,		1.1	2.0		1.1	2.0	mA
		R _L = ∞ , V _{CC} = 30V		1.6	2.5				
Voltage Gain	G _V	V _{CC} = 15V, R _L ≥ 15KΩ (for large swing)	25	100		2	30		V/mV
Large Signal Response Time	t _{RES}	V _I = TTL Logic Swing V _{REF} = 1.4V, V _{RL} = 5V, R _L = 5.1KΩ		350			350		ns
Response Time	t _{RES}	V _{RL} = 5V, R _L = 5.1KΩ		1.4			1.4		μs
Output Sink Current	I _{SINK}	V _{I(-)} ≥ 1V, V _{I(+)} = 0V, V _{O(P)} ≤ 1.5V	6	18		6	18		mA
Output Saturation Voltage	V _{SAT}	V _{I(-)} ≥ 1V, V _{I(+)} = 0V		140	400		140	400	mV
		I _{SINK} = 4mA NOTE 1			700			700	
Output Leakage Current	I _{O(LKG)}	V _{I(+)} = 0		0.1			0.1		nA
		V _{I(-)} = 1V			1.0			1.0	μA
Differential Voltage	V _{I(DIFF)}	NOTE 1	0		36			28	V

NOTE 1 KA339/A: 0 ≤ T_A ≤ +70°CKA239/A: -25 ≤ T_A +85°CKA2901/3302: -40 ≤ T_A < +85°C

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1 SUPPLY CURRENT

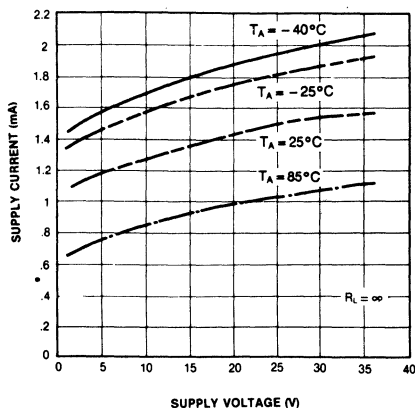


Fig. 2 INPUT CURRENT

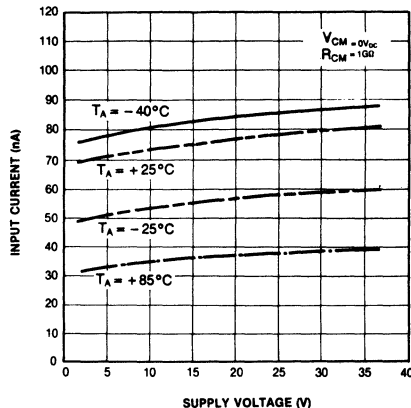


Fig. 3 OUTPUT SATURATION VOLTAGE

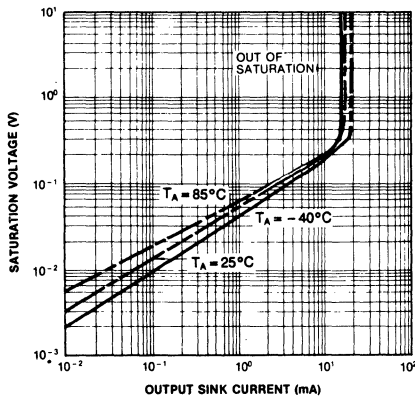


Fig. 4 RESPONSE TIME FOR VARIOUS INPUT OVERDRIVE-NEGATIVE TRANSITION

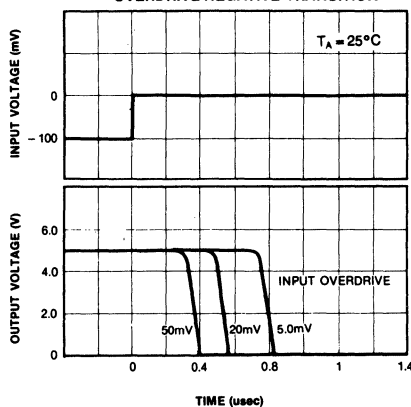
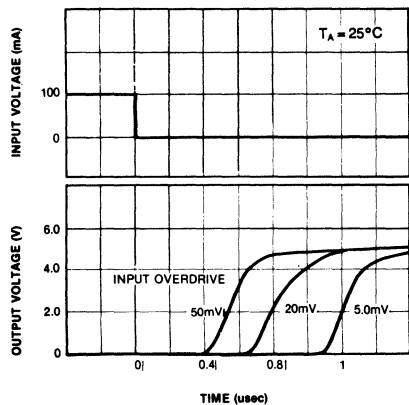


Fig. 5 RESPONSE TIME FOR VARIOUS INPUT OVERDRIVE-POSITIVE TRANSITION



DC TO DC CONVERTER CONTROLLER

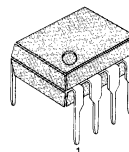
The KA34063A is a monolithic regulator subsystem intended for use as DC to DC converter. This device contains a temperature compensated bandgap reference, a duty-cycle control oscillator, driver and high current output switch.

It can be used for step down, step-up or inverting switching regulators as well as for series pass regulators.

FEATURES

- Operation From 3.0 to 40V Input
- Short Circuit Current Limiting
- Low Standby Current
- Output Switch Current of 1.5A Without External Transistors
- Output Voltage Adjustable
- Frequency Of Operation From 100Hz to 100KHz
- Step-Up, Step-Down or Inverting Switching Regulators

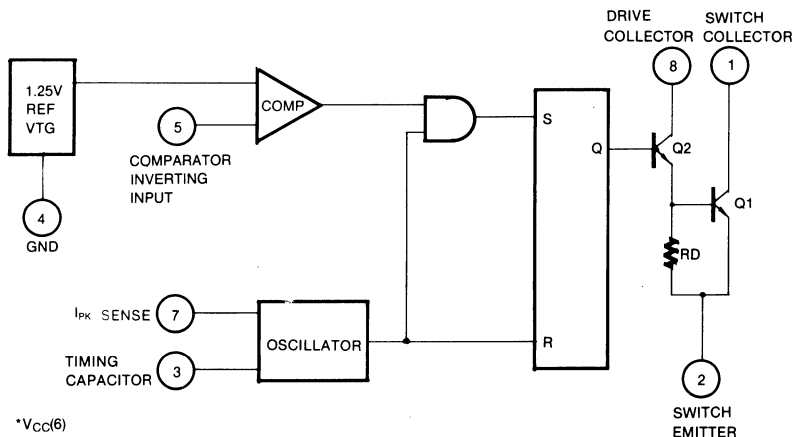
8 DIP



ORDERING INFORMATION

Device	Package	Operating Temperature
KA34063A	8DIP	0 ~ +70°C

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	40	V
Comparator Input Voltage Range	$V_{I(Comp)}$	-0.3 ~ +40	V
Switch Collector Voltage	$V_C (SW)$	40	V
Switch Emitter Voltage	$V_E (SW)$	40	V
Switch Collector To Emitter Voltage	$V_{CE (SW)}$	40	V
Driver Collector Voltage	$V_{C(DR)}$	40	V
Switch Current	I_{SW}	1.5	A

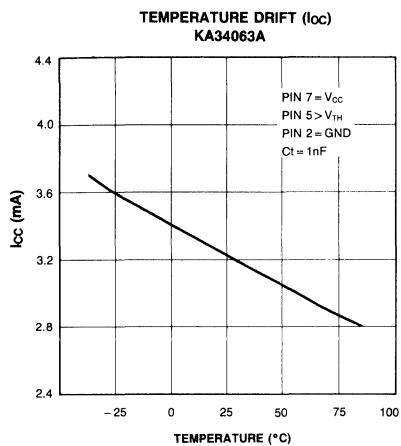
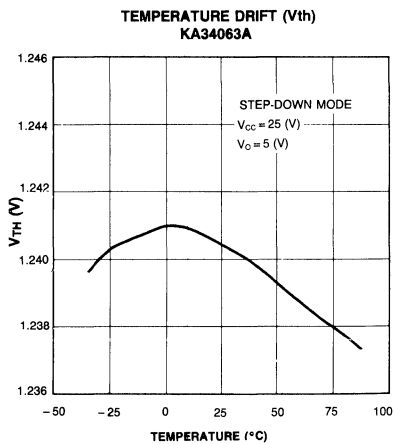
ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V, T_A = 0°C to +70°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
OSCILLATOR						
Charging Current	CHG	V _{CC} = 5 to 40V T _A = 25°C	22	31	42	μA
Discharging Current	I _{DISCHG}	V _{CC} = 5 to 40V T _A = 25°C	140	190	260	μA
Oscillator Amplitude	V _{I(OSC)}	T _A = 25°C		0.5		V
Discharge To Charge Current Ratio	K	V ₇ = V _{CC} T _A = 25°C	5.2	6.1	7.5	
Current Limit Sense Voltage	V _{SENSE(C.L)}	I _{CHG} = I _{DISCHG} T _A = 25°C	250	300	350	mV
OUTPUT SWITCH						
Saturation Voltage 1 (Note)	V _{CE(SAT)1}	I _{SW} = 1.0A, V _{C (driver)} = V _{C (SW)}		0.95	1.3	V
Saturation Voltage 2 (Note)	V _{CE(SAT)2}	I _{SW} = 1.0A, V _{C (driver)} = 50mA		0.45	0.7	V
DC Current Gain (Note)	G _{I(DC)}	I _{SW} = 1.0A, V _{CE} = 5.0V, T _A = 25°C	50	180		
Collector off State Current (Note)	α _(OFF)	V _{CE} = 40V, T _A = 25°C		10	100	nA
COMPARATOR						
Threshold Voltage	V _{TH}		1.21	1.24	1.29	V
Threshold Voltage Line Regulation	ΔV _{TH}	V _{CC} = 3 to 40V		2.0	5.0	mV
Input Bias Current	I _{BIAS}	V _I = 0V		50	400	nA
TOTAL DEVICE						
Supply Current	I _{CC}	V _{CC} = 5 to 40V C _T = 0.001μF V ₇ = V _{CC} V _S > V _{TH} pin2 = GND		2.7	4.0	mA

(Note)

Output switch tests are performed under pulsed conditions to minimize power dissipation.



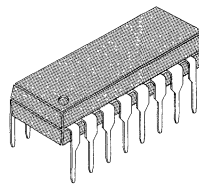
VOLTAGE-MODE PWM CONTROLLER

The KA3525A is a monolithic integrated circuit that included all of the control circuit necessary for a pulse width modulating regulator. There are a voltage reference, an error amplifier, a pulse width modulator, an oscillator, under-voltage lockout, soft start circuit, and output drivers in the chip.

FEATURES

- $5V \pm 1\%$ Reference
- Oscillator Sync Terminal
- Internal Soft Start
- Deadtime Control
- Under-Voltage Lockout

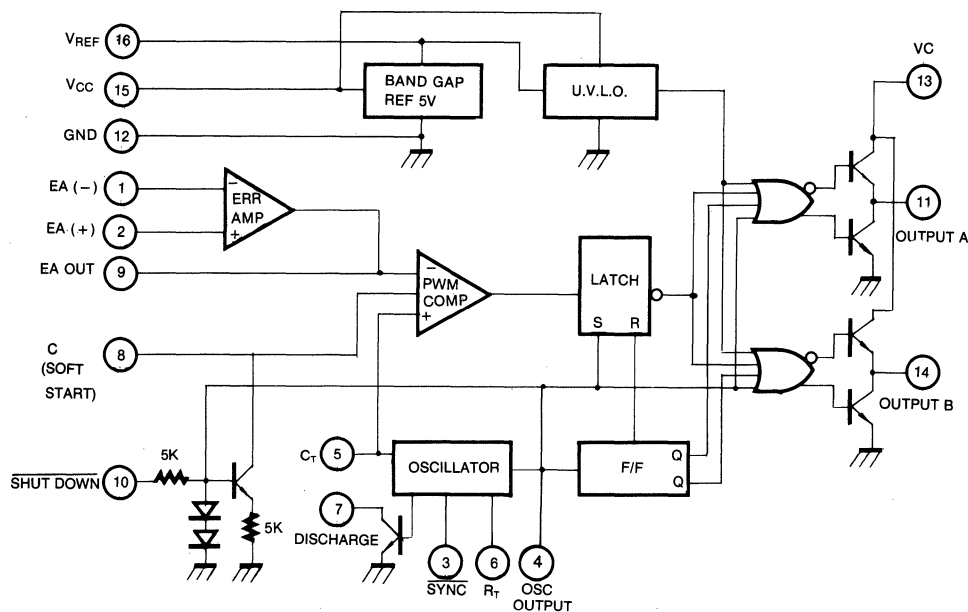
16 DIP



ORDERING INFORMATION

Device	Package	Operating Temperature
KA3525A	16 DIP	0 ~ +70°C

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	40	V
Collector Supply Voltage	V_C	40	V
Output Current, Sink or Source	I_O	500	mA
Reference Output Current	I_{REF}	50	mA
Oscillator Charging Current	$I_{CHG(OSC)}$	5	mA
Power Dissipation ($T_A = 25^\circ\text{C}$)	P_D	1000	mW
Operating Temperature	T_{OPR}	$0 \sim +70$	$^\circ\text{C}$
Storage Temperature	T_{STG}	$-65 \sim +150$	$^\circ\text{C}$
Lead Temperature (Soldering, 10 sec)	T_{LEAD}	+300	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS

(V_{CC} = 20V, T_A = 0°C to +70°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
REFERENCE SECTION						
Reference Output Voltage	V_{REF}	$T_J = 25^\circ\text{C}$	5.0	5.1	5.2	V
Line Regulation	ΔV_{REF}	$V_{CC} = 8 \text{ to } 35\text{V}$		9	20	mV
Load Regulation	ΔV_{REF}	$I_{REF} = 0 \text{ to } 20\text{mA}$		20	50	mV
Short Circuit Output Current	I_{SC}	$V_{REF} = 0, T_J = 25^\circ\text{C}$		80	100	mA
Total Output Variation (Note 1)	ΔV_{REF}	Line, Load and Temperature	4.95		5.25	V
Temperature Stability (Note 1)	ST_T			20	50	mV
Long Term Stability (Note 1)	ST	$T_J = 125^\circ\text{C}, 1 \text{ KHrs}$		20	50	mV
OSCILLATOR SECTION						
Initial Accuracy (Note 1, 2)	ACCUR	$T_J = 25^\circ\text{C}$		± 3	± 6	%
Frequency Change With Voltage	$\Delta f/\Delta V_{CC}$	$V_{CC} = 8 \text{ to } 35\text{V}$ (Note 1, 2)		± 0.8	± 2	%
Maximum Frequency	$f_{(MAX)}$	$R_T = 2\text{K}\Omega, C_T = 470\text{pF}$	400	430		KHz
Minimum Frequency	$f_{(MIN)}$	$R_T = 200\text{K}\Omega, C_T = 0.1\mu\text{F}$		60	120	Hz
Clock Amplitude (Note 1, 2)	$V_{(CLK)}$		3	4		V
Clock Width (Note 1, 2)	$t_{W(CLK)}$	$T_J = 25^\circ\text{C}$	0.3	0.6	1	μs
Sync Threshold	$V_{TH(SYNC)}$		1.2	2	2.8	V
Sync Input Current	$I_{I(SYNC)}$	Sync = 3.5V		1.3	2.5	mA

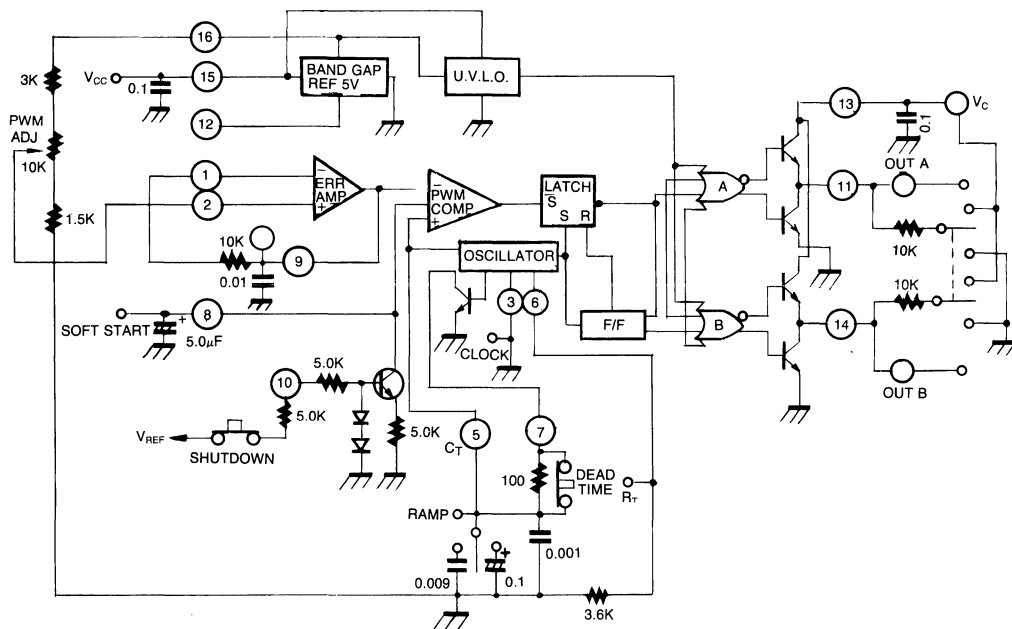
ELECTRICAL CHARACTERISTICS(V_{CC} = 20V, T_A = 0°C to +70°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
ERROR AMPLIFIER SECTION (V _{CM} = 5.1V)						
Input Offset Voltage	V _{IO}			1.5	10	mV
Input Bias Current	I _{BIAS}			1	10	μA
Input Offset Current	I _{IO}			0.1	1	μA
Open Loop Voltage Gain	G _{VO}	R _L ≥ 10MΩ	60	80		dB
Common Mode Rejection Ratio	CMRR	V _{CM} = 1.5 to 5.2V	60	90		dB
Power Supply Rejection Ratio	PSRR	V _{CC} = 8 to 3.5V	50	60		dB
PWM COMPARATOR SECTION						
Minimum Duty Cycle	D _(MIN)				0	%
Maximum Duty Cycle	D _(MAX)		45	49		%
Input Threshold Voltage (Note 2)	V _{TH1}	Zero Duty Cycle	0.7	0.9		V
Input Threshold Voltage (Note 2)	V _{TH2}	Max Duty Cycle		3.2	3.6	V
SOFT-START SECTION						
Soft Start Current	I _{SOFT}	V _{SD} = 0V, V _{SS} = 0V	25	51	80	μA
Soft Start Low Level Voltage	V _{SL}	V _{SD} = 25V		0.3	0.7	V
Shutdown Threshold Voltage	V _{TH(SD)}		0.6	0.8	1	V
Shutdown Input Current	I _{I(SD)}	V _{SD} = 2.5V		0.3	1	mA
OUTPUT SECTION						
Low Output Voltage I	V _{OL I}	I _{SINK} = 20mA		0.1	0.4	V
Low Output Voltage II	V _{OL II}	I _{SINK} = 100mA		0.05	2	V
High Output Voltage I	V _{OH I}	SOURCE = 20mA	18	19		V
High Output Voltage II	V _{OH II}	I _{SOURCE} = 100mA	17	18		V
Under Voltage Lockout	V _{UV}	V _B and V _g = High	6	7	8	V
Collector Leakage Current	I _{LKG}	V _{CC} = 35V		80	200	μA
Rise Time (Note 1)	t _R	C _L = 1μF, T _J = 26°C		80	600	nS
Fall Time (Note 1)	t _F	C _L = 1μF, T _J = 25°C		70	300	nS
STANDBY CURRENT						
Supply Current	I _{CC}	V _{CC} = 35V		12	20	mA

(Note)

- These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production
- Tested at f_{OSC} = 40 KHz (R_T = 3.6K, C_T = 0.01μF, R_D = 0Ω)

2



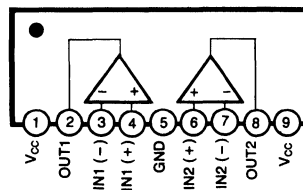
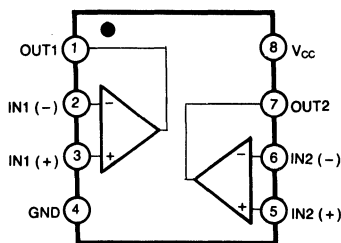
DUAL OPERATIONAL AMPLIFIERS

The KA258 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltage. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. Application areas include transducer amplifier, DC gain blocks and all the conventional OP amp circuits which now can be easily implemented in single power supply systems.

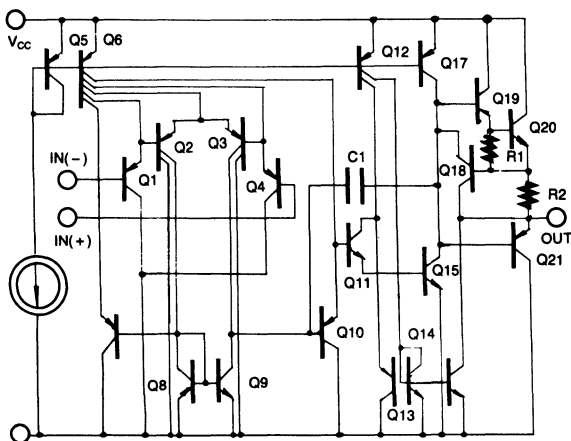
FEATURES

- Internally frequency compensated for unity gain
- Large DC voltage gain: 100dB
- Wide power supply range: KA258/A, KA358/A: 3V ~ 32V
(or $\pm 1.5V \sim 16V$)
KA2904: 3V ~ 26V (or $\pm 1.5V \sim \pm 13V$)
- Input common-mode voltage range includes ground
- Large output voltage swing: 0V DC to $V_{CC} - 1.5V$ DC
- Power drain suitable for battery operation.

BLOCK DIAGRAM



SCHEMATIC DIAGRAM (One section only)



ORDERING INFORMATION

Device	Package	Operating Temperature
KA358 KA358A	8 DIP	0 ~ +70°C
KA358S KA358AS	9 SIP	
KA358D KA358AD	8 SOP	-25 ~ +85°C
KA258 KA258A	8 DIP	
KA258S KA258AS	9 SIP	
KA258D KA258AD	8 SOP	
KA2904	8DIP	-40 ~ +85°C
KA2904S	9 SIP	
KA2904D	8SOP	

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	KA258/KA258A	KA358/KA358A	KA2904	Unit
Supply Voltage	V_{CC}	± 16 or 32	± 16 or 32	± 13 or 26	V
Differential Input Voltage	$V_{I(DIFF)}$	± 32	± 32	± 26	V
Input Voltage	V_I	-0.3 to +32	-0.3 to +32	-0.3 to +26	V
Output Short Circuit to GND $V_{CC} \leq V$ $T_A = 25^\circ\text{C}$ (One Amp)		Continuous	Continuous	Continuous	
Operating Temperature Range	T_{OPR}	-25 ~ +85	0 ~ +70	-40 ~ +85	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-65 ~ +150	-65 ~ +150	-65 ~ +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V, V_{EE} = GND, T_A = 25 $^\circ\text{C}$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	KA258			KA358			KA2904			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	$V_{CM} = 0\text{V}$ to $V_{CC} - 1.5\text{V}$ $V_{O(P)} = 1.4\text{V}$, $R_S = 0\Omega$		2.9	5.0		2.9	7.0		2.9	7.0	mV
Input Offset Current	I_{IO}			3	30		5	50		5	50	nA
Input Bias Current	I_{BIAS}			45	150		45	250		45	250	nA
Input Common-Mode Voltage Range	$V_{I(R)}$	$V_{CC} = 30\text{V}$ (KA2904, $V_{CC} = 26\text{V}$)	0		$V_{CC} - 1.5$	0		$V_{CC} - 1.5$	0		$V_{CC} - 1.5$	V
Supply Current	I_{CC}	$R_L = \infty$, $V_{CC} = 30\text{V}$ (KA2902, $V_{CC} = 26\text{V}$)		0.8	2.0		0.8	2.0		0.8	2.0	mA
		$R_L = \infty$, over full temperature range		0.5	1.2		0.5	1.2		0.5	1.2	mA
Large Signal Voltage Gain	G_V	$V_{CC} = 15\text{V}$, $R_L \geq 2\text{K}\Omega$ $V_{O(P)} = 1\text{V}$ to 11V	50	100		25	100		25	100		V/mV
Output Voltage Swing	$V_{O(H)}$ $V_{O(L)}$	$V_{CC} = 30\text{V}$ $R_L = 2\text{K}\Omega$	26			26			22			V
		$V_{CC} = 26\text{V}$ for 2904 $R_L = 10\text{K}\Omega$	27	28		27	28		23	24		V
		$V_{CC} = 5\text{V}$ $R_L \geq 10\text{K}\Omega$		5	20		5	20		5	100	mV
Common-Mode Rejection Ratio	CMRR		70	85		65	80		50	80		dB
Power Supply Rejection Ratio	PSRR		65	100		65	100		50	100		dB
Channel Separation	CS	$f = 1\text{KHz}$ to 20KHz		120			120			120		dB
Short Circuit to GND	I_{SC}			40	60		40	60		40	60	mA
Output Current	I_{SOURCE}	$V_{I(+)} = 1\text{V}$, $V_{I(-)} = 0\text{V}$ $V_{CC} = 15\text{V}$, $V_{O(P)} = 2\text{V}$	10	30		10	30		10	30		mA
		$V_{I(+)} = 0\text{V}$, $V_{I(-)} = 1\text{V}$ $V_{CC} = 15\text{V}$, $V_{O(P)} = 2\text{V}$	10	15		10	15		10	15		mA
	I_{SINK}	$V_{I(+)} = 0\text{V}$, $V_{I(-)} = 1\text{V}$ $V_{CC} = 15\text{V}$, $V_{O(P)} = 200\text{mV}$	12	100		12	100					μA
Differential Input Voltage	$V_{I(DIFF)}$				V_{CC}			V_{CC}			V_{CC}	V

ELECTRICAL CHARACTERISTICS(V_{CC} = 5.0V, V_{EE} = GND, unless otherwise specified)The following specification apply over the range of $-25^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for the KA258; and the $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for the KA358; and the $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for the KA2904

Characteristic	Symbol	Test Conditions	KA258			KA358			KA2904			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V _{IO}	V _{CM} = 0V to V _{CC} - 1.5V V _{O(P)} = 1.4V, R _S = 0Ω			7.0			9.0			10.0	mV
Input Offset Voltage Drift	V _{IO}	R _S = 0Ω		7.0			7.0			7.0		μV/°C
Input Offset Current	I _{IO}				100			150		45	200	nA
Input Offset Current Drift	ΔI _{IO} /ΔT			10			10			10		pA/°C
Input Bias Current	I _{BIAS}			40	300		40	500		40	500	nA
Input Common-Mode Voltage Range	V _{I(R)}	V _{CC} = 30V (KA2904, V _{CC} 26V)	0		V _{CC} -2.0	0		V _{CC} -2.0	0		V _{CC} -2.0	V
Large Signal Voltage Gain	G _V	V _{CC} = 15V, R _L ≥ 2.0KΩ V _{O(P)} = 1V to 11V	25			15			15			V/mV
Output Voltage Swing	V _{O(H)}	V _{CC} = 30V V _{CC} = 26V for 2904	R _L = 2KΩ 26			26			26			V
			R _L = 10KΩ 27	28		27	28		27	28		V
	V _{O(L)}	V _{CC} = 5V, R _L ≥ 10KΩ		5	20		5	20		5	100	mV
Output Current	I _{SOURCE}	V _{I(+)} = 1V, V _{I(-)} = 0V V _{CC} = 15V, V _{O(P)} = 2V	10	30		10	30		10	30		mA
	I _{SINK}	V _{I(+)} = 0V, V _{I(-)} = 1V V _{CC} = 15V, V _{O(P)} = 2V	5	8		5	9		5	9		mA
Differential Input Voltage	V _{I(DIFF)}				V _{CC}			V _{CC}			V _{CC}	V

ELECTRICAL CHARACTERISTICS(V_{CC} = 5.0V, V_{EE} = GND, T_A = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	KA258A			KA358A			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V _{IO}	V _{CM} = 0V to V _{CC} - 1.5V V _{O(P)} = 1.4V, R _S = 0		1.0	3.0		2.0	3.0	mV
Input Offset Current	I _{IO}			2	15		5	30	nA
Input Bias Current	I _{BIAS}			40	80		45	100	nA
Input Common-Mode Voltage Range	V _{I(R)}	V _{CC} = 30V	0		V _{CC} - 1.5	0		V _{CC} - 1.5	V
Supply Current	I _{CC}	R _L = ∞, V _{CC} = 30V		0.8	2.0		0.8	2.0	mA
		R _L = ∞, over full temperature range		0.5	1.2		0.5	1.2	mA
Large Signal Voltage Gain	G _V	V _{CC} = 15V, R _L ≥ 2KΩ V _O = 1V to 11V	50	100		25	100		V/mV
Output Voltage Swing	V _{OH}	V _{CC} = 30V V _{CC} = 26V for 2904	26			26			V
		R _L = 2KΩ R _L = 10KΩ	27	28		27	28		V
	V _{OL}	V _{CC} = 5V, R _L ≥ 10KΩ		5	20		5	20	mV
Common-Mode Rejection Ratio	CMRR		70	85		65	85		dB
Power Supply Rejection Ratio	PSRR		65	100		65	100		dB
Channel Separation	CS	f = 1KHz to 20KHz		120			120		dB
Short Circuit to GND	I _{SC}			40	60		40	60	mA
Output Current	I _{SOURCE}	V _{I(+)} = 1V, V _{I(-)} = 0V V _{CC} = 15V, V _{O(P)} = 2	20	30		20	30		mA
	I _{SINK}	V _{I(+)} = 0V, V _{I(-)} = 1V V _{CC} = 15V, V _O = 2V	10	15		10	15		mA
		V _{I(+)} = 0V, V _{I(-)} = 1V V _{O(P)} = 200mV	12	100		12	100		μA
Differential Input Voltage	V _{I(DIFF)}				V _{CC}			V _{CC}	V

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0V$, $V_{EE} = GND$, unless otherwise specified)

The following specification apply over the range of $-25^{\circ}C \leq T_A \leq +85^{\circ}C$ for the KA258A; and the $0^{\circ}C \leq T_A \leq +70^{\circ}C$ for the KA358A

Characteristic	Symbol	Test Conditions	KA258A			KA358A			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	$V_{CM} = 0V$ to $V_{CC} - 1.5V$ $V_{O(P)} = 1.4V$, $R_S = 0\Omega$			4.0			5.0	mV
Input Offset Voltage Drift	$\Delta V_{IO} / \Delta T$			7.0	15		7.0	20	$\mu V / ^{\circ}C$
Input Offset Current	I_{IO}				30			75	nA
Input Offset Current Drift	$\Delta I_{IO} / \Delta T$			10	200		10	300	$pA / ^{\circ}C$
Input Bias Current	I_{BIAS}			40	100		40	200	nA
Input Common-Mode Voltage Range	$V_{I(R)}$	$V_{CC} = 30V$	0		$V_{CC} - 2.0$	0		$V_{CC} - 2.0$	V
Output Voltage Swing	$V_{O(H)}$	$V_{CC} = 30V$ $V_{CC} = 30V$	$R_L = 2K\Omega$ $R_L = 10K\Omega$	26 27		26 27			V V
	$V_{O(L)}$	$V_{CC} = 5V$, $R_L \geq 10K\Omega$		5	20		5	20	mV
Large Signal Voltage Gain	G_V	$V_{CC} = 15V$, $R_L \geq 2.0K\Omega$ $V_{O(P)} = 1V$ to $11V$	25			15			V/mV
Output Current	I_{SOURCE}	$V_{I(+)} = 1V$, $V_{I(-)} = 0V$ $V_{CC} = 15V$, $V_{O(P)} = 2V$	10	30		10	30		mA
	I_{SINK}	$V_{I(+)} = 0V$, $V_{I(-)} = 1V$ $V_{CC} = 15V$, $V_{O(P)} = 2V$	5	9		5	9		mA
Differential Input Voltage	$V_{I(DIFF)}$				V_{CC}			V_{CC}	V

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1 SUPPLY CURRENT

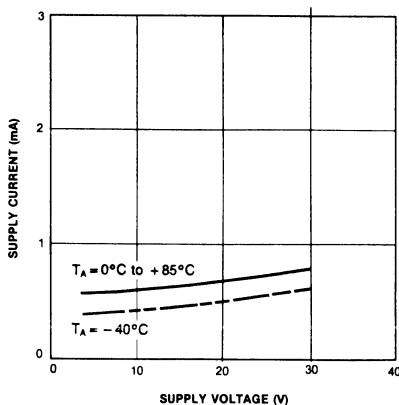


Fig. 2 VOLTAGE GAIN

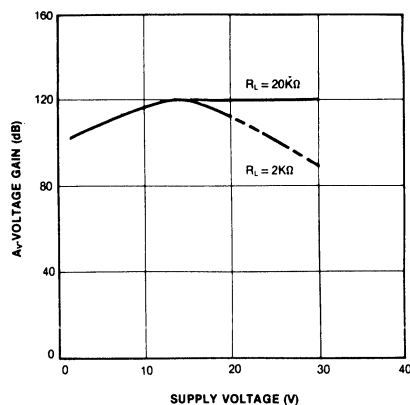


Fig. 3 OPEN LOOP FREQUENCY RESPONSE

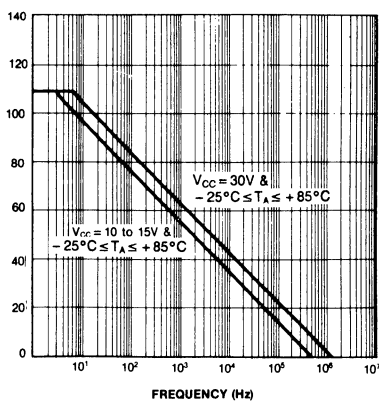


Fig. 4 LARGE SIGNAL FREQUENCY

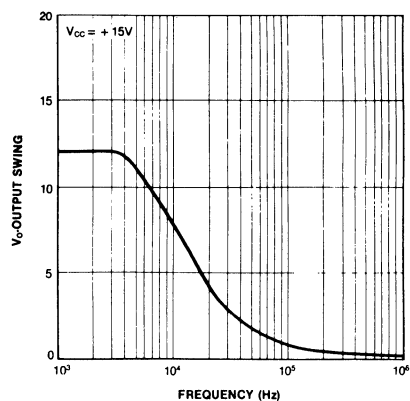
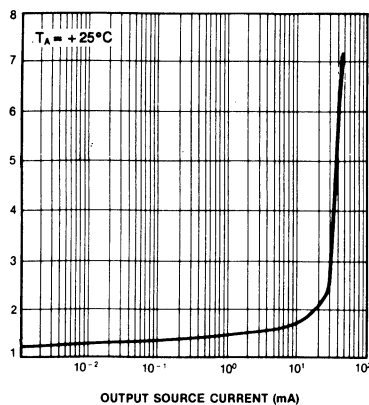
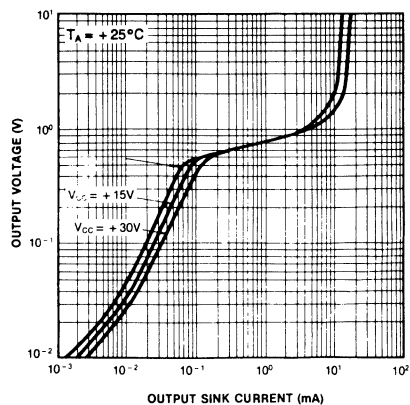
Fig. 5 OUTPUT CHARACTERISTICS
CURRENT SOURCINGFig. 6 OUTPUT CHARACTERISTICS
CURRENT SINKING

Fig. 7 INPUT VOLTAGE RANGE

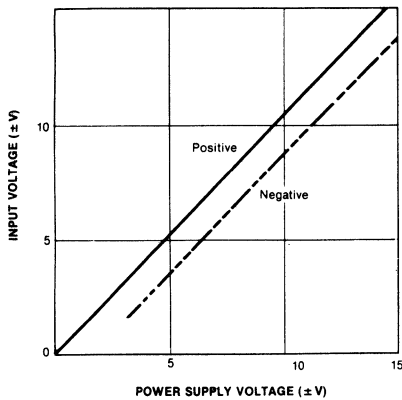


Fig. 9 CURRENT LIMITING

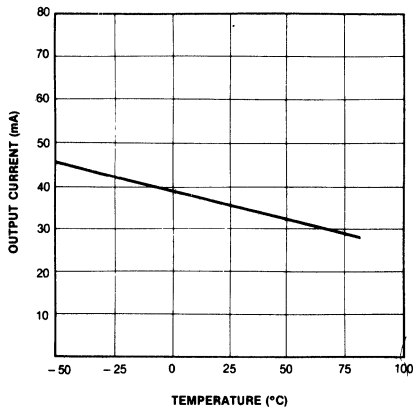


Fig. 11 VOLTAGE FOLLOWER PULSE RESPONSE

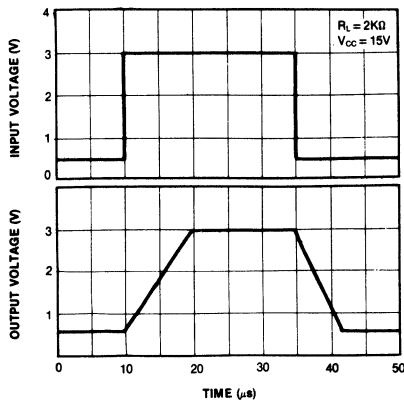


Fig. 8 COMMON-MODE REJECTION RATIO

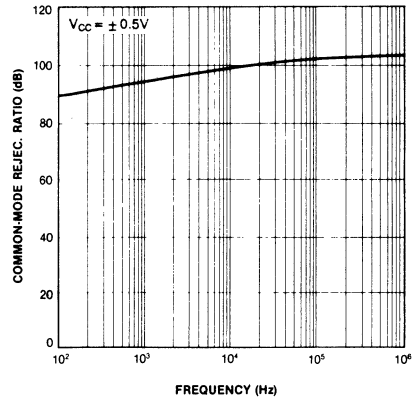


Fig. 10 INPUT CURRENT

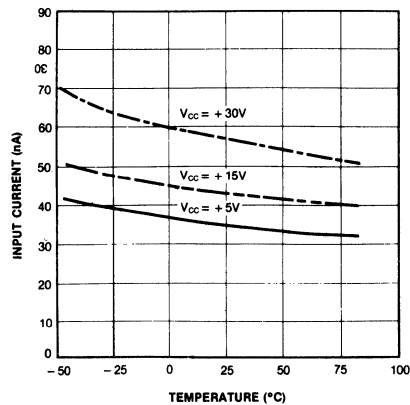
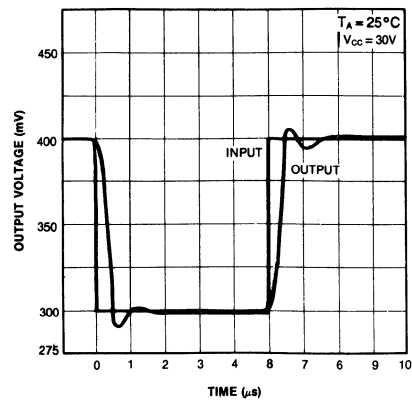


Fig. 12 VOLTAGE FOLLOWER PULSE RESPONSE (SMALL SIGNAL)



CURRENT-MODE PWM CONTROLLERS

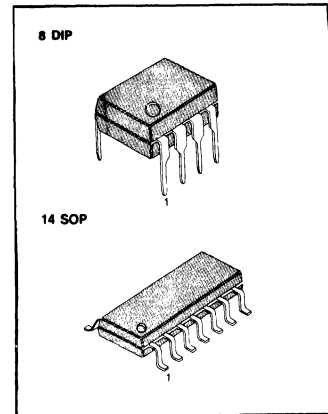
The KA3842B/3B/4B/5B are fixed frequency current-mode PWM controllers. They are specially designed for Off-Line and DC-to-DC converter applications with minimal external components. These integrated circuits feature a trimmed oscillator for precise duty cycle control, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totempole output ideally suited for driving a power MOSFET.

Protection circuitry includes built-in under-voltage lockout and current limiting.

The KA3842B and KA3844B have UVLO thresholds of 16V (on) and 10V (off). The KA3843B and KA3845B are 8.5V (on) and 7.9V (off). The KA3842B and KA3843B can operate within 100% duty cycle. The KA3844B and KA3845B can operate within 50% duty cycle.

FEATURES

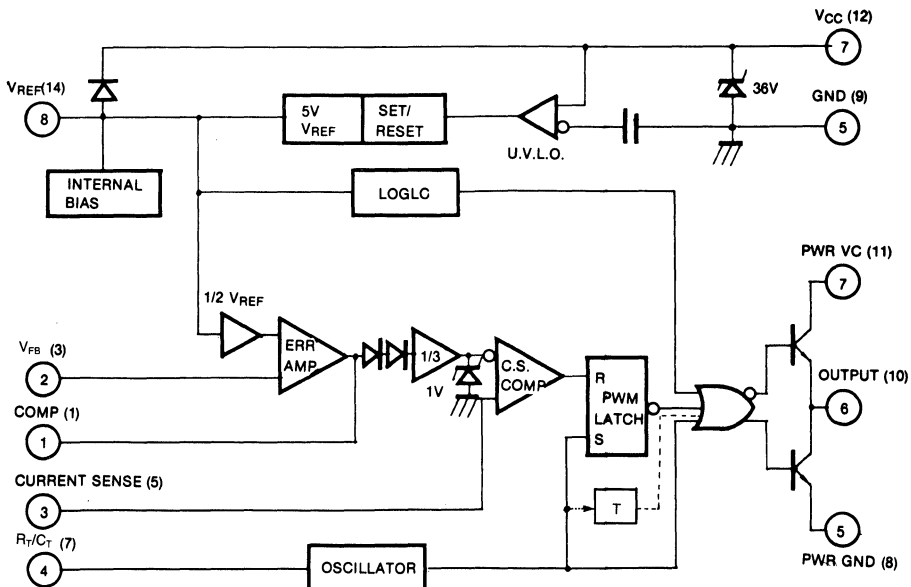
- Low Start Up Current
- Maximum Duty Clamp
- U/V Lockout With Hysteresis
- Operating Frequency Up To 500 KHz



ORDERING INFORMATION

Device	Package	Operating Temperature
KA384XB	8 DIP	0 ~ +70°C
KA384XBD	14 SOP	0 ~ +70°C

BLOCK DIAGRAM



* () IS 14SOIC PIN NO

* TOGGLE FLIP FLOP USED ONLY IN KA3844B, KA3845B

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	30	V
Output Current	I_O	± 1	A
Analog Inputs	$V_{(ANA)}$	-0.3 to V_{CC}	V
Error Amp Output Sink Current	$I_{SINK(EA)}$	10	mA
Power Dissipation ($T_A = 25^\circ\text{C}$)	P_D	1	W

ELECTRICAL CHARACTERISTICS

(* $V_{CC} = 15\text{V}$, $R_T = 10\text{K}\Omega$, $C_T = 3.3\text{nF}$, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
REFERENCE SECTION						
Reference Output Voltage	V_{REF}	$T_J = 25^\circ\text{C}$, $I_{REF} = 1\text{mA}$	4.90	5.00	5.10	V
Line Regulation	ΔV_{REF}	$12\text{V} \leq V_{CC} \leq 25\text{V}$		6	20	mV
Load Regulation	ΔV_{REF}	$1\text{mA} \leq I_{REF} \leq 20\text{mA}$		6	25	mV
Short Circuit Output Current	I_{SC}	$T_A = 25^\circ\text{C}$		-100	-180	mA
OSCILLATOR SECTION						
Oscillation Frequency	f	$T_J = 25^\circ\text{C}$	47	52	57	KHz
Frequency Change with Voltage	$\Delta f / \Delta V_{CC}$	$12\text{V} \leq V_{CC} \leq 25\text{V}$		0.05	1	%
Oscillator Amplitude	$V_{(OSC)}$			1.6		V_{pp}
ERROR AMPLIFIER SECTION						
Input Bias Current	I_{BIAS}			-0.1	-2	μA
Input Voltage	$V_{(EA)}$	$V_1 = 2.5\text{V}$	2.42	2.50	2.58	V
Open Loop Voltage Gain	G_{VO}	$2\text{V} \leq V_O \leq 4\text{V}$	65	90		dB
Power Supply Rejection Ratio	PSRR	$12\text{V} \leq V_{CC} \leq 25\text{V}$	60	70		dB
Output Sink Current	I_{SINK}	$V_2 = 2.7\text{V}$, $V_1 = 1.1\text{V}$	2	7		mA
Output Source Current	I_{SOURCE}	$V_2 = 2.3\text{V}$, $V_1 = 5\text{V}$	-0.5	-1.0		mA
High Output Voltage	V_{OH}	$V_2 = 2.3\text{V}$, $R_L = 15\text{K}\Omega$ to GND	5	6		V
Low Output Voltage	V_{OL}	$V_2 = 2.7\text{V}$, $R_L = 15\text{K}\Omega$ to Pin 8		0.8	1.1	V
CURRENT SENSE SECTION						
Gain	G_V	(Note 1 & 2)	2.85	3	3.15	V/V
Maximum Input Signal	$V_{(MAX)}$	$V_1 = 5\text{V}$ (Note 1)	0.9	1	1.1	V
Power Supply Rejection Ratio	PSRR	$12\text{V} \leq V_{CC} \leq 25\text{V}$ (Note 1)		70		dB
Input Bias Current	I_{BIAS}			-3	-10	μA

ELECTRICAL CHARACTERISTICS (Continued)(* $V_{CC} = 15V$, $R_T = 10K\Omega$, $C_T = 3.3nF$, $T_A = 0^\circ C$ to $+70^\circ C$ unless otherwise specified)

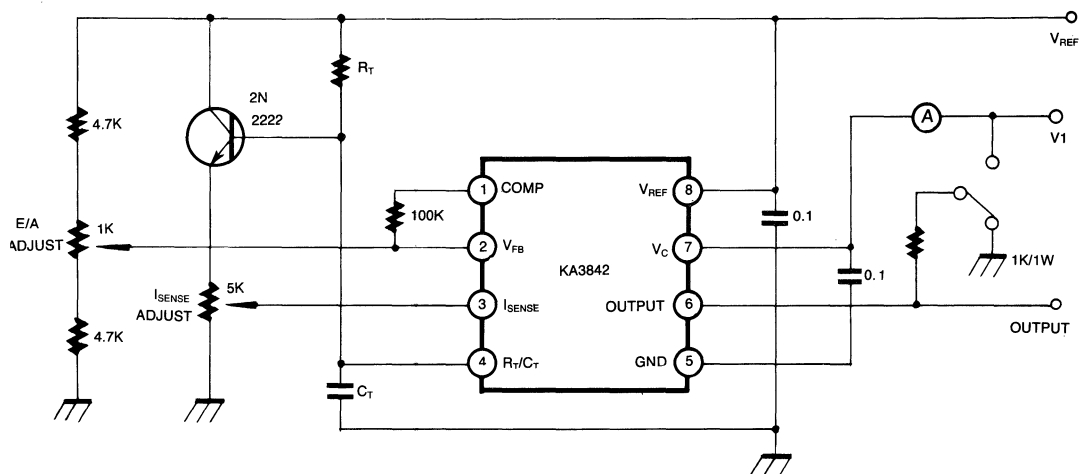
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
OUTPUT SECTION						
Low Output Voltage	V _{OL}	I _{SINK} = 20mA		0.08	0.4	V
		I _{SINK} = 200mA		1.4	2.2	V
High Output Voltage	V _{OH}	I _{SOURCE} = 20mA	13	13.5		V
		I _{SOURCE} = 200mA	12	13.0		V
Rise Time	t _R	T _J = 25°C, C _L = 1nF (Note 3)		45	150	nS
Fall Time	t _F	T _J = 25°C, C _L = 1nF (Note 3)		35	150	nS
UNDER-VOLTAGE LOCKOUT SECTION						
Start Threshold	V _{TH(ST)}	KA3842B/44B	14.5	16.0	17.5	V
		KA3843B/45B	7.8	8.4	9.0	V
Min. Operating Voltage (After Turn On)	V _{OPR(MIN)}	KA3842B/44B	8.5	10.0	11.5	V
		KA3843B/45B	7.0	7.6	8.2	V
PWM SECTION						
Max. Duty Cycle	D _(MAX)	KA3842B/43B	95	97	100	%
		KA3844B/45B	47	48	50	%
Min. Duty Cycle	D _(MIN)				0	%
TOTAL STANDBY CURRENT						
Start-Up Current	I _{ST}			0.45	1	mA
Operating Supply Current	I _{CC(OPR)}	V ₃ = V ₂ = OV		14	17	mA
Zener Voltage	V _Z	I _{CC} = 25mA	30	38		V

*Adjust V_{CC} above the start threshold before setting at 15VNote 1. Parameter measured at trip point of lath with $V_2 = 0$

2. Gain defined as: $A = \frac{\Delta V_1}{\Delta V_3}$; $0 \leq V_3 \leq 0.8V$

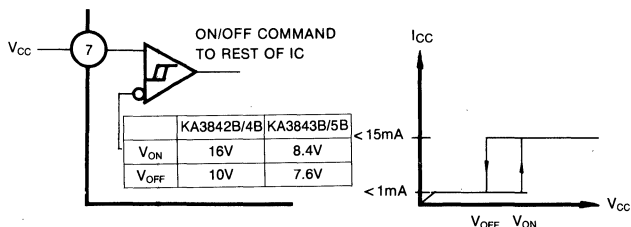
3. These parameters, although guaranteed, are not 100% tested in production.

Fig. 1 Open Loop Test Circuit



High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5K Ω potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

Fig. 2 Under Voltage Lockout



During Under-Voltage Lock-Out, the output driver is biased to a high impedance state. Pin 6 should be shunted to ground with a bleeder resistor to prevent activating the power switch with output leakage current.

Fig. 3 Error Amp Configuration

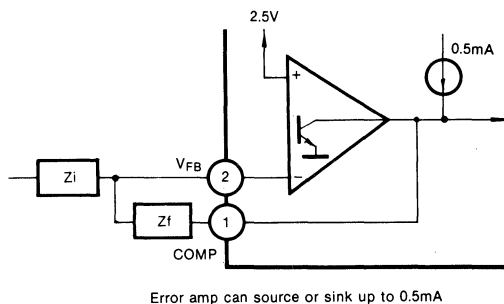
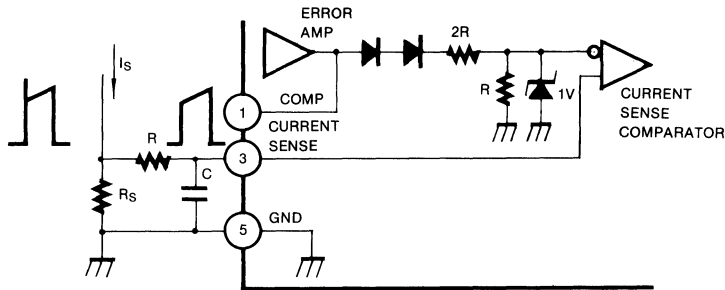


Fig. 4 Current Sense Circuit

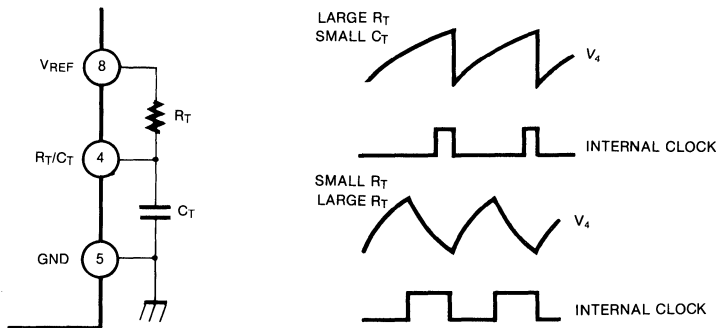


Peak current (I_S) is determined by the formula:

$$I_{S(MAX)} \approx \frac{1.0V}{R_S}$$

A small RC filter may be required to suppress switch transients.

Fig. 5 Oscillator Waveforms and Maximum Duty Cycle



Oscillator timing capacitor, C_T , is charged by V_{REF} through R_T , and discharged by an internal current source. During the discharge time, the internal clock signal blanks the output to the low state. Selection of R_T and C_T therefore determines both oscillator frequency and maximum duty cycle. Charge and discharge times are determined by the formulas:

$$t_c \approx 0.55 R_T C_T$$

$$t_d \approx R_T C_T \ln \left(\frac{0.0063 R_T - 2.7}{0.0063 R_T - 4} \right)$$

Frequency, then, is: $f = (t_c + t_d)^{-1}$

$$\text{For } R_T > 5K\Omega, f \approx \frac{1.8}{R_T C_T}$$

Fig. 6 Oscillator Dead Time & Frequency
DEADTIME vs C_T ($R_T > 5K$)

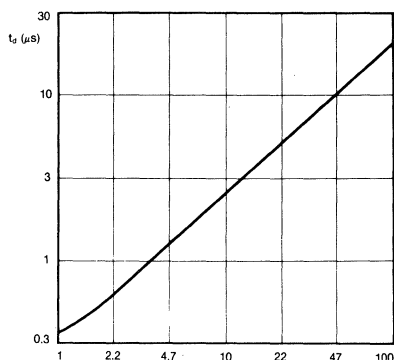


Fig. 7 Timing Resistance vs Frequency

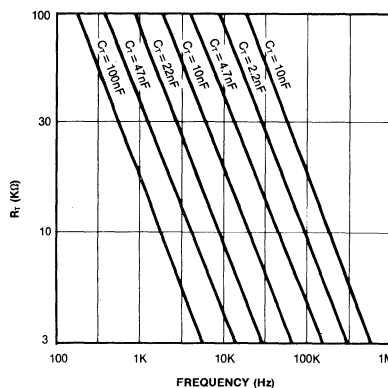
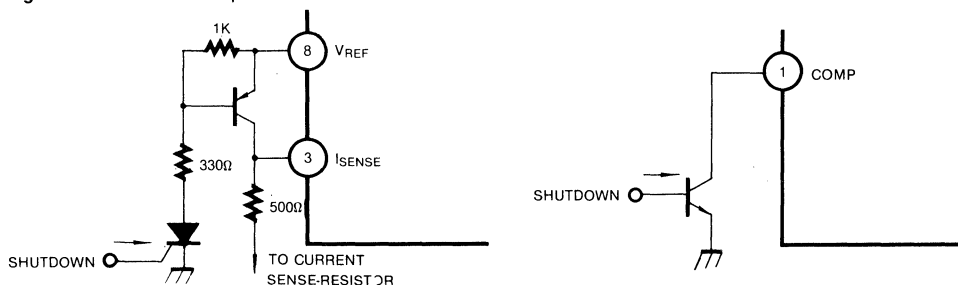
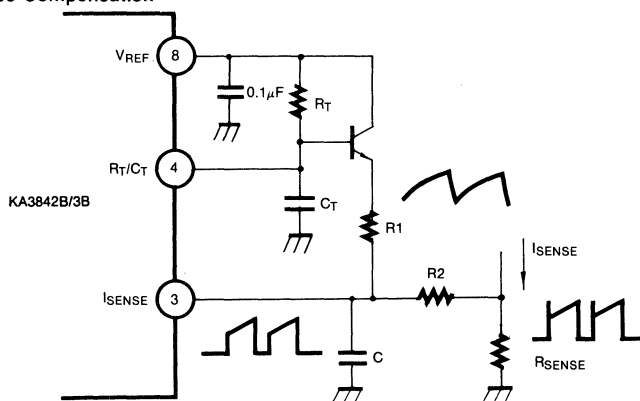


Fig. 8 Shutdown Techniques



Shutdown of the KA3842B can be accomplished by two methods; either raise pin 3 above 1V or pull pin 1 below a voltage two diode drops above ground. Either method causes the output of the PWM comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at pins 1 and/or 3 is removed. In one example, an externally latched shutdown may be accomplished by adding an SCR which will be reset by cycling V_{CC} below the lower UVLO threshold. At this point the reference turns off, allowing the SCR to reset.

Fig. 9 Slope Compensation



A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50%.

Note that capacitor, C , forms a filter with R_2 to suppress the leading edge switch spikes.

Fig. 10 TEMPERATURE DRIFT (V_{ref})
KA3842B

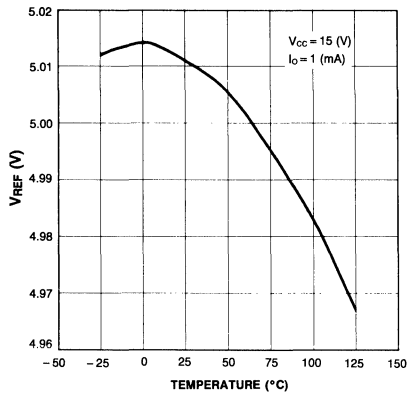


Fig. 11 TEMPERATURE DRIFT (1st)
KA3842B

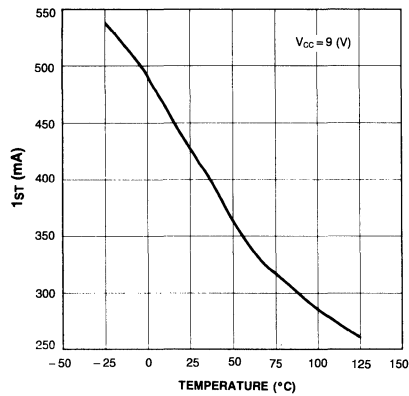
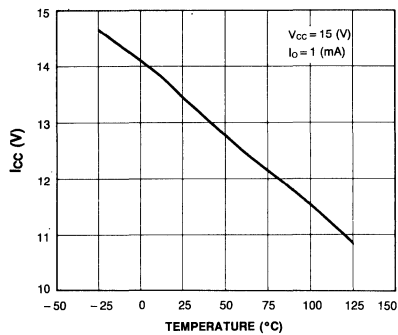


Fig. 12 TEMPERATURE DRIFT (I_{cc})
KA3842B



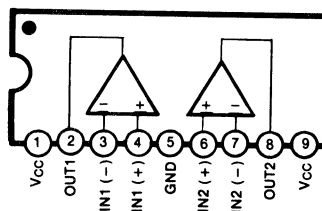
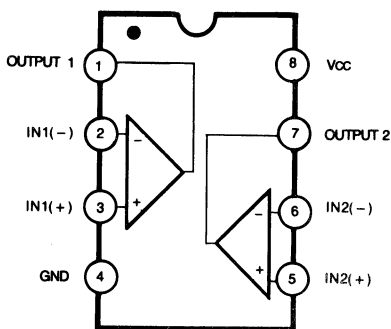
DUAL DIFFERENTIAL COMPARATOR

The KA293 series consists of two independent voltage comparators designed to operate from a single power supply over a wide voltage range.

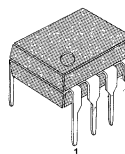
FEATURES

- Single Supply Operation: 2V to 36V
- Dual Supply Operation: $\pm 1\text{V}$ to $\pm 18\text{V}$
- Allow Comparison of Voltages Near Ground Potential
- Low Current Drain 800 μA Typ
- Compatible with all Forms of Logic
- Low Input Bias Current 25nA Typ
- Low Input Offset Current $\pm 5\text{nA}$ Typ
- Low Offset Voltage $\pm 1\text{mV}$ Typ

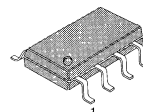
BLOCK DIAGRAM



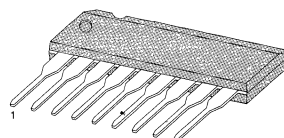
8 DIP



8 SOP



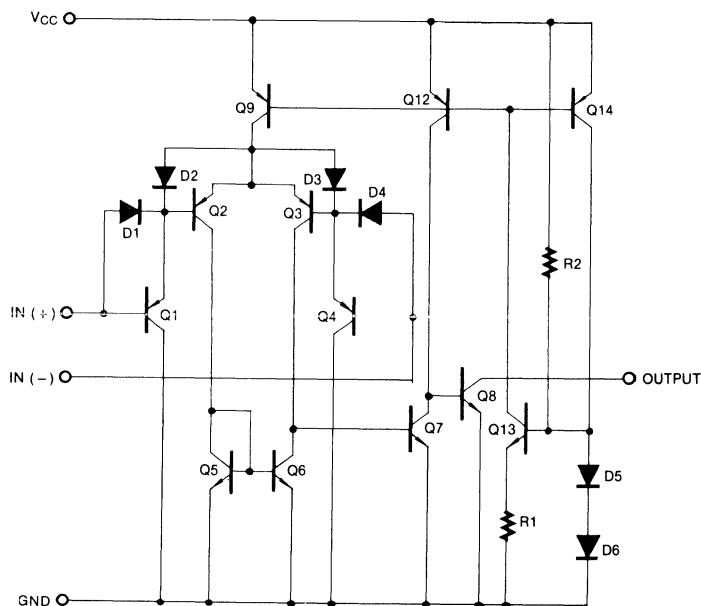
9 SIP



ORDERING INFORMATION

Device	Package	Operating Temperature
KA393 KA393A	8 DIP	0 ~ +75°C
KA393S KA393AS	9 SIP	
KA393D KA393AD	8 SOP	
KA293 KA293A	8 DIP	-25 ~ +85°C
KA293S KA293AS	9 DIP	
KA293D KA293AD	8 SOP	
KA2903	8 DIP	-40 ~ +85°C
KA2903D	8 SOP	
KA2903S	9 SIP	

SCHEMATIC DIAGRAM



2

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	± 18 or 36	V
Differential Input Voltage	$V_{I(DIFF)}$	36	V
Input Voltage	V_I	-0.3 to $+36$	V
Output Short Circuit to GND		Continuous	
Power Dissipation	P_D	570	mW
Operating Temperature KA393/KA393A KA293/KA293A KA2903	T_{OPR}	$0 \sim +70$ $-25 \sim +85$ $-40 \sim +85$	$^{\circ}\text{C}$
Storage Temperature	T_{STG}	$-65 \sim +150$	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25^\circ C$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	KA293A/KA393A			KA293/KA393			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	$V_{CM} = 0V$ to $V_{CC} - 1.5V$ $V_{O(P)} = 1.4V$, $R_S = 0$ NOTE 1		± 1	± 2		± 1	± 5	mV
Input Offset Current	I_{IO}	NOTE 1		± 5	± 50		± 5	± 50	nA
Input Bias Current	I_{BIAS}	NOTE 1		65	250		65	250	nA
Input Common Mode Voltage Range	$V_{I(R)}$	NOTE 1	0		$V_{CC} - 1.5$	0		$V_{CC} - 1.5$	V
Supply Current	I_{CC}	$R_L = \infty$ $R_L = \infty$ $V_{CC} = 30V$		0.6	1		0.6	1	mA
Voltage Gain	G_V	$V_{CC} = 15V$, $R_L \geq 15K\Omega$ (for large $V_{O(P-P)}$ swing)	50	200		50	200		V/mV
Large Signal Response Time	t_{RES}	$V_I = \text{TTL Logic Swing}$ $V_{REF} = 1.4V$, $V_{RL} = 5V$, $R_L = 5.1K\Omega$		350			350		nS
Response Time	t_{RES}	$V_{RL} = 5V$, $R_L = 5.1K\Omega$		1.4			1.4		μS
Output Sink Current	I_{SINK}	$V_{I(-)} \geq 1V$, $V_{I(+)} = 0V$, $V_{O(P)} \leq 1.5V$	6	18		6	18		mA
Output Saturation Voltage	V_{SAT}	$V_{I(-)} \geq 1V$, $V_{I(+)} = 0V$ $I_{SINK} = 4mA$ NOTE 1		160	400		160	400	mV
Output Leakage Current	$I_{O(LKG)}$	$V_{I(-)} = 0$, $V_{O(P)} = 5V$ $V_{I(+)} = 1V$, $V_{O(P)} = 30V$		0.1			0.1		nA
					1.0			1.0	μA

NOTE 1

KA393/A: $0 \leq T_A \leq +70^\circ C$ KA293/A: $-25 \leq T_A \leq +85^\circ C$ KA2903: $-40 \leq T_A \leq +85^\circ C$

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25^\circ C$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	KA2903			Unit
			Min	Typ	Max	
Input Offset Voltage	V_{IO}	$V_{CM} = 0V$ to $V_{CC} - 1.5V$ $V_{O(P)} = 1.4V$, $R_S = 0$ NOTE 1		± 1 ± 9	± 7 ± 15	mV
Input Offset Current	I_{IO}	NOTE 1		± 5 ± 50	± 50 ± 200	nA
Input Bias Current	I_{BIAS}	NOTE 1		65	250 500	nA
Input Common Mode Voltage Range	$V_{I(R)}$	NOTE 1	0 0		$V_{CC}-1.5$ $V_{CC}-2$	V
Supply Current	I_{CC}	$R_L = \infty$		0.6	1	mA
		$R_L = \infty$ $V_{CC} = 30V$		1	2.5	
Voltage Gain	G_V	$V_{CC} = 15V$, $R_L \geq 15K\Omega$ (for large $V_{O(P-P)}$ swing)	25	100		V/mV
Large Signal Response Time	t_{RES}	$V_I = \text{TTL Logic Swing}$ $V_{REF} = 1.4V$, $V_{RL} = 5V$, $R_L = 5.1K\Omega$		350		nS
Response Time	t_{RES}	$V_{RL} = 5V$, $R_L = 5.1K\Omega$		1.5		μS
Output Sink Current	I_{SINK}	$V_{I(-)} \geq 1V$, $V_{I(+)} = 0V$, $V_{O(P)} \leq 1.5V$	6	16		mA
Output Saturation Voltage	V_{SAT}	$V_{I(-)} \geq 1V$, $V_{I(+)} = 0V$ $I_{SINK} = 4mA$ NOTE 1		160	400 700	mV
Output Leakage Current	$I_{O(LKG)}$	$V_{I(-)} = 0$, $V_{O(P)} = 5V$		0.1		nA
		$V_{I(+)} = 1V$, $V_{O(P)} = 30V$			1.0	μA

NOTE 1

KA393/A: $0 \leq T_A \leq +70^\circ C$ KA293/A: $-25 \leq T_A \leq +85^\circ C$ KA2903: $-40 \leq T_A \leq +85^\circ C$

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1 SUPPLY CURRENT

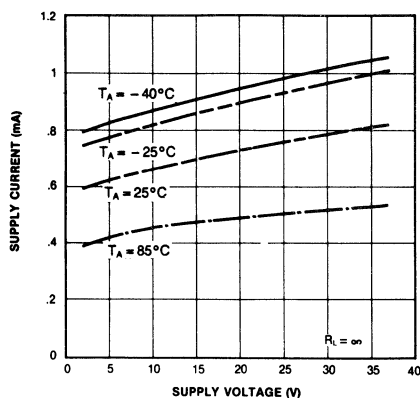


Fig. 2 INPUT CURRENT

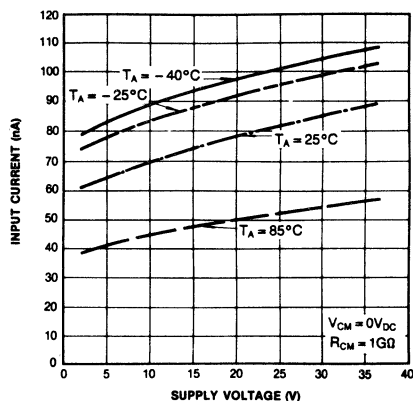


Fig. 3 OUTPUT SATURATION VOLTAGE

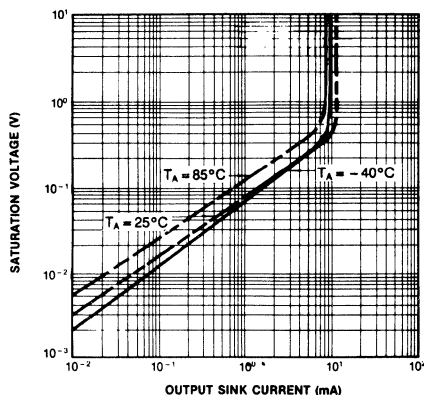


Fig. 4 RESPONSE TIME FOR VARIOUS INPUT OVERDRIVE-NEGATIVE TRANSITION

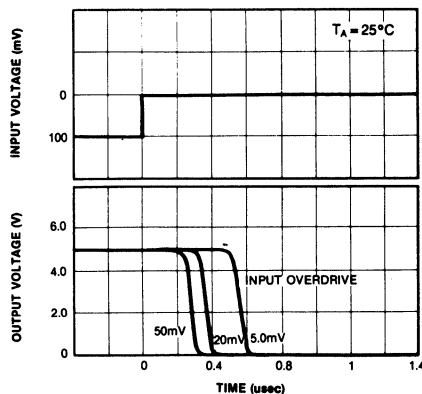
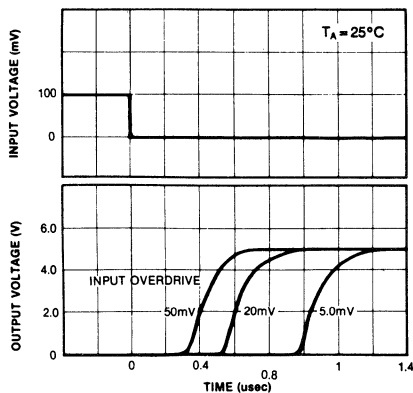


Fig. 5 RESPONSE TIME FOR VARIOUS INPUT OVERDRIVE-POSITIVE TRANSITION



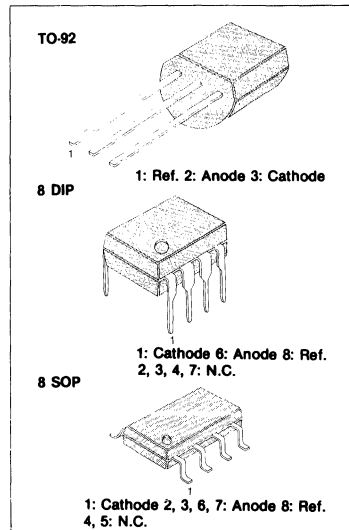
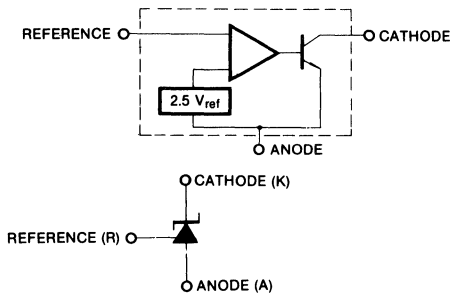
PROGRAMMABLE PRECISION REFERENCES

The KA431/A are three-terminal adjustable regulator series with a guaranteed thermal stability over applicable temperature ranges. The output voltage may be set to any value between V_{ref} (approximately 2.5 volts) and 36 volts with two external resistors. These devices have a typical dynamic output impedance of 0.2Ω . Active output circuitry provides a very sharp turn-on characteristic, making these devices excellent replacement for zener diodes in many applications.

FEATURES

- Programmable output voltage to 36 volts
- Low dynamic output impedance 0.2Ω typical
- Sink current capability of 1.0 to 100mA
- Equivalent full-range temperature coefficient of $50\text{ppm}/^\circ\text{C}$ typical
- Temperature compensated for operation over full rated operating temperature range
- Low output noise voltage
- Fast turn on response

BLOCK DIAGRAM



ORDERING INFORMATION

Device	Operating Temperature	Package
KA431Z	$0 \sim +70^\circ\text{C}$	TO-92
KA431	$0 \sim +70^\circ\text{C}$	8 DIP
KA431D	$0 \sim +70^\circ\text{C}$	8 SOP
KA431AZ	$0 \sim +70^\circ\text{C}$	TO-92

ABSOLUTE MAXIMUM RATINGS

(Operating temperature range applies unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Cathode Voltage	V_{KA}	37	V
Cathode Current Range (Continuous)	I_{KA}	- 100 ~ + 150	mA
Reference Input Current Range	I_{REF}	0.05 ~ + 10	mA
Power Dissipation D, Z Suffix Package N Suffix Package	P_D	770 1000	mW mW
Operating Temperature Range	T_{OPR}	0 ~ + 70	
Storage Temperature Range	T_{STG}	- 65 ~ + 150	°C

RECOMMENDED OPERATING CONDITIONS

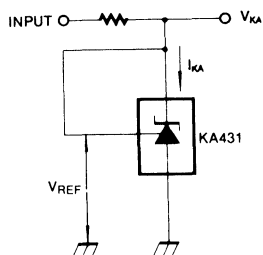
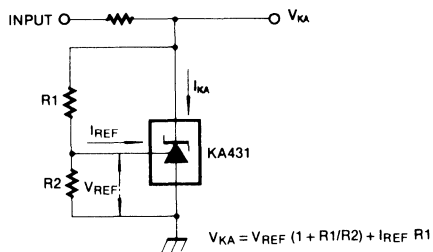
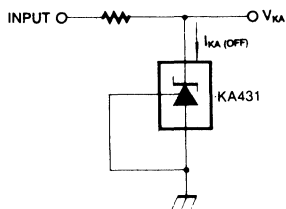
Characteristic	Symbol	Min	Typ	Max	Unit
Cathode Voltage	V_{KA}	V_{REF}		36	V
Cathode Current	I_{KA}	1.0		100	mA

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	KA431			KA431A			Unit
			Min	Typ	Max	Min	Typ	Max	
Reference Input Voltage	V_{REF}	$V_{KA} = V_{REF}$, $I_{KA} = 10\text{mA}$	2.440	2.495	2.550	2.470	2.495	2.520	V
Deviation of Reference Input Voltage Over-Temperature (Note 1)	$\Delta V_{REF}/\Delta T$	$V_{KA} = V_{REF}$, $I_{KA} = 10\text{mA}$ $T_{MIN} \leq T_A \leq T_{MAX}$		4.5	17		4.5	17	mV
Ratio of Change in Reference Input Voltage to the Change in Cathode Voltage	$\Delta V_{REF}/\Delta V_{KA}$	$I_{KA} = 10\text{mA}$ $\Delta V_{KA} = 10\text{V} - V_{REF}$		- 1.0	- 2.7		- 1.0	- 2.7	mV/V
		$\Delta V_{KA} = 36\text{V} - 10\text{V}$		- 0.5	- 2.0		- 0.5	- 2.0	
Reference Input Current	I_{REF}	$I_{KA} = 10\text{mA}$, $R_1 = 10\text{K}\Omega$, $R_2 = \infty$		1.5	4		1.5	4	μA
Deviation of Reference Input Current Over Full Temperature Range	$\Delta I_{REF}/\Delta T$	$I_{KA} = 10\text{mA}$, $R_1 = 10\text{K}\Omega$, $R_2 = \infty$ $T_A = \text{Full Range}$		0.4	1.2		0.4	1.2	μA
Minimum Cathode Current for Regulation	$I_{KA(MIN)}$	$V_{KA} = V_{REF}$		0.45	1.0		0.45	1.0	mA
Off-State Cathode Current	$I_{KA(OFF)}$	$V_{KA} = 36\text{V}$, $V_{REF} = 0$		0.05	1.0		0.05	1.0	μA
Dynamic Impedance (Note 2)	Z_{KA}	$V_{KA} = V_{REF}$, $I_{KA} = 1$ to 100mA $f \leq 1.0\text{KHz}$		0.15	0.5		0.15	0.5	Ω

 $T_{MIN} = 0^\circ\text{C}$, $T_{MAX} = +70^\circ\text{C}$

TEST CIRCUITS

Fig. 1 Test Circuit for $V_{KA} = V_{REF}$ Fig. 2 Test Circuit for $V_{KA} \geq V_{REF}$ Fig. 3 Test Circuit for $I_{KA} \text{ (OFF)}$ 

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 4 CATHODE CURRENT VS CATHODE VOLTAGE

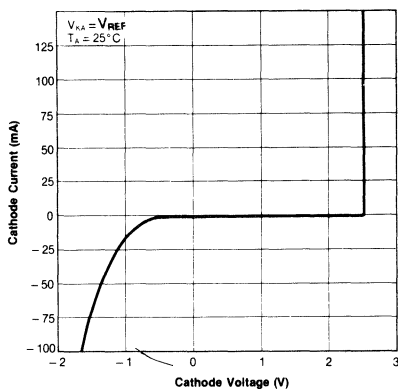


Fig. 5 CATHODE CURRENT VS CATHODE VOLTAGE

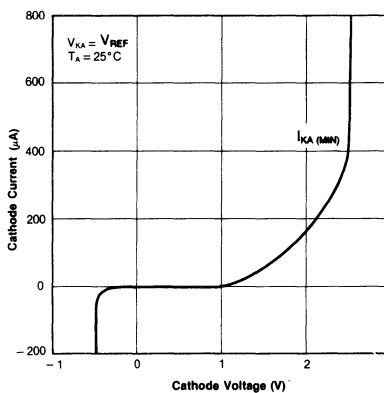


Fig. 6 CHANGE IN REFERENCE VOLTAGE VS CATHODE VOLTAGE

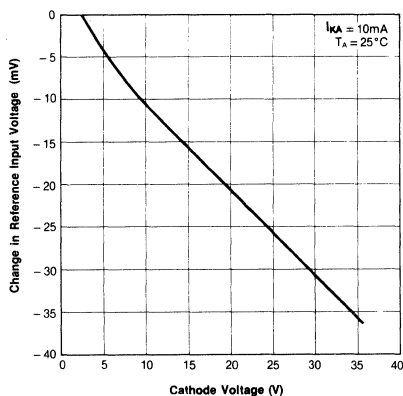


Fig. 7 DYNAMIC IMPEDANCE VS FREQUENCY

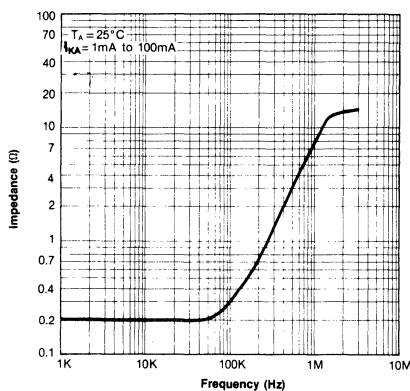
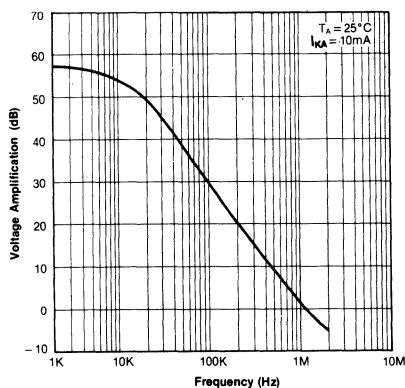
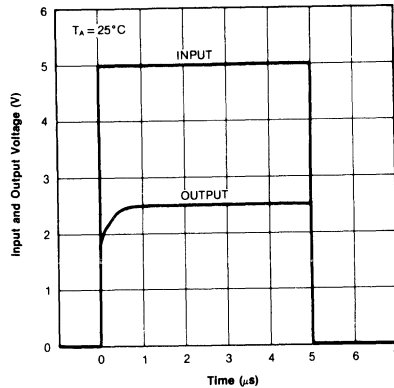


Fig. 8 SMALL SIGNAL VOLTAGE AMPLIFICATION VS FREQUENCY



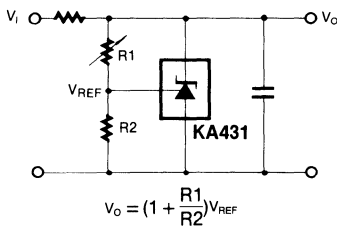
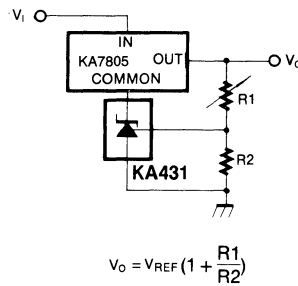
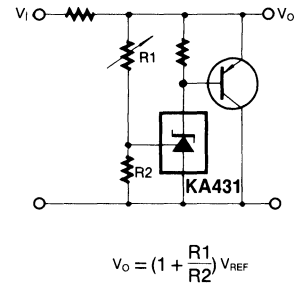
TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 9 PULSE RESPONSE



TYPICAL APPLICATIONS

Fig. 10 —SHUNT REGULATOR

Fig. 11—OUTPUT CONTROL
OF A THREE-TERMINAL
FIXED REGULATORFig. 12—HIGHER-CURRENT
SHUNT REGULATOR

TYPICAL APPLICATIONS

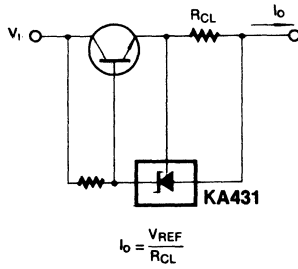
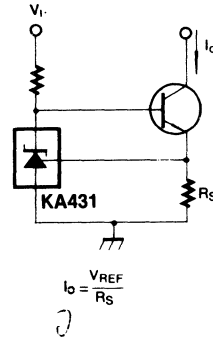
Fig. 13—CURRENT LIMITER OR
CURRENT SOURCE

Fig. 14—CONSTANT-CURRENT SINK



SINGLE TIMERS

The KA555/I is a highly stable controller capable of producing accurate timing pulses. With monostable operation, the time delay is controlled by one external and one capacitor. With astable operation, the frequency and duty cycle are accurately controlled with two external resistors and one capacitor.

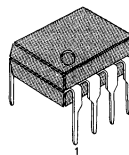
FEATURES

- High Current Drive Capability (= 200mA)
- Adjustable Duty Cycle
- Temperature Stability Of 0.005%/°C
- Timing From μ Sec To Hours
- Turn Off Time Less Than 2 μ Sec

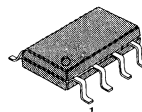
APPLICATIONS

- Precision Timing
- Pulse Generation
- Time Delay Generation
- Sequential Timing

8 DIP



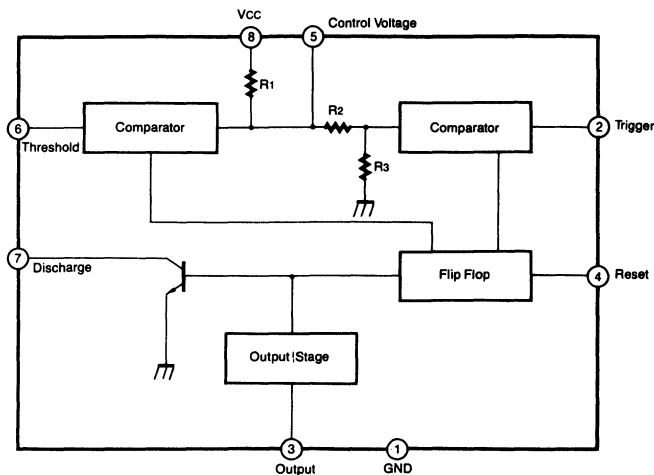
8 SOP



ORDERING INFORMATION

Device	Package	Operating Temperature
KA555D	8 DIP	0 ~ +70°C
KA555 I	8 SOP	
KA555 ID	8 DIP	-40 ~ +85°C
KA555 ID	8 SOP	

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Lead Temperature (soldering 10 sec)	T_{LEAD}	300	$^\circ\text{C}$
Power Dissipation	P_D	600	mW
Operating Temperature Range KA555	T_{OPR}	$0 \sim +70$	$^\circ\text{C}$
KA555I		$-40 \sim +85$	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	$-65 \sim +150$	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$, $V_{CC} = 5 \sim 15\text{V}$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		4.5		16	V
Supply Current * I_{CC} (low stable)	I_{CC}	$V_{CC} = 5\text{V}$, $R_L = \infty$		3	6	mA
		$V_{CC} = 15\text{V}$, $R_L = \infty$		7.5	15	mA
*Timing Error (Monostable) ²Initial Accuracy Drift with Temperature Drift with Supply Voltage	ACCUR $\Delta t/\Delta T$ $\Delta t/\Delta V_{CC}$	$R_A = 1\text{K}\Omega$ to 100K Ω $C = 0.1\mu\text{F}$		1.0 50 0.1	3.0 0.5	% ppm/ $^\circ\text{C}$ %/V
*Timing Error (astable) ²Initial Accuracy Drift with Temperature Drift with Supply Voltage	ACCUR $\Delta t/\Delta T$ $\Delta t/\Delta V_{CC}$	$R_A = 1\text{K}$ to 100K Ω $C = 0.1\mu\text{F}$		2.25 150 0.3		% ppm/ $^\circ\text{C}$ %/V
Control Voltage	V_C	$V_{CC} = 15\text{V}$	9.0	10.0	11.0	V
		$V_{CC} = 5\text{V}$	2.6	3.33	4.0	V
Threshold Voltage	V_{TH}	$V_{CC} = 15\text{V}$		10.0		V
		$V_{CC} = 5\text{V}$		3.33		V
*³Threshold Current	I_{TH}			0.1	0.25	μA
Trigger Voltage	V_{TR}	$V_{CC} = 5$	1.1	1.67	2.2	V
Trigger Voltage	V_{TR}	$V_{CC} = 15\text{V}$	4.5	5	5.6	V
Trigger Current	I_{TR}	$V_{TR} = 0\text{V}$		0.01	2.0	μA
Reset Voltage	V_{RST}		0.4	0.7	1.0	V
Reset Current	I_{RST}			0.1	0.4	mA

APPLICATION NOTE

The application circuit shows astable mode.

Pin 6 (threshold) is tied to Pin 2 (trigger) and Pin 4 (reset) is tied to V_{CC} (Pin 8).

The external capacitor C_1 of Pin 6 and Pin 2 charges through R_A , R_B and discharges through R_B only.

In the internal circuit of the KA555 one input of the upper comparator is the $2/3 V_{CC}$ (* $R_1 = R_2 = R_3$), another input if it is connected Pin 6.

As soon as charging C_1 is higher than $2/3 V_{CC}$, discharge transistor Q_1 turns on and C_1 discharges to collector of transistor Q_1 .

Therefore, the flip-flop circuit is reset and output is low.

One input of lower comparator is the $1/3 V_{CC}$, discharge transistor Q_1 turn off and C_1 charges through R_A and R_B .

Therefore, the flip-flop circuit is set and output is high.

So to say, when C_1 charges through R_A and R_B output is high and when C_1 discharges through R_B output is low.

The charge time (output is high) T_1 is $0.693 (R_A + R_B) C_1$ and the discharge time (output is low) T_2 is $0.693 (R_B C_1)$.

$$\left(\ln \frac{V_{CC} - 1/3 V_{CC}}{V_{CC} - 2/3 V_{CC}} = 0.693 \right)$$

Thus the total period time T is given by

$$T = T_1 + T_2 = 0.693 (R_A + 2R_B) C_1$$

Then the frequency of astable mode is given by

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B) C_1}$$

The duty cycle is given by

$$D.C = \frac{T_2}{T} = \frac{R_B}{R_A + 2R_B}$$

If you make use of the KA556 you can make two astable modes.

DUAL TIMERS

The KA556/I series dual monolithic timing circuits are a highly stable controller capable of producing accurate time delays or oscillation.

The KA556 is a dual KA555. Timing is provided an external resistor and capacitor for each timing function.

The two timers operate independently of each other, sharing only V_{CC} and ground.

The circuits may be triggered and reset on falling waveforms. The output structures may sink or source 200mA.

FEATURES

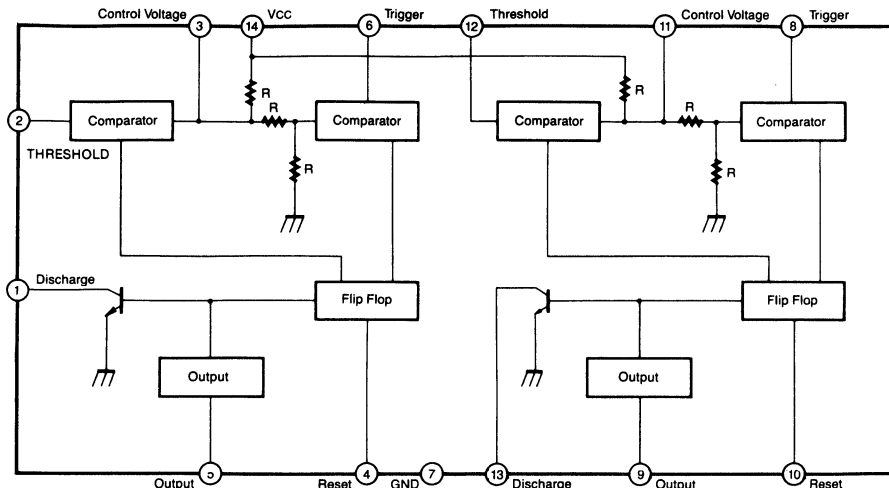
- Replaces Two KA555 Timers
- Operates in Both Astable And Monostable Modes
- High Output Current
- TTL Compatible
- Timing From Microsecond To Hours
- Adjustable Duty Cycle
- Temperature Stability Of 0.005% Per °C

APPLICATIONS

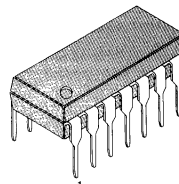
- Precision Timing
- Pulse Shaping
- Pulse Width Modulation
- Frequency Division
- Traffic Light Control

- Sequential Timing
- Pulse Generator
- Time Delay Generator
- Touch Tone Encoder
- Tone Burst Generator

BLOCK DIAGRAM



14 DIP



ORDERING INFORMATION

Device	Package	Operating Temperature
KA556	14 DIP	0 ~ +70°C
KA556I	14 DIP	-40 ~ +85°C

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Lead Temperature (soldering 10 sec)	T_{LEAD}	300	$^\circ\text{C}$
Power Dissipation	P_D	600	mW
Operating Temperature Range KA556 KA556I	T_{OPR}	0 ~ +70	$^\circ\text{C}$
		-40 ~ +85	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-65 ~ +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$, $V_{CC} = 5 \sim 15\text{V}$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		4.5		16	V
*1 Supply Current (Two timers) (low state)	I_{CC}	$V_{CC} = 5\text{V}$, $R_L = \infty$ $V_{CC} = 15\text{V}$, $R_L = \infty$		5 16	12 30	mA
*2 Timing Error (monostable) Initial Accuracy Drift with Temperature Drift with Supply Voltage	ACCUR $\Delta t/\Delta T$ $\Delta t/\Delta V_{CC}$	$R_A = 2\text{K}\Omega$ to $100\text{K}\Omega$ $C = 0.1\mu\text{F}$ $T = 1.1RC$		0.75 50 0.1		% ppm/ $^\circ\text{C}$ %/V
Control Voltage	V_C	$V_{CC} = 15\text{V}$	9.0	10.0	11.0	V
		$V_{CC} = 5\text{V}$	2.6	3.33	4.0	V
Threshold Voltage	V_{TH}	$V_{CC} = 15\text{V}$	8.8	10.0	11.2	V
		$V_{CC} = 5\text{V}$	2.4	3.33	4.2	V
*3 Threshold Current	I_{TH}			30	250	nA
Trigger Voltage	V_{TR}	$V_{CC} = 15\text{V}$	4.5	5.0	5.6	V
		$V_{CC} = 5\text{V}$	1.1	1.6	2.2	V
Trigger Current	I_{TR}	$V_{TH} = 0\text{V}$		0.01	2.0	μA
*5 Reset Voltage	V_{RST}		0.4	0.6	1.0	V
Reset Current	I_{RST}			0.03	0.6	mA
Low Output Voltage	V_{OL}	$V_{CC} = 15\text{V}$ $I_{SINK} = 10\text{mA}$		0.1	0.25	V
		$I_{SINK} = 50\text{mA}$		0.4	0.75	V
		$I_{SINK} = 100\text{mA}$		2.0	3.2	V
		$I_{SINK} = 200\text{mA}$		2.5		V
		$V_{CC} = 5\text{V}$ $I_{SINK} = 8\text{mA}$		0.25	0.35	V
		$I_{SINK} = 5\text{mA}$		0.15	0.25	V

ELECTRICAL CHARACTERISTICS(V_{CC} = 5V to +15V, T_A = 25°C unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
High Output Voltage	V _{OH}	V _{CC} = 15V				V
		I _{SOURCE} = 200mA		12.5		V
		I _{SOURCE} = 100mA	12.75	13.3		V
		V _{CC} = 5V				V
		I _{SOURCE} = 100mA	2.75	3.3		V
Rise Time of Output	t _R			100	300	nsec
Fall Time of Output	t _F			100	300	nsec
Discharge Leakage Current	I _{LKG}			10	100	nA
*4 Matching Characteristics						
Initial Accuracy	ACCUR			1.0	2.0	%
Drift with Temperature	Δt/ΔT			10		ppm/°C
Drift with Supply Voltage	Δt/ΔV _{CC}			0.2	0.5	%/V
*2 Timing Error (astable)		R _A , R _B = 1kΩ to 100kΩ				
Initial Accuracy	ACCUR	C = 0.1μF		2.25		%
Drift with Temperature	Δt/ΔT	V _{CC} = 15V		150		ppm/°C
Drift with Supply Voltage				0.3		%/V

Notes:

- *1. Supply current when output is high is typically 1.0mA less at V_{CC} = 5V.
- *2. Tested at V_{CC} = 5V and V_{CC} = 15V
- *3. This will determine the maximum value of R_A + R_B for 15V operation.
The maximum total R = 20MΩ, and for 5V operation the maximum total R = 6.6MΩ.
- *4. Matching characteristics refer to the difference between performance characteristics of each timer section in the monostable mode.
- *5. As reset voltage lowers, timing is inhibited and then the output goes low.

QUAD TIMERS

The KA558/I series are monolithic Quad Timers which can be used to produce four entirely independent timing functions. These highly stable, general purpose controllers can be used in a monostable mode to produce accurate time delays, from microseconds to hours. The time is precisely controlled by one external resistor and one capacitor in the time delay mode. A stable mode can be operated y using two of four time sections.

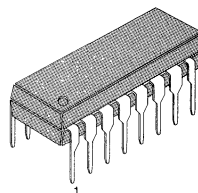
FEATURES

- Wide Supply Voltage Range: 4.5V To 16V
- 100mA Output Current Per Section
- Edge Triggered Without Coupling Capacitor
- Time Period Equals RC
- Output Independent Of Trigger Conditions

APPLICATIONS

- Quad One-Shot
- Sequential Timing
- Precision Timing
- Time Delay Generation

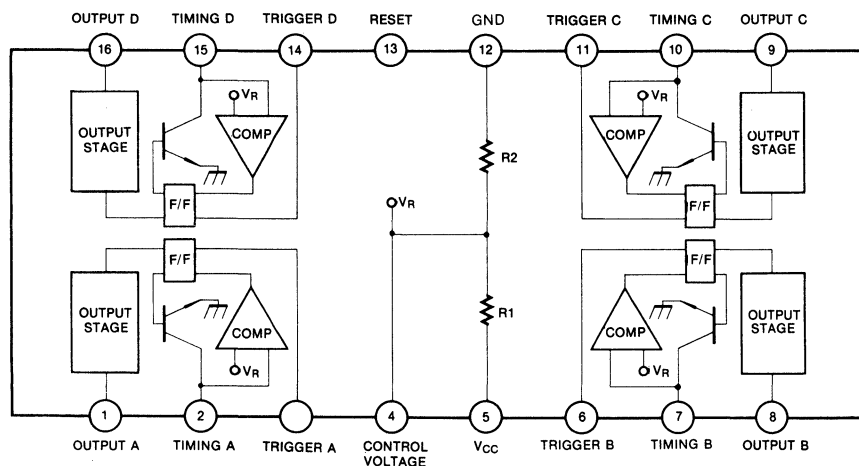
16 DIP



ORDERING INFORMATION

Device	Package	Operating Temperature
KA558	16 DIP	0 ~ +70°C
KA558I	16 DIP	-40 ~ +85°C

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Lead Temperature (soldering 10 sec)	T_{LEAD}	300	$^\circ\text{C}$
Power Dissipation	P_D	600	mW
Operating Temperature Range KA558	T_{OPR}	0 ~ +70	$^\circ\text{C}$
KA558I		-40 ~ +85	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-65 ~ +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS

($V_{CC} = 5 \sim 15\text{V}$, $T_A = 25^\circ\text{C}$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		4.5		16	V
Supply Current	I_{CC}	$V_{CC} = 15\text{V}$, reset voltage = 15V		16	36	mA
Timing Error ($T = RC$)	ACCUR	$R = 2\text{K}\Omega$ to $100\text{K}\Omega$, $C = 1\mu\text{F}$		± 2	5	%
Initial Accuracy						
Drift with Temperature				30	150	PPM/ $^\circ\text{C}$
Drift with Supply Voltage	$\Delta t/\Delta V_{CC}$			0.1	0.9	%/V
¹ Trigger Voltage	V_{TR}	$V_{CC} = 15\text{V}$	0.8	1.5	2.4	V
¹ Trigger Current	I_{TR}	Trigger voltage = 0V		5.0	100	μA
² Reset Voltage	V_{RST}	Reset	0.8	1.5	2.4	V
² Reset Current	I_{RST}	Reset		50	500	μA
Threshold Voltage	V_{TH}			$0.63 \times V_{CC}$		V
Threshold Current	I_{TH}			15		nA
³ Output Voltage	V_O	$I_L = 10\text{mA}$		0.1	0.4	V
		$I_L = 100\text{mA}$		1.0	2.0	
Output Leakage Current	I_{LKG}			10	500	nA
Propagation Delay Time	t_D			1.0		μs
Rise Time	t_R	$I_L = 100\text{mA}$		100		nS
Fall Time	t_F	$I_L = 100\text{mA}$		100		nS

- NOTES: 1. The trigger functions only on the falling edge of the trigger pulse only after previously being high. After reset the trigger must be brought high and then low to implement triggering.
2. For reset below 0.8V, outputs set low and trigger inhibited.
3. Output structure is open collector which requires a pull up resistor to V_{CC} to sink current. The output is nomally low sinking current.

3-TERMINAL LOW DROPOUT VOLTAGE REGULATOR

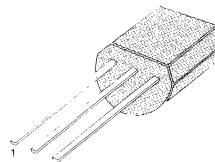
KA76L05 is an adjustable 3-terminal low dropout voltage regulator designed to need very low quiescent current.

Internally, implemented circuits include 60V load dump protection, -50V reverse transient short circuit and thermal over load protection.

FEATURES

- Limited input voltage and high efficiency.
- Internal thermal over load protection.
- 60V load dump protection.
- Output current up to 100mA.

TO-92

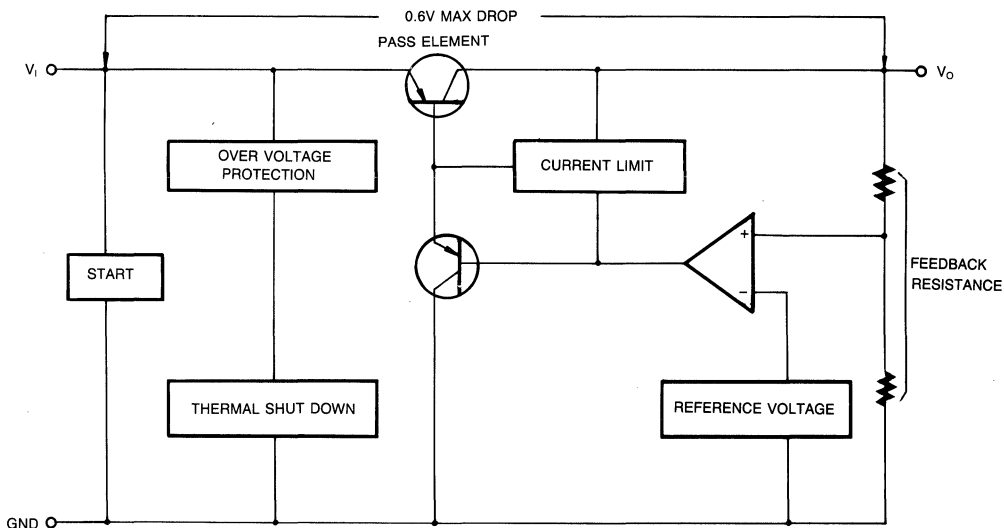


1: Input 2: GND 3: Output

ORDERING INFORMATION

Device	Package	Operating Temperature
KA76L05Z	TO-92	- 40 ~ + 125°C

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Input Voltage	V_I	33	V
Over Protection Voltage	$V_{(OP)}$	60	V
Operating Junction Temperature Range	T_{OPR}	-40 ~ +125	°C
Maximum Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{STG}	-65 ~ +150	°C

ELECTRICAL CHARACTERISTICS ($V_I = 14V$, $I_O = 10mA$, $C_O = 100\mu F$, $T_A = 25^\circ C$)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage (I)	V_O (I)	$V_I = 14V$, $I_O = 10mA$	4.81	5.0	5.19	V
Output Voltage (II)	V_O (II)	$V_I = 6 \sim 26V$, $I_O = 100mA$, $T_J = -40 \sim +125^\circ C$	4.75	5.0	5.25	V
Line Regulation (I)	ΔV_O (I)	$V_I = 9 \sim 16V$, $I_O = 10mA$	—	2.0	10	mV
Line Regulation (II)	ΔV_O (II)	$V_I = 6 \sim 26V$, $I_O = 10mA$	—	4.0	30	mV
Load Regulation	ΔV_O (III)	$V_I = 14V$, $I_O = 5 \sim 100mA$	—	10	50	mV
Output Impedance	Z_O	$V_I = 14V$, $I_O = 100mA$	—	100	600	mΩ
Quiescent Current (I)	I_Q (I)	$V_I = 6 \sim 26V$, $I_O \leq 10mA$	—	0.1	1.0	mA
Quiescent Current (II)	I_Q (II)	$V_I = 14V$, $I_O \leq 100mA$	—	5.0	30	mA
Output Noise Voltage	V_N	$V_I = 14V$, $I_O = 10mA$, $f = 10Hz \sim 100KHz$	—	150	1000	μV_{rms}
Ripple Rejection	RR	$V_I = 14V$, $I_O = 10mA$, $f = 120Hz$	55	80	—	dB
Dropout Voltage (I)	V_D (I)	$I_O = 10mA$, $V_O = V_I - V_O$	—	0.03	0.2	V
Dropout Voltage (II)	V_D (II)	$I_O = 100mA$, $V_D = V_{IN} - V_O$	—	0.1	0.6	V
Max Operational Input Voltage	V_{IN}	$I_O = 10mA$	26	33	—	V
Max Line Transient	$V_{LT (MAX)}$	$V_I = 14V$, $I_O = 10mA$, Time = 100ms	60	70	—	V
Reverse Polarity Input Voltage DC	$V_{I (DC)}$	$V_I = 14V$, $I_O = 10mA$, $V_O \geq -0.3V$	-15	-30	—	V
Reverse Polarity Input Voltage Transient	$V_{I (TR)}$	$V_I = 14V$, $I_O = 10mA$, Time $\leq 10ms$	-50	-80	—	V
Peak Output Current	I_{PK}	$V_I = 14V$	200	400	600	mA

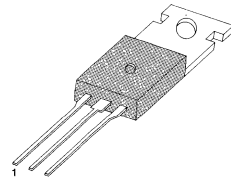
3-TERMINAL 1A POSITIVE VOLTAGE REGULATORS

The KA78XX series of three-terminal positive regulators are available in the TO-220 package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

FEATURES

- Output Current up to 1A
- Output Voltages of 5; 6; 8; 9; 10; 11; 12; 15; 18; 24V
- Thermal Overload Protection
- Short Circuit Protection
- Output Transistor SOA Protection

TO-220

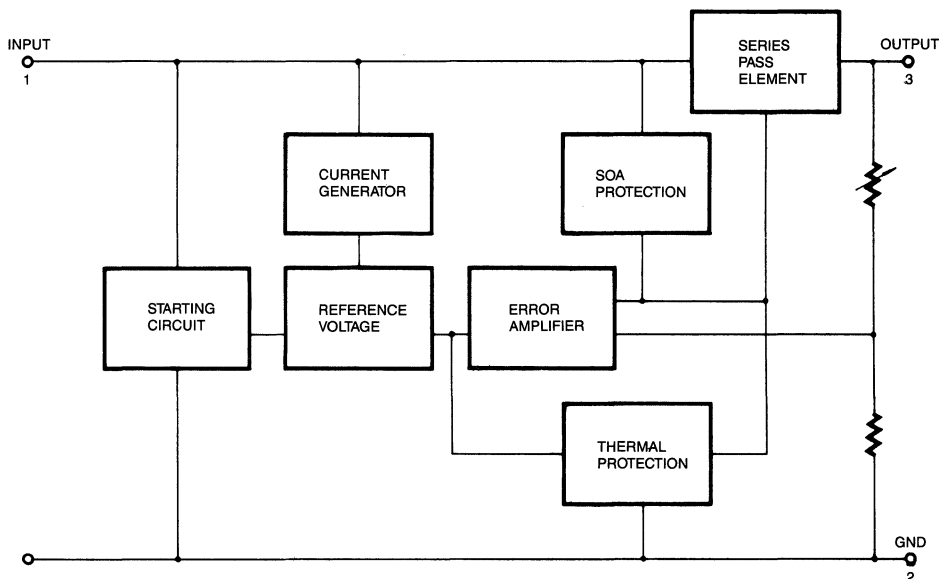


1: Input 2: GND 3: Output

ORDERING INFORMATION

Device	Package	Operating Temperature
KA78XX	TO-220	0 ~ +125°C
KA78XXA	TO-220	
KA78XXI	TO-220	-40 ~ +125°C

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Characteristic	Symbol	Value	Unit
Input Voltage (for $V_O = 5\text{V}$ to 18V) (for $V_O = 24\text{V}$)	V_I	35	V
	V_I	40	V
Thermal Resistance Junction-Cases	$R_{\theta JC}$	5	$^\circ\text{C/W}$
Thermal Resistance Junction-Air	$R_{\theta JA}$	65	$^\circ\text{C/W}$
Operating Junction Temperature Range KA78XX/A KA78XXI	T_{OPR}	$0 \sim +125$	$^\circ\text{C}$
		$-40 \sim +125$	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	$-65 \sim +150$	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS KA7805/I

(Refer to test circuit, $T_{MIN} < T_J < T_{MAX}$, $I_O = 500\text{mA}$, $V_I = 10\text{V}$, $C_I = 0.33\mu\text{F}$, $C_O = 0.1\mu\text{F}$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		KA7805I			KA7805			Unit
				Min	Typ	Max	Min	Typ	Max	
Output Voltage	V _O	T _J = 25°C		4.8	5.0	5.2	4.8	5.0	5.2	V
		5.0mA ≤ 1.0A, P _O ≤ 15W V _I = 7V to 20V V _I = 8V to 20V		4.75	5.0	5.25	4.75	5.0	5.25	
Line Regulation	ΔV _O	T _J = 25°C	V _I = 7V to 25V		4.0	100		4.0	100	mV
			V _I = 8V to 12V		1.6	50		1.6	50	
Load Regulation	ΔV _O	T _J = 25°C	I _O = 5.0mA to 1.5A		9	100		9	100	mV
			I _O = 250mA to 750mA		4	50		4	50	
Quiescent Current	I _Q	T _J = 25°C			5.0	8		5.0	8	mA
Quiescent Current Change	ΔI _Q	I _O = 5mA to 1.0A			0.03	0.5		0.03	0.5	mA
		V _I = 7V to 25V						0.3	1.3	
		V _I = 8V to 25V			0.3	1.3				
Output Voltage Drift	ΔV _O /ΔT	I _O = 5mA			−0.8			−0.8		mV/°C
Output Noise Voltage	V _N	f = 10Hz to 100KHz T _A = 25°C			42			42		μV
Ripple Rejection	RR	f = 120Hz V _I = 8 to 18V		62	73		62	73		dB
Dropout Voltage	V _O	I _O = 1A, T _J = 25°C			2			2		V
Output Resistance	R _O	f = 1KHz			15			15		mΩ
Short Circuit Current	I _{SC}	V _I = 35V, T _A = 25°C			230			230		mA
Peak Current	I _{PK}	T _J = 25°C			2.2			2.2		A

* $T_{MIN} < T_J < T_{MAX}$ KA78XXI: $T_{MIN} = -40^\circ\text{C}$, $T_{MAX} = 125^\circ\text{C}$ KA78XX, $T_{MIN} = 0^\circ\text{C}$, $T_{MAX} = 125^\circ\text{C}$ * Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

ELECTRICAL CHARACTERISTICS KA7806/I(Refer to test circuit, $T_{\text{MIN}} < T_J < T_{\text{MAX}}$, $I_O = 500\text{mA}$, $V_I = 11\text{V}$, $C_I = 0.33\mu\text{F}$, $C_O = 0.1\mu\text{F}$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		KA7806I			KA7806			Unit
				Min	Typ	Max	Min	Typ	Max	
Output Voltage	V _o	T _J = 25°C		5.75	6.0	6.25	5.75	6.0	6.25	V
		5.0mA ≤ i _o ≤ 1.0A, P _O ≤ 15W V _I = 8.0V to 21V V _I = 9.0V to 21V								
				5.7	6.0	6.3		5.7	6.0	
Line Regulation	ΔV _o	T _J = 25°C	V _I = 8V to 25V		5	120		5	120	mV
			V _I = 9V to 13V		1.5	60		1.5	60	
Load Regulation	ΔV _o	T _J = 25°C	i _o = 5mA to 1.5A		9	120		9	120	mV
			i _o = 250mA to 750mA		3	60		3	60	
Quiescent Current	I _Q	T _J = 25°C			5.0	8		5.0	8	mA
Quiescent Current Change	ΔI _Q	i _o = 5mA to 1A					0.5		0.5	mA
		V _I = 8V to 25V							1.3	
		V _I = 9V to 25V					1.3			
Output Voltage Drift	ΔV _o /ΔT	i _o = 5mA			- 0.8			- 0.8		mV/°C
Output Noise Voltage	V _N	f = 10Hz to 100KHz, T _A = 25°C				45			45	μV
Ripple Rejection	RR	f = 120Hz V _I = 9 to 19V			59	75		59	75	dB
Dropout Voltage	V _D	i _o = 1A, T _J = 25°C				2			2	V
Output Resistance	R _o	f = 1KHz				19			19	mΩ
Short Circuit Current	I _{sc}	V _I = 35V, T _A = 25°C				250			250	mA
Peak Current	I _{PK}	T _J = 25°C				2.2			2.2	A

* $T_{\text{MIN}} < T_J < T_{\text{MAX}}$ KA78XXI: $T_{\text{MIN}} = -40^\circ\text{C}$, $T_{\text{MAX}} = 125^\circ\text{C}$ KA78XX, $T_{\text{MIN}} = 0^\circ\text{C}$, $T_{\text{MAX}} = 125^\circ\text{C}$ * Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

ELECTRICAL CHARACTERISTICS KA7808/I

(Refer to test circuit, $T_{MIN} < T_J < T_{MAX}$, $I_O = 500mA$, $V_I = 14V$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	KA7808I			KA7808			Unit
			Min	Typ	Max	Min	Typ	Max	
Output Voltage	V _O	T _J = 25°C	7.7	8.0	8.3	7.7	8.0	8.3	V
		5.0mA ≤ I _O ≤ 1.0A, P _D ≤ 15W V _I = 10.5V to 23V V _I = 11.5V to 23V							
			7.6	8.0	8.4	7.6	8.0	8.4	
Line Regulation	ΔV _O	T _J = 25°C	V _I = 10.5V to 25V	5.0	160		5.0	160	mV
			V _I = 11.5V to 17V	2.0	80		2.0	80	
Load Regulation	ΔV _O	T _J = 25°C	I _O = 5.0mA to 1.5A	10	160		10	160	mV
			I _O = 250mA to 750mA	5.0	80		5.0	80	
Quiescent Current	I _Q	T _J = 25°C		5.0	8		5.0	8	mA
Quiescent Current Change	ΔI _Q	I _O = 5mA to 1.0A		0.05	0.5		0.05	0.5	mA
		V _I = 10.5V to 25V					0.5	1.0	
		V _I = 11.5V to 25V		0.5	1.0				
Output Voltage Drift	ΔV _O /ΔT	I _O = 5mA		−0.8			−0.8		mV/°C
Output Noise Voltage	V _N	f = 10Hz to 100KHz, T _A = 25°C		52			52		μV
Ripple Rejection	RR	f = 120Hz, V _I = 11.5V to 21.5	56	73		56	73		dB
Dropout Voltage	V _D	I _O = 1A, T _J = 25°C		2			2		V
Output Resistance	R _O	f = 1KHz		17			17		mΩ
Short Circuit Current	I _{SC}	V _I = 35V, T _A = 25°C		230			230		mA
Peak Current	I _{PK}	T _J = 25°C		2.2			2.2		A

* $T_{MIN} < T_J < T_{MAX}$

KA78XXI: $T_{MIN} = -40^\circ C$, $T_{MAX} = 125^\circ C$

KA78XX, $T_{MIN} = 0^\circ C$, $T_{MAX} = 125^\circ C$

* Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

ELECTRICAL CHARACTERISTICS KA7809/I(Refer to test circuit, $T_{\text{MIN}} < T_J < T_{\text{MAX}}$, $I_O = 500\text{mA}$, $V_I = 15\text{V}$, $C_I = 0.33\mu\text{F}$, $C_O = 0.1\mu\text{F}$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		KA7809I			KA7809			Unit
				Min	Typ	Max	Min	Typ	Max	
Output Voltage	V _o	T _J = 25°C		8.65	9	9.35	8.65	9	9.35	V
		5.0mA ≤ I _o ≤ 1.0A, P _o ≤ 15W V _I = 11.5V to 24V V _I = 12.5V to 24V		8.6	9	9.4	8.6	9	9.4	
Line Regulation	Δ V _o	T _J = 25°C	V _I = 11.5V to 25V		6	180		6	180	mV
			V _I = 12V to 25V		2	90		2	90	
Load Regulation	Δ V _o	T _J = 25°C	I _o = 5mA to 1.5A		12	180		12	180	mV
			I _o = 250mA to 750mA		4	90		4	90	
Quiescent Current	I _q	T _J = 25°C			5.0	8		5.0	8.0	mA
Quiescent Current Change	ΔI _q	I _o = 5mA to 1.0A				0.5			0.5	mA
		V _I = 11.5V to 26V							1.3	
		V _I = 12.5V to 26V				1.3				
Output Voltage Drift	Δ V _o /Δ T	I _o = 5mA			− 1			− 1		mV/°C
Output Noise Voltage	V _N	f = 10Hz to 100KHz, T _A = 25°C			58			58		μV
Ripple Rejection	RR	f = 120Hz V _I = 13V to 23V		56	71		56	71		dB
Dropout Voltage	V _D	I _o = 1A, T _J = 25°C			2			2		V
Output Resistance	R _O	f = 1KHz			17			17		mΩ
Short Circuit Current	I _{SC}	V _I = 35V, T _A = 25°C			250			250		mA
Peak Current	I _{PK}	T _J = 25°C			2.2			2.2		A

* $T_{\text{MIN}} < T_J < T_{\text{MAX}}$ KA78XXI: $T_{\text{MIN}} = -40^\circ\text{C}$, $T_{\text{MAX}} = 125^\circ\text{C}$ KA78XX, $T_{\text{MIN}} = 0^\circ\text{C}$, $T_{\text{MAX}} = 125^\circ\text{C}$ * Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

ELECTRICAL CHARACTERISTICS KA7810/I(Refer to test circuit, $T_{\text{MIN}} < T_J < T_{\text{MAX}}$, $I_o = 500\text{mA}$, $V_i = 16\text{V}$, $C_i = 0.33\mu\text{F}$, $C_o = 0.1\mu\text{F}$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	KA7810I			KA7810			Unit
			Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_o	$T_J = 25^\circ\text{C}$	9.6	10	10.4	9.6	10	10.4	V
		$5.0\text{mA} \leq I_o \leq 1.0\text{A}$, $P_D \leq 15\text{W}$ $V_i = 12.5\text{V to } 25\text{V}$ $V_i = 13.5\text{V to } 25\text{V}$				9.5	10	10.5	
			9.5	10	10.5				
Line Regulation	ΔV_o	$T_J = 25^\circ\text{C}$	$V_i = 12.5\text{V to } 25\text{V}$				10	200	mV
			$V_i = 13\text{V to } 20\text{V}$				3	100	
Load Regulation	ΔV_o	$T_J = 25^\circ\text{C}$	$I_o = 5\text{mA to } 1.5\text{A}$				12	200	mV
			$I_o = 250\text{mA to } 750\text{mA}$				4	100	
Quiescent Current	I_Q	$T_J = 25^\circ\text{C}$		5.1	8		5.1	8	mA
Quiescent Current Change	ΔI_Q	$I_o = 5\text{mA to } 1.0\text{A}$			0.5			0.5	mA
		$V_i = 12.5\text{V to } 29\text{V}$						1.0	
		$V_i = 13.5\text{V to } 29\text{V}$			1.0				
Output Voltage Drift	$\Delta V_o / \Delta T$	$I_o = 5\text{mA}$		-1			-1		mV/ $^\circ\text{C}$
Output Noise Voltage	V_N	$f = 10\text{Hz to } 100\text{kHz}$, $T_A = 25^\circ\text{C}$		58			58		μV
Ripple Rejection	RR	$f = 120\text{Hz}$ $V_i = 14\text{V to } 24\text{V}$	56	71		56	71		dB
Dropout Voltage	V_D	$I_o = 1\text{A}$, $T_J = 25^\circ\text{C}$		2			2		V
Output Resistance	R_o	$f = 1\text{KHz}$		17			17		$\text{m}\Omega$
Short Circuit Current	I_{SC}	$V_i = 35\text{V}$, $T_A = 25^\circ\text{C}$		250			250		mA
Peak Current	I_{PK}	$T_J = 25^\circ\text{C}$		2.2			2.2		A

* $T_{\text{MIN}} < T_J < T_{\text{MAX}}$ KA78XXI: $T_{\text{MIN}} = -40^\circ\text{C}$, $T_{\text{MAX}} = 125^\circ\text{C}$ KA78XX, $T_{\text{MIN}} = 0^\circ\text{C}$, $T_{\text{MAX}} = 125^\circ\text{C}$ * Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty is used.

ELECTRICAL CHARACTERISTICS KA7811/I(Refer to test circuit, $T_{\text{MIN}} < T_J < T_{\text{MAX}}$, $I_O = 500\text{mA}$, $V_I = 18\text{V}$, $C_I = 0.33\mu\text{F}$, $C_O = 0.1\mu\text{F}$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	KA7811I			KA7811			Unit	
			Min	Typ	Max	Min	Typ	Max		
Output Voltage	V _O	T _J = 25°C	10.6	11	11.4	10.6	11	11.4	V	
		5.0mA ≤ I _O ≤ 1.0A, P _D ≤ 15W V _I = 13.5V to 26V V _I = 14.5V to 26V								
			10.5	11	11.5	10.5	11	11.5		
Line Regulation	Δ V _O	T _J = 25°C	V _I = 13.5 to 25V		10	220		10	220	mV
			V _I = 14 to 21V		3.0	110		3.0	110	
Load Regulation	Δ V _O	T _J = 25°C	I _O = 5.0mA to 1.5A		12	220		12	220	mV
			I _O = 250mA to 750mA		4	110		4	110	
Quiescent Current	I _Q	T _J = 25°C		5.1	8		5.1	8	mA	
Quiescent Current Change	ΔI _Q	I _O = 5mA to 1A			0.5			0.5	mA	
		V _I = 13.5V to 29V					1.0			
		V _I = 14.5V to 29V			1.0					
Output Voltage Drift	Δ V _O /Δ T	I _O = 5mA		− 1			− 1		mV/°C	
Output Noise Voltage	V _N	f = 10Hz to 100KHz, T _A = 25°C		70			70		μV	
Ripple Rejection	RR	f = 120Hz V _I = 14V to 24V	55	71		55	71		dB	
Dropout Voltage	V _D	I _O = 1A, T _J = 25°C		2			2		V	
Output Resistance	R _O	f = 1KHz		18			18		mΩ	
Short Circuit Current	I _{SC}	V _I = 35V, T _A = 25°C		250			250		mA	
Peak Current	I _{PK}	T _J = 25°C		2.2			2.2		A	

* $T_{\text{MIN}} < T_J < T_{\text{MAX}}$ KA78XXI: $T_{\text{MIN}} = -40^\circ\text{C}$, $T_{\text{MAX}} = 125^\circ\text{C}$ KA78XX, $T_{\text{MIN}} = 0^\circ\text{C}$, $T_{\text{MAX}} = 125^\circ\text{C}$ * Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

ELECTRICAL CHARACTERISTICS KA7812/I(Refer to test circuit, $T_{\min} < T_J < T_{\max}$, $I_O = 500\text{mA}$, $V_I = 19\text{V}$, $C_I = 0.33\mu\text{F}$, $C_O = 0.1\mu\text{F}$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	KA7812I			KA7812			Unit
			Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_O	$T_J = 25^\circ\text{C}$	11.5	12	12.5	11.5	12	12.5	V
		$5.0\text{mA} \leq I_O \leq 1.0\text{A}$, $P_O \leq 15\text{W}$							
		$V_I = 14.5\text{V to } 27\text{V}$ $V_I = 15.5\text{V to } 27\text{V}$	11.4	12	12.6	11.4	12	12.6	
Line Regulation	ΔV_O	$T_J = 25^\circ\text{C}$	$V_I = 14.5 \text{ to } 30\text{V}$				10	240	mV
			$V_I = 16 \text{ to } 22\text{V}$				3.0	120	
Load Regulation	ΔV_O	$T_J = 25^\circ\text{C}$	$I_O = 5\text{mA to } 1.5\text{A}$				11	240	mV
			$I_O = 250\text{mA to } 750\text{mA}$				5.0	120	
Quiescent Current	I_Q	$T_J = 25^\circ\text{C}$		5.1	8		5.1	8	mA
Quiescent Current Change	ΔI_Q	$I_O = 5\text{mA to } 1.0\text{A}$		0.1	0.5		0.1	0.5	mA
		$V_I = 14.5\text{V to } 30\text{V}$					0.5	1.0	
		$V_I = 15\text{V to } 30\text{V}$		0.5	1.0				
Output Voltage Drift	$\Delta V_O / \Delta T$	$I_O = 5\text{mA}$		-1			-1		mV/ $^\circ\text{C}$
Output Noise Voltage	V_N	$f = 10\text{Hz to } 100\text{KHz}$, $T_A = 25^\circ\text{C}$		76			76		μV
Ripple Rejection	RR	$f = 120\text{Hz}$ $V_I = 15\text{V to } 25\text{V}$	55	71		55	71		dB
Dropout Voltage	V_D	$I_O = 1\text{A}$, $T_J = 25^\circ\text{C}$		2			2		V
Output Resistance	R_O	$f = 1\text{KHz}$		18			18		$\text{m}\Omega$
Short Circuit Current	I_{SC}	$V_I = 35\text{V}$, $T_A = 25^\circ\text{C}$		230			230		mA
Peak Current	I_{PK}	$T_J = 25^\circ\text{C}$		2.2			2.2		A

* $T_{\min} < T_J < T_{\max}$ KA78XXI: $T_{\min} = -40^\circ\text{C}$, $T_{\max} = 125^\circ\text{C}$ KA78XX, $T_{\min} = 0^\circ\text{C}$, $T_{\max} = 125^\circ\text{C}$ * Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

ELECTRICAL CHARACTERISTICS KA7815/I(Refer to test circuit, $T_{MIN} < T_J < T_{MAX}$, $I_O = 500mA$, $V_I = 23V$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	KA7815I			KA7815			Unit
			Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_O	$T_J = 25^\circ C$	14.4	15	15.6	14.4	15	15.6	V
		$5.0mA \leq I_O \leq 1.0A$, $P_O \leq 15W$ $V_I = 17.5V$ to $30V$ $V_I = 18.5V$ to $30V$	14.25	15	15.75	14.25	15	15.75	
Line Regulation	ΔV_O	$T_J = 25^\circ C$		$V_I = 17.5$ to $30V$	11	300	11	300	mV
				$V_I = 20$ to $26V$	3	150	3	150	
Load Regulation	ΔV_O	$T_J = 25^\circ C$		$I_O = 5.0mA$ to $1.5A$	12	300	12	300	mV
				$I_O = 250mA$ to $750mA$	4	150	4	150	
Quiescent Current	I_Q	$T_J = 25^\circ C$		5.2	8	5.2	8		mA
Quiescent Current Change	ΔI_Q	$I_O = 5mA$ to $1.0A$			0.5			0.5	mA
		$V_I = 17.5V$ to $30V$						1.0	
		$V_I = 18.5V$ to $30V$			1.0				
Output Voltage Drift	$\Delta V_O / \Delta T$	$I_O = 5mA$		- 1		- 1			mV/ $^\circ C$
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$, $T_A = 25^\circ C$		90		90			μV
Ripple Rejection	RR	$f = 120Hz$ $V_I = 18.5$ to $28.5V$	54	70		54	70		dB
Dropout Voltage	V_D	$I_O = 1A$, $T_J = 25^\circ C$		2		2			V
Output Resistance	R_O	$f = 1KHz$		19		19			m Ω
Short Circuit Current	I_{SC}	$V_I = 35V$, $T_A = 25^\circ C$		250		250			mA
Peak Current	I_{PK}	$T_J = 25^\circ C$		2.2		2.2			A

* $T_{MIN} < T_J < T_{MAX}$ KA78XXI: $T_{MIN} = -40^\circ C$, $T_{MAX} = 125^\circ C$ KA78XX, $T_{MIN} = 0^\circ C$, $T_{MAX} = 125^\circ C$ * Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

ELECTRICAL CHARACTERISTICS KA7818/I(Refer to test circuit, $T_{\text{MIN}} < T_J < T_{\text{MAX}}$, $I_o = 500\text{mA}$, $V_i = 27\text{V}$, $C_i = 0.33\mu\text{F}$, $C_o = 0.1\mu\text{F}$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	KA7818I			KA7818			Unit	
			Min	Typ	Max	Min	Typ	Max		
Output Voltage	V _o	T _J = 25°C	17.3	18	18.7	17.3	18	18.7	V	
		5.0mA ≤ I _o ≤ 1.0A, P _D ≤ 15W								
		V _I = 21V to 33V V _I = 22V to 33V	17.1	18	18.9	17.1	18	18.9		
Line Regulation	Δ V _o	T _J = 25°C	V _I = 21 to 33V		15	360		15	360	mV
			V _I = 24 to 30V		5	180		5	180	
Load Regulation	Δ V _o	T _J = 25°C	I _o = 5mA to 1.5A		15	360		15	360	mV
			I _o = 250mA to 750mA		5.0	180		5.0	180	
Quiescent Current	I _Q	T _J = 25°C		5.2	8		5.2	8	mA	
Quiescent Current Change	Δ I _Q	I _o = 5mA to 1A			0.5			0.5	mA	
		V _I = 21V to 33V						1		
		V _I = 22V to 33V			1					
Output Voltage Drift	Δ V _o /Δ T	I _o = 5mA		− 1			− 1		mV/°C	
Output Noise Voltage	V _N	f = 10Hz to 100KHz, T _A = 25°C		110			110		μV	
Ripple Rejection	RR	f = 120Hz V _I = 22V to 32V	53	69		53	69		dB	
Dropout Voltage	V _D	I _o = 1A, T _J = 25°C		2			2		V	
Output Resistance	R _O	f = 1KHz		22			22		mΩ	
Short Circuit Current	I _{SC}	V _I = 35V, T _A = 25°C		250			250		mA	
Peak Current	I _{PK}	T _J = 25°C		2.2			2.2		A	

* $T_{\text{MIN}} < T_J < T_{\text{MAX}}$ KA78XXI: $T_{\text{MIN}} = -40^\circ\text{C}$, $T_{\text{MAX}} = 125^\circ\text{C}$ KA78XX, $T_{\text{MIN}} = 0^\circ\text{C}$, $T_{\text{MAX}} = 125^\circ\text{C}$ * Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty is used.

ELECTRICAL CHARACTERISTICS KA7824/I(Refer to test circuit, $T_{\text{MIN}} < T_J < T_{\text{MAX}}$, $I_o = 500\text{mA}$, $V_i = 33\text{V}$, $C_i = 0.33\mu\text{F}$, $C_o = 0.1\mu\text{F}$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	KA7824I			KA7824			Unit
			Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_o	$T_J = 25^\circ\text{C}$	23	24	25	23	24	25	V
		$5.0\text{mA} \leq I_o \leq 1.0\text{A}$, $P_D \leq 15\text{W}$							
		$V_i = 27\text{V to } 38\text{V}$ $V_i = 28\text{V to } 38\text{V}$	22.8	24	25.2	22.8	24	25.2	
Line Regulation	ΔV_o	$T_J = 25^\circ\text{C}$	$V_i = 27\text{V to } 38\text{V}$				17	480	mV
			$V_i = 30\text{V to } 36\text{V}$				6	240	
Load Regulation	ΔV_o	$T_J = 25^\circ\text{C}$	$I_o = 5\text{mA to } 1.5\text{A}$				15	480	mV
			$I_o = 250\text{mA to } 750\text{mA}$				5.0	240	
Quiescent Current	I_q	$T_J = 25^\circ\text{C}$		5.2	8		5.2	8	mA
Quiescent Current Change	ΔI_q	$I_o = 5\text{mA to } 1\text{A}$		0.1	0.5		0.1	0.5	mA
		$V_i = 27\text{V to } 38\text{V}$					0.5	1	
		$V_i = 28\text{V to } 38\text{V}$		0.5	1				
Output Voltage Drift	$\Delta V_o / \Delta T$	$I_o = 5\text{mA}$		-1.5			-1.5		mV/ $^\circ\text{C}$
Output Noise Voltage	V_N	$f = 10\text{Hz to } 100\text{KHz}$, $T_A = 25^\circ\text{C}$		160			160		μV
Ripple Rejection	RR	$f = 120\text{Hz}$ $V_i = 28\text{V to } 38\text{V}$	50	67		50	67		dB
Dropout Voltage	V_D	$I_o = 1\text{A}$, $T_J = 25^\circ\text{C}$		2			2		V
Output Resistance	R_o	$f = 1\text{KHz}$		28			28		$\text{m}\Omega$
Short Circuit Current	I_{SC}	$V_i = 35\text{V}$, $T_A = 25^\circ\text{C}$		230			230		mA
Peak Current	I_{PK}	$T_J = 25^\circ\text{C}$		2.2			2.2		A

* $T_{\text{MIN}} < T_J < T_{\text{MAX}}$ KA78XXI: $T_{\text{MIN}} = -40^\circ\text{C}$, $T_{\text{MAX}} = 125^\circ\text{C}$ KA78XX, $T_{\text{MIN}} = 0^\circ\text{C}$, $T_{\text{MAX}} = 125^\circ\text{C}$ * Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty is used.

ELECTRICAL CHARACTERISTICS KA7805A(Refer to the test circuits, $T_J = 0$ to 125°C , $I_O = 1\text{A}$, $V_I = 10\text{V}$, $C_I = 0.33\mu\text{F}$, $C_O = 0.1\mu\text{F}$ unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_O	$T_J = 25^\circ\text{C}$	4.9	5	5.1	V
		$I_O = 5\text{mA}$ to 1A , $P_D \leq 15\text{W}$ $V_I = 7.5$ to 20V	4.8	5	5.2	
*Line Regulation	ΔV_O	$V_I = 7.5$ to 25V , $I_O = 500\text{mA}$		5	50	mV
		$V_I = 8\text{V}$ to 12V		3	50	
		$T_J = 25^\circ\text{C}$ $V_I = 7.3\text{V}$ to 25V		5	50	
		$V_I = 8\text{V}$ to 12V		1.5	25	
*Load Regulation	ΔV_O	$T_J = 25^\circ\text{C}$ $I_O = 5\text{mA}$ to 1.5A		9	100	mV
		$I_O = 5\text{mA}$ to 1A		9	100	
		$I_O = 250$ to 750mA		4	50	
Quiescent Current	I_Q	$T_J = 25^\circ\text{C}$		5.0	6	mA
Quiescent Current Change	ΔI_Q	$I_O = 5\text{mA}$ to 1A			0.5	mA
		$V_I = 8$ to 25V , $I_O = 500\text{mA}$			0.8	
		$V_I = 7.5$ to 20V , $T_J = 25^\circ\text{C}$			0.8	
Output Voltage Drift	$\frac{\Delta V_O}{\Delta T}$	$I_O = 5\text{mA}$		-0.8		mV/ $^\circ\text{C}$
Output Noise Voltage	V_N	$f = 10\text{Hz}$ to 100KHz : $T_A = 25^\circ\text{C}$		10		$\frac{\mu\text{V}}{V_O}$
Ripple Rejection	RR	$f = 120\text{Hz}$, $I_O = 500\text{mA}$ $V_I = 8$ to 18V		68		dB
Dropout Voltage	V_D	$I_O = 1\text{A}$, $T_J = 25^\circ\text{C}$		2		V
Output Resistance	R_O	$f = 1\text{KHz}$		17		m Ω
Short Circuit Current	I_{sc}	$V_I = 35\text{V}$, $T_A = 25^\circ\text{C}$		250		mA
Peak Current	I_{PK}	$T_J = 25^\circ\text{C}$		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS KA7806A(Refer to the test circuits, $T_J = 0$ to 150°C , $I_O = 1\text{A}$, $V_I = 11\text{V}$, $C_I = 0.33\mu\text{F}$, $C_O = 0.1\mu\text{F}$ unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_O	$T_J = 25^\circ\text{C}$	5.88	6	6.12	V
		$I_O = 5\text{mA}$ to 1A , $P_D \leq 15\text{W}$ $V_I = 8.6$ to 21V	5.76	6	6.24	
*Line Regulation	ΔV_O	$V_I = 8.6$ to 25V , $I_O = 500\text{mA}$		5	60	mV
		$V_I = 9$ to 13V		3	60	
		$T_J = 25^\circ\text{C}$	$V_I = 8.3$ to 21V	5	60	
			$V_I = 9$ to 13V	1.5	30	
*Load Regulation	ΔV_O	$T_J = 25^\circ\text{C}$ $I_O = 5\text{mA}$ to 1.5A		9	100	mV
		$I_O = 5\text{mA}$ to 1A		4	100	
		$I_O = 250$ to 750mA		5.0	50	
Quiescent Current	I_Q	$T_J = 25^\circ\text{C}$		4.3	6	mA
Quiescent Current Change	ΔI_Q	$I_O = 5\text{mA}$ to 1A			0.5	mA
		$V_I = 9$ to 25V , $I_O = 500\text{mA}$			0.8	
		$V_I = 8.6$ to 21V , $T_J = 25^\circ\text{C}$			0.8	
Output Voltage Drift	$\frac{\Delta V_O}{\Delta T}$	$I_O = 5\text{mA}$		-0.8		mV/ $^\circ\text{C}$
Output Noise Voltage	V_N	$f = 10\text{Hz}$ to 100KHz $T_A = 25^\circ\text{C}$		10		$\frac{\mu\text{V}}{V_O}$
Ripple Rejection	RR	$f = 120\text{Hz}$, $I_O = 500\text{mA}$ $V_I = 9$ to 19V		65		dB
Dropout Voltage	V_D	$I_O = 1\text{A}$, $T_J = 25^\circ\text{C}$		2		V
Output Resistance	R_O	$f = 1\text{KHz}$		17		$\text{m}\Omega$
Short Circuit Current	I_{sc}	$V_I = 35\text{V}$, $T_A = 25^\circ\text{C}$		250		mA
Peak Current	I_{PK}	$T_J = 25^\circ\text{C}$		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS KA7808A

(Refer to the test circuits, $T_J = 0$ to 150°C , $I_O = 1\text{A}$, $V_I = 14\text{V}$, $C_I = 0.33\mu\text{F}$, $C_O = 0.1\mu\text{F}$ unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_O	$T_J = 25^\circ\text{C}$	7.84	8	8.16	V
		$I_O = 5\text{mA}$ to 1A , $P_D \leq 15\text{W}$ $V_I = 10.6$ to 23V	7.7	8	8.3	
*Line Regulation	ΔV_O	$V_I = 10.6$ to 25V , $I_O = 500\text{mA}$		6	80	mV
		$V_I = 11$ to 17V		3	80	
		$T_J = 25^\circ\text{C}$ $V_I = 10.4$ to 23V		6	80	
		$V_I = 11$ to 17V		2	40	
*Load Regulation	ΔV_O	$T_J = 25^\circ\text{C}$ $I_O = 5\text{mA}$ to 1.5A		12	100	mV
		$I_O = 5\text{mA}$ to 1A		12	100	
		$I_O = 250$ to 750mA		5	50	
Quiescent Current	I_Q	$T_J = 25^\circ\text{C}$		5.0	6	mA
Quiescent Current Change	ΔI_Q	$I_O = 5\text{mA}$ to 1A			0.5	mA
		$V_I = 11$ to 25V , $I_O = 500\text{mA}$			0.8	
		$V_I = 10.6$ to 23V , $T_J = 25^\circ\text{C}$			0.8	
Output Voltage Drift	$\frac{\Delta V_O}{\Delta T}$	$I_O = 5\text{mA}$		-0.8		mV/ $^\circ\text{C}$
Output Noise Voltage	V_N	$f = 10\text{Hz}$ to 100KHz $T_A = 25^\circ\text{C}$		10		$\frac{\mu\text{V}}{V_O}$
Ripple Rejection	RR	$f = 120\text{Hz}$, $I_O = 500\text{mA}$ $V_I = 11.5$ to 21.5V		62		dB
Dropout Voltage	V_O	$I_O = 1\text{A}$, $T_J = 25^\circ\text{C}$		2		V
Output Resistance	R_O	$f = 1\text{KHz}$		18		$\text{m}\Omega$
Short Circuit Current	I_{sc}	$V_I = 35\text{V}$, $T_A = 25^\circ\text{C}$		250		mA
Peak Current	I_{PK}	$T_J = 25^\circ\text{C}$		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS KA7809A(Refer to the test circuits, $T_J = 0$ to 125°C , $I_o = 1\text{A}$, $V_I = 15\text{V}$, $C_I = 0.33\mu\text{F}$, $C_O = 0.1\mu\text{F}$ unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	$T_J = 25^\circ\text{C}$	8.82	9.0	9.18	V
		$I_o = 5\text{mA}$ to 1.0A , $P_D \leq 15\text{W}$ $V_I = 11.2\text{V}$ to 24V	8.65	9.0	9.35	
Line Regulation	ΔV_o	$V_I = 11.7\text{V}$ to 25V $I_o = 500\text{mA}$		6	90	mV
		$V_I = 12.5\text{V}$ to 19V		4	45	
		$T_J = 25^\circ\text{C}$		6	90	
				2	45	
Load Regulation	ΔV_o	$T_J = 25^\circ\text{C}$ $I_o = 5\text{mA}$ to 1.0A		12	100	mV
		$I_o = 5\text{mA}$ to 1.0A		12	100	
		$I_o = 250\text{mA}$ to 750mA		5	50	
Quiescent Current	I_q	$T_J = 25^\circ\text{C}$		5.0	6.0	mA
Quiescent Current Change	ΔI_q	$V_I = 11.7\text{V}$ to 24V , $T_J = 25^\circ\text{C}$			0.8	mA
		$V_I = 12\text{V}$ to 25V , $I_o = 500\text{mA}$			0.8	
		$I_o = 5\text{mA}$ to 1.0A			0.5	
Output Voltage Drift	$\Delta V_o / \Delta T$	$I_o = 5\text{mA}$		- 1.0		mV/ $^\circ\text{C}$
Output Noise Voltage	V_N	$f = 10\text{Hz}$ to 100KHz , $T_A = 25^\circ\text{C}$		10		$\mu\text{V}/V_o$
Ripple Rejection	RR	$f = 120\text{Hz}$, $V_I = 12\text{V}$ to 22V $I_o = 500\text{mA}$		62		dB
Dropout Voltage	V_D	$I_o = 1.0\text{A}$, $T_J = 25^\circ\text{C}$		2.0		V
Output Resistance	R_o	$f = 1\text{KHz}$		17		m
Short Circuit Current	I_{SC}	$V_I = 35\text{V}$, $T_A = 25^\circ\text{C}$		250		mA
Peak Current	I_{PK}	$T_J = 25^\circ\text{C}$		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS KA7810A(Refer to the test circuits, $T_J = 0$ to 125°C , $I_O = 1\text{A}$, $V_I = 16\text{V}$, $C_I = 0.33\mu\text{F}$, $C_O = 0.1\mu\text{F}$ unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_O	$T_J = 25^\circ\text{C}$	9.8	10	10.2	V
		$I_O = 5\text{mA}$ to 1.0A , $P_D \leq 15\text{W}$ $V_I = 12.8\text{V}$ to 25V	9.6	10	10.4	
Line Regulation	ΔV_O	$V_I = 12.8\text{V}$ to 26V $I_O = 500\text{mA}$		8	100	mV
		$V_I = 13\text{V}$ to 20V		4	50	
		$T_J = 25^\circ\text{C}$ $V_I = 12.5\text{V}$ to 25V		8	100	
		$V_I = 13\text{V}$ to 20V		3	50	
Load Regulation	ΔV_O	$T_J = 25^\circ\text{C}$ $I_O = 5\text{mA}$ to 1.5A		12	100	mV
		$I_O = 5\text{mA}$ to 1.0A		12	100	
		$I_O = 250\text{mA}$ to 750mA		5	50	
Quiescent Current	I_Q	$T_J = 25^\circ\text{C}$		5.0	6.0	mA
Quiescent Current Change	ΔI_Q	$I_O = 5\text{mA}$ to 1.0A			0.5	mA
		$V_I = 13\text{V}$ to 26V , $I_O = 500\text{mA}$			0.8	
		$V_I = 12.8\text{V}$ to 25V , $T_J = 25^\circ\text{C}$			0.8	
Output Voltage Drift	$\Delta V_O / \Delta T$	$I_O = 5\text{mA}$		-1.0		mV/ $^\circ\text{C}$
Output Noise Voltage	V_N	$f = 10\text{Hz}$ to 100KHz , $T_A = 25^\circ\text{C}$		10		$\mu\text{V}/V_O$
Ripple Rejection	RR	$f = 120\text{Hz}$, $V_I = 14\text{V}$ to 24V $I_O = 500\text{mA}$		62		dB
Dropout Voltage	V_D	$I_O = 1.0\text{A}$, $T_J = 25^\circ\text{C}$		2.0		V
Output Resistance	R_O	$f = 1\text{KHz}$		17		m
Short Circuit Current	I_{SC}	$V_I = 35\text{V}$, $T_A = 25^\circ\text{C}$		250		mA
Peak Current	I_{PK}	$T_J = 25^\circ\text{C}$		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS KA7811A(Refer to the test circuits, $T_J = 0$ to 125°C , $I_O = 1\text{A}$, $V_I = 18\text{V}$, $C_I = 0.33\mu\text{F}$, $C_O = 0.1\mu\text{F}$ unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_O	$T_J = 25^\circ\text{C}$	10.8	11.0	11.2	V
		$I_O = 5\text{mA}$ to 1.0A , $P_O \leq 15\text{W}$ $V_I = 13.8\text{V}$ to 26V	10.6	11.0	11.4	
Line Regulation	ΔV_O	$V_I = 13.8\text{V}$ to 27V $I_O = 500\text{mA}$		10	110	mV
		$V_I = 15\text{V}$ to 21V		4	55	
		$T_J = 25^\circ\text{C}$		10	110	
				3	55	
Load Regulation	ΔV_O	$T_J = 25^\circ\text{C}$ $I_O = 5\text{mA}$ to 1.5A		12	100	mV
		$I_O = 5\text{mA}$ to 1.0A		12	100	
		$I_O = 250\text{mA}$ to 750mA		5	50	
Quiescent Current	I_Q	$T_J = 25^\circ\text{C}$		5.1	6.0	mA
					6.0	
Quiescent Current Change	ΔI_Q	$V_I = 13.8\text{V}$ to 26V , $T_J = 25^\circ\text{C}$			0.8	mA
		$V_I = 14\text{V}$ to 27V , $I_O = 500\text{mA}$			0.8	
		$I_O = 5\text{mA}$ to 1.0A			0.5	
Output Voltage Drift	$\Delta V_O / \Delta T$	$I_O = 5\text{mA}$		-1.0		mV/ $^\circ\text{C}$
Output Noise Voltage	V_N	$f = 10\text{Hz}$ to 100KHz , $T_A = 25^\circ\text{C}$		10		$\mu\text{V}/V_O$
Ripple Rejection	RR	$f = 120\text{Hz}$, $V_I = 14\text{V}$ to 24V $I_O = 500\text{mA}$		61		dB
Dropout Voltage	V_D	$I_O = 1.0\text{A}$, $T_J = 25^\circ\text{C}$		2.0		V
Output Resistance	R_O	$f = 1\text{KHz}$		18		m
Short Circuit Current	I_{SC}	$V_I = 35\text{V}$, $T_A = 25^\circ\text{C}$		250		mA
Peak Current	I_{PK}	$T_J = 25^\circ\text{C}$		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS KA7812A(Refer to the test circuits, $T_J = 0$ to 150°C , $I_O = 1\text{A}$, $V_I = 19\text{V}$, $C_I = 0.33\mu\text{F}$, $C_O = 0.1\mu\text{F}$ unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_O	$T_J = 25^\circ\text{C}$	11.75	12	12.25	V
		$I_O = 5\text{mA}$ to 1A , $P_D \leq 15\text{W}$ $V_I = 14.8$ to 27V	11.5	12	12.5	
*Line Regulation	ΔV_O	$V_I = 14.8$ to 30V , $I_O = 500\text{mA}$		10	120	mV
		$V_I = 16$ to 22V		4	120	
		$T_J = 25^\circ\text{C}$	$V_I = 14.5$ to 27V	10	120	
			$V_I = 16$ to 22V	3	60	
*Load Regulation	ΔV_O	$T_J = 25^\circ\text{C}$ $I_O = 5\text{mA}$ to 1.5A		12	100	mV
		$I_O = 5\text{mA}$ to 1A		12	100	
		$I_O = 250$ to 750mA		5	50	
Quiescent Current	I_Q	$T_J = 25^\circ\text{C}$		5.1	6	mA
Quiescent Current Change	ΔI_Q	$I_O = 5\text{mA}$ to 1A			0.5	mA
		$V_I = 15$ to 30V , $I_O = 500\text{mA}$			0.8	
		$V_I = 14.8$ to 27V , $T_J = 25^\circ\text{C}$			0.8	
Output Voltage Drift	$\frac{\Delta V_O}{\Delta T}$	$I_O = 5\text{mA}$		- 1		mV/ $^\circ\text{C}$
Output Noise Voltage	V_N	$f = 10\text{Hz}$ to 100KHz $T_A = 25^\circ\text{C}$		10		$\frac{\mu\text{V}}{V_O}$
Ripple Rejection	RR	$f = 120\text{Hz}$, $I_O = 500\text{mA}$ $V_I = 15$ to 25V		60		dB
Dropout Voltage	V_D	$I_O = 1\text{A}$, $T_J = 25^\circ\text{C}$		2		V
Output Resistance	R_O	$f = 1\text{KHz}$		18		$\text{m}\Omega$
Short Circuit Current	I_{SC}	$V_I = 35\text{V}$, $T_A = 25^\circ\text{C}$		250		mA
Peak Current	I_{PK}	$T_J = 25^\circ\text{C}$		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS KA7815A(Refer to the test circuits, $T_J = 0$ to 150°C , $I_O = 1\text{A}$, $V_I = 23\text{V}$, $C_I = 0.33\mu\text{F}$, $C_O = 0.1\mu\text{F}$ unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_O	$T_J = 25^\circ\text{C}$	14.7	15	15.3	V
		$I_O = 5\text{mA}$ to 1A , $P_D \leq 15\text{W}$ $V_I = 17.7$ to 30V	14.4	15	15.6	
*Line Regulation	ΔV_O	$V_I = 17.9$ to 30V , $I_O = 500\text{mA}$		10	150	mV
		$V_I = 20$ to 26V		5	150	
		$T_J = 25^\circ\text{C}$ $V_I = 17.5$ to 30V		11	150	
		$V_I = 20$ to 26V		3	75	
*Load Regulation	ΔV_O	$T_J = 25^\circ\text{C}$ $I_O = 5\text{mA}$ to 1.5A		12	100	mV
		$I_O = 5\text{mA}$ to 1A		12	100	
		$I_O = 250$ to 750mA		5	50	
Quiescent Current	I_Q	$T_J = 25^\circ\text{C}$		5.2	6	mA
Quiescent Current Change	ΔI_Q	$I_O = 5\text{mA}$ to 1A			0.5	mA
		$V_I = 17.5$ to 30V , $I_O = 500\text{mA}$			0.8	
		$V_I = 17.5$ to 30V , $T_J = 25^\circ\text{C}$			0.8	
Output Voltage Drift	$\frac{\Delta V_O}{\Delta T}$	$I_O = 5\text{mA}$		-1		mV/ $^\circ\text{C}$
Output Noise Voltage	V_N	$f = 10\text{Hz}$ to 100KHz $T_A = 25^\circ\text{C}$		10		$\frac{\mu\text{V}}{V_O}$
Ripple Rejection	RR	$f = 120\text{Hz}$, $I_O = 500\text{mA}$ $V_I = 18.5$ to 28.5V		58		dB
Dropout Voltage	V_D	$I_O = 1\text{A}$, $T_J = 25^\circ\text{C}$		2		V
Output Resistance	R_O	$f = 1\text{KHz}$		19		$\text{m}\Omega$
Short Circuit Current	I_{SC}	$V_I = 35\text{V}$, $T_A = 25^\circ\text{C}$		250		mA
Peak Current	I_{PK}	$T_J = 25^\circ\text{C}$		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS KA7818A(Refer to the test circuits, $T_J = 0$ to 150°C , $I_O = 1\text{A}$, $V_I = 27\text{V}$, $C_1 = 0.33\mu\text{F}$, $C_O = 0.1\mu\text{F}$ unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_O	$T_J = 25^\circ\text{C}$	17.64	18	18.36	V
		$I_O = 5\text{mA}$ to 1A , $P_D \leq 15\text{W}$ $V_I = 21$ to 33V	17.3	18	18.7	
*Line Regulation	ΔV_O	$V_I = 21$ to 33V , $I_O = 500\text{mA}$		15	180	mV
		$V_I = 21$ to 33V ,		5	180	
		$T_J = 25^\circ\text{C}$ $V_I = 20.6$ to 33V		15	180	
		$V_I = 24$ to 30V		5	90	
*Load Regulation	ΔV_O	$T_J = 25^\circ\text{C}$ $I_O = 5\text{mA}$ to 1.5A		15	100	mV
		$I_O = 5\text{mA}$ to 1A		15	100	
		$I_O = 250$ to 750mA		7	50	
Quiescent Current	I_Q	$T_J = 25^\circ\text{C}$		5.2	6	mA
Quiescent Current Change	ΔI_Q	$I_O = 5\text{mA}$ to 1A			0.5	mA
		$V_I = 21$ to 33V , $I_O = 500\text{mA}$			0.8	
		$V_I = 21$ to 33V , $T_J = 25^\circ\text{C}$			0.8	
Output Voltage Drift	$\frac{\Delta V_O}{\Delta T}$	$I_O = 5\text{mA}$		-1		mV/ $^\circ\text{C}$
Output Noise Voltage	V_N	$f = 10\text{Hz}$ to 100KHz $T_A = 25^\circ\text{C}$		10		$\frac{\mu\text{V}}{V_O}$
Ripple Rejection	RR	$f = 120\text{Hz}$, $I_O = 500\text{mA}$ $V_I = 22$ to 32V		57		dB
Dropout Voltage	V_D	$I_O = 1\text{A}$, $T_J = 25^\circ\text{C}$		2		V
Output Resistance	R_O	$f = 1\text{KHz}$		19		$\text{m}\Omega$
Short Circuit Current	I_{sc}	$V_I = 35\text{V}$, $T_A = 25^\circ\text{C}$		250		mA
Peak Current	I_{PK}	$T_J = 25^\circ\text{C}$		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS KA7824A(Refer to the test circuits, $T_J = 0$ to 150°C , $I_o = 1\text{A}$, $V_i = 33\text{V}$, $C_i = 0.33\mu\text{F}$, $C_o = 0.1\mu\text{F}$ unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	$T_J = 25^\circ\text{C}$	23.5	24	24.5	V
		$I_o = 5\text{mA}$ to 1A , $P_o \leq 15\text{W}$ $V_i = 27.3$ to 38V	23	24	25	
*Line Regulation	ΔV_o	$V_i = 27$ to 38V , $I_o = 500\text{mA}$		18	240	mV
		$V_i = 30$ to 36V		6	240	
		$T_J = 25^\circ\text{C}$ $V_i = 26.7$ to 38V		18	240	
		$V_i = 30$ to 36V		6	120	
*Load Regulation	ΔV_o	$T_J = 25^\circ\text{C}$ $I_o = 5\text{mA}$ to 1.5A		15	100	mV
		$I_o = 5\text{mA}$ to 1A		15	100	
		$I_o = 250$ to 750mA		7	50	
Quiescent Current	I_Q	$T_J = 25^\circ\text{C}$		5.2	6	mA
Quiescent Current Change	ΔI_Q	$I_o = 5\text{mA}$ to 1A			0.5	mA
		$V_i = 27.3$ to 38V , $I_o = 500\text{mA}$			0.8	
		$V_i = 27.3$ to 38V , $T_J = 25^\circ\text{C}$			0.8	
Output Voltage Drift	$\frac{\Delta V_o}{\Delta T}$	$I_o = 1\text{mA}$		-1.5		mV/ $^\circ\text{C}$
Output Noise Voltage	V_N	$f = 10\text{Hz}$ to 100KHz $T_A = 25^\circ\text{C}$		10		$\frac{\mu\text{V}}{V_o}$
Ripple Rejection	RR	$f = 120\text{Hz}$, $I_o = 500\text{mA}$ $V_i = 28$ to 38V		54		dB
Dropout Voltage	V_D	$I_o = 1\text{A}$, $T_J = 25^\circ\text{C}$		2		V
Output Resistance	R_o	$f = 1\text{KHz}$		20		m Ω
Short Circuit Current	I_{sc}	$V_i = 35\text{V}$, $T_A = 25^\circ\text{C}$		250		mA
Peak Current	I_{PK}	$T_J = 25^\circ\text{C}$		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

TEST CIRCUITS

Fig. 1 DC Parameters

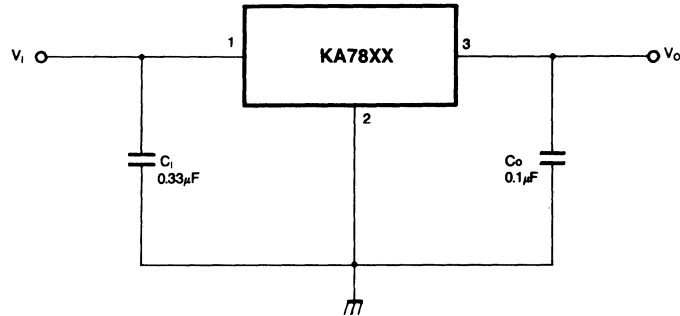


Fig. 2 Load Regulation

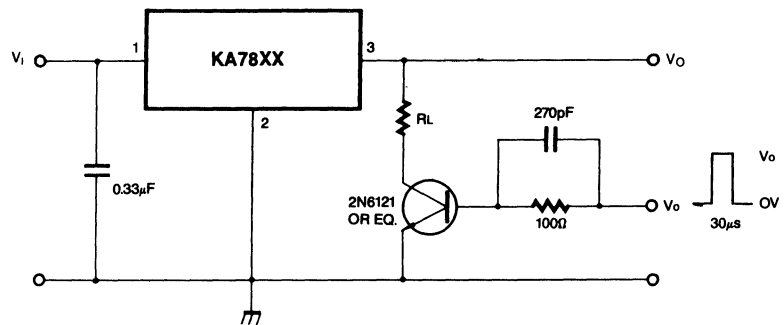
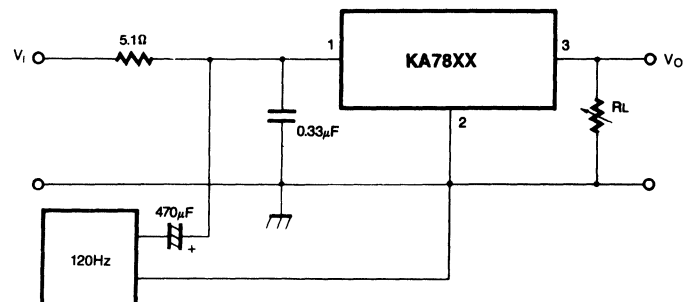


Fig. 3 Ripple Rejection



APPLICATION CIRCUITS

Fig. 4 Fixed Output Regulator

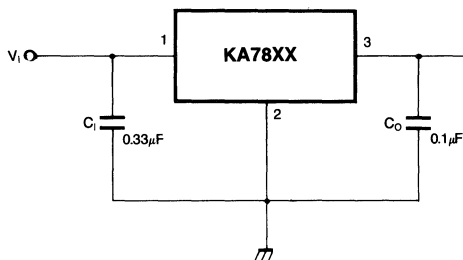
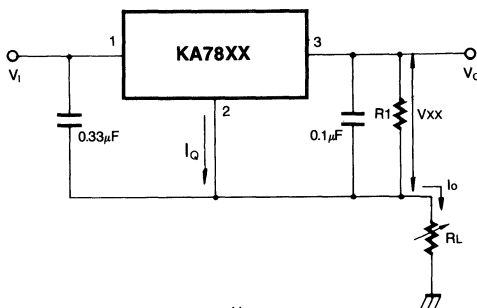


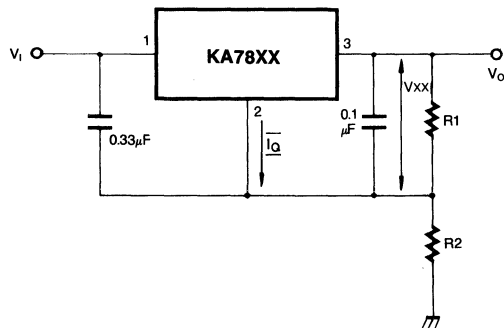
Fig. 5 Constant Current Regulator

**Notes:**

- (1) To specify an output voltage, substitute voltage value for "XX."
A common ground is required between the input and the output voltage. The input voltage must remain typically 2.0V above the output voltage even during the low point on the input ripple voltage.
- (2) C_I is required if regulator is located an appreciable distance from power supply filter.
- (3) C_O improves stability and transient response.

$$I_O = \frac{V_{XX}}{R_1} + I_Q$$

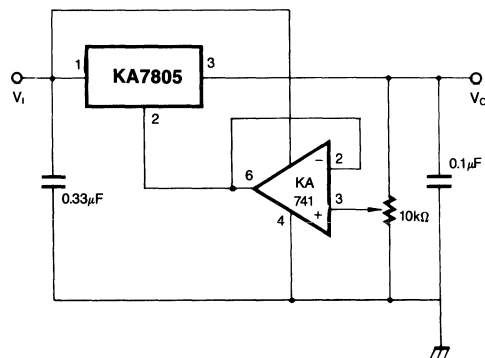
Fig. 6 Circuit for Increasing Output Voltage



$$I_{R1} \geq 5 I_Q$$

$$V_O = V_{XX} (1 + R_2/R_1) + I_Q R_2$$

Fig. 7 Adjustable Output Regulator (7 to 30V)



APPLICATION CIRCUIT

Fig. 8 High Current Voltage Regulator

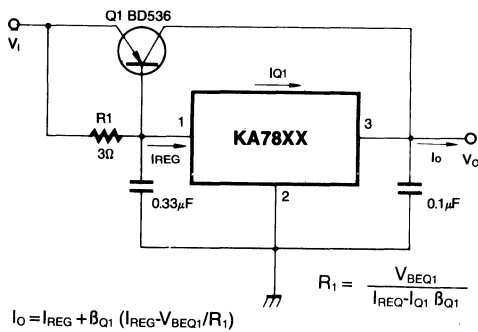


Fig. 9 High Output Current with Short Circuit Protection

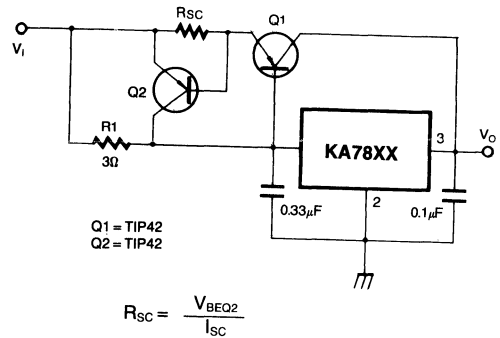


Fig. 10 Tracking Voltage Regulator

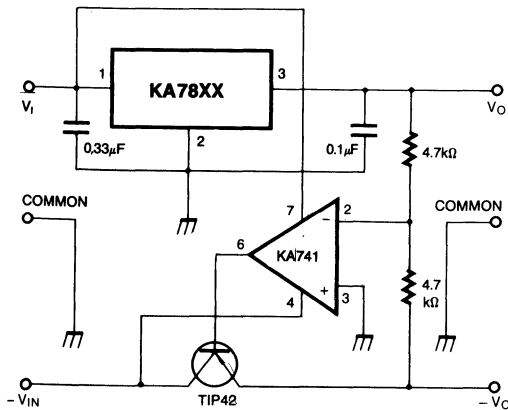


Fig. 11 Split Power Supply ($\pm 15V-1A$)

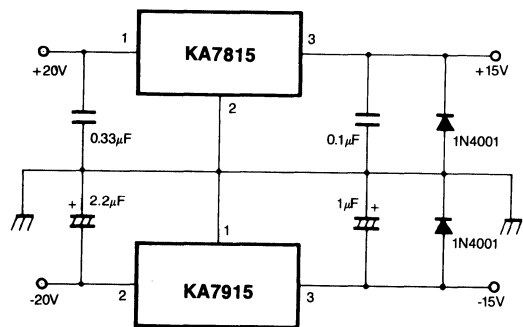


Fig. 12 Negative Output Voltage Circuit

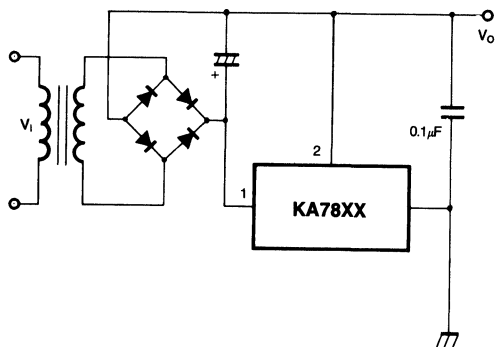
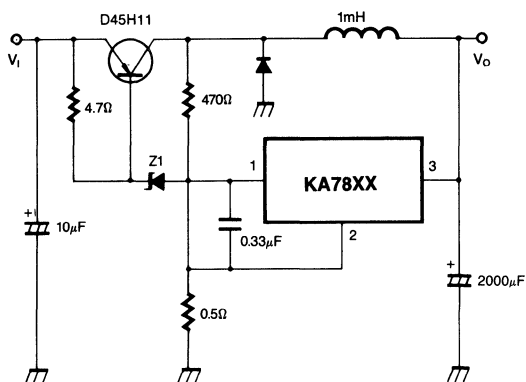


Fig. 13 Switching Regulator



TYPICAL PERFORMANCE CHARACTERISTICS

FIG. 14 QUIESCENT CURRENT

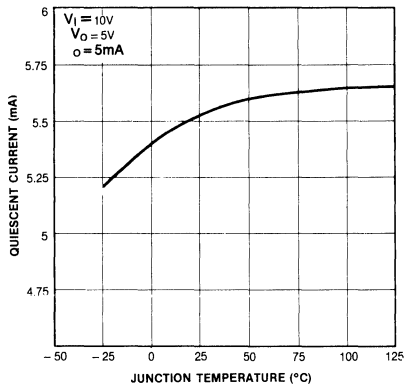


FIG. 15 PEAK OUTPUT CURRENT

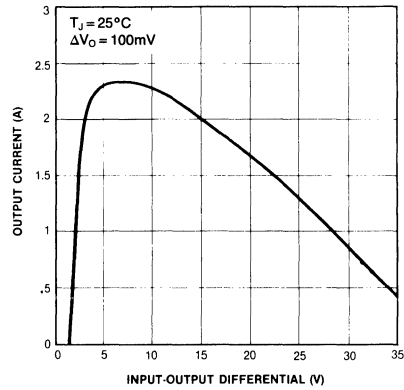


FIG. 16 OUTPUT VOLTAGE

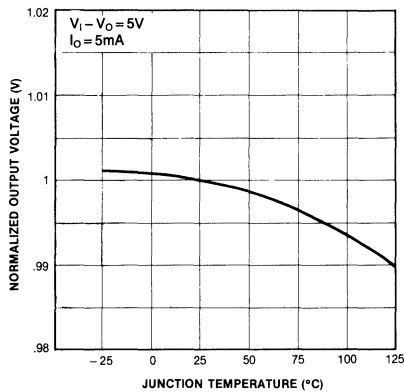
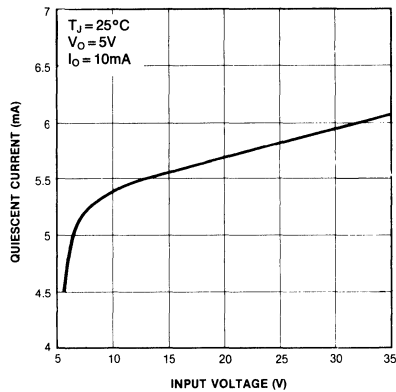


FIG. 17 QUIESCENT CURRENT



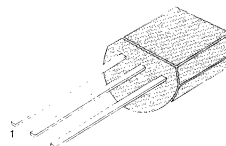
3-TERMINAL 0.1A POSITIVE VOLTAGE REGULATORS

The KA78LXX series of fixed voltage monolithic integrated circuit voltage regulators are suitable for applications that required supply up to 100mA.

FEATURES

- Maximum Output Current of 100mA
- Output Voltage of 5V, 6V, 8V, 9V, 10V, 12V, 15V, 18V and 24V.
- Thermal Overload Protection
- Short Circuit Current Limiting

TO-92

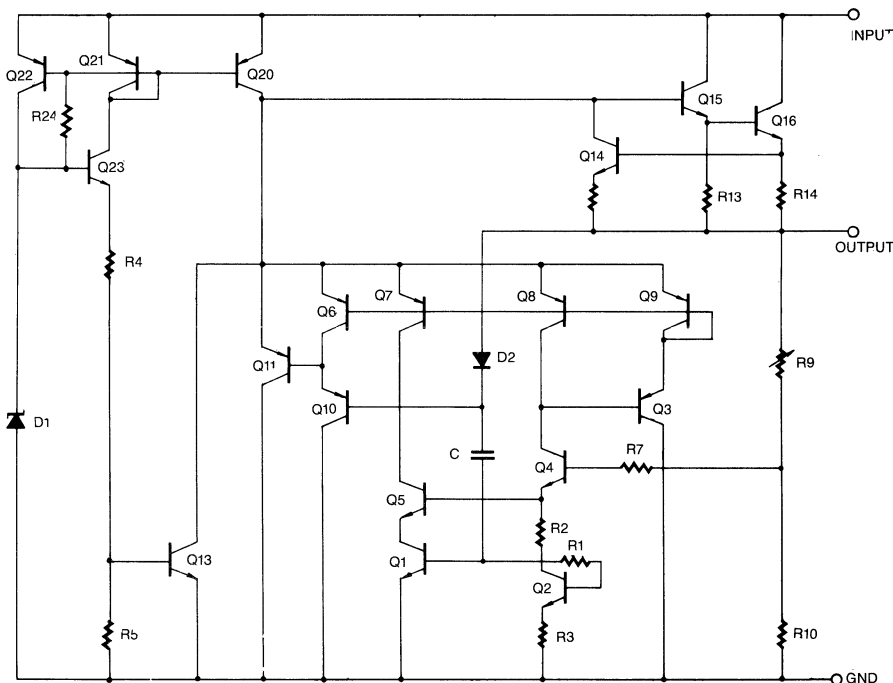


1: Output 2: GND 3: Input

ORDERING INFORMATION

Device	Package	Operating Temperature
KA78LXXAZ	TO-92	0 ~ +125°C

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise specified)

Characteristic	Symbol	Value	Unit
Input Voltage (for $V_O = 5\text{V}$, 8V) (for $V_O = 12\text{V}$, 15V)	V_I	30 35	V V
Operating Junction Temperature Range	T_{OPR}	$0 \sim +125$	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	$-65 \sim +150$	$^\circ\text{C}$

KA78L05A ELECTRICAL CHARACTERISTICS

($V_I = 10\text{V}$, $I_O = 40\text{mA}$, $0^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$, $C_I = 0.33\mu\text{F}$, $C_O = 0.1\mu\text{F}$, unless otherwise specified. (Note 1))

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V _O	T _J = 25°C		4.8	5.0	5.2	V
Line Regulation		ΔV _O	T _J = 25°C	7V ≤ V _I ≤ 20V		8	150	mV
				8V ≤ V _I ≤ 20V		6	100	mV
Load Regulation		ΔV _O	T _J = 25°C	1mA ≤ I _O ≤ 100mA		11	60	mV
				1mA ≤ I _O ≤ 40mA		5.0	30	mV
Output Voltage		V _O	7V ≤ V _I ≤ 20V	1mA ≤ I _O ≤ 40mA	4.75		5.25	V
			7V ≤ V _I ≤ V _{MAX} (Note 2)	1mA ≤ I _O ≤ 70mA	4.75		5.25	V
Quiescent Current		I _Q	T _J = 25°C			2.0	5.5	mA
Quiescent Current Change	with line	ΔI _Q	8V ≤ V _I ≤ 20V				1.5	mA
	with load	ΔI _O	1mA ≤ I _O ≤ 40mA				0.1	mA
Output Noise Voltage		V _N	T _A = 25°C, 10Hz ≤ f ≤ 100KHz			40		μV
Temperature Coefficient of V _O		$\frac{\Delta V_O}{\Delta T}$	I _O = 5mA			− 0.65		mV/°C
Ripple Rejection		RR	f = 120Hz, 8V ≤ V _I ≤ 18V, T _J = 25°C		41	80		dB
Dropout Voltage		V _D	T _J = 25°C			1.7		V

KA78L06A ELECTRICAL CHARACTERISTICS(V_I = 12V, I_O = 40mA, 0°C < T_J < 125°C, C_I = 0.33μF, C_O = 0.1μF, unless otherwise specified. (Note 1))

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V _O	T _J = 25°C		5.75	6.0	6.25	V
Line Regulation		ΔV _O	T _J = 25°C	8.5V < V _I < 20V		64	175	mV
				9V ≥ V _I ≥ 20V		54	125	
Load Regulation		ΔV _O	T _J = 25°C	1mA < I _O < 100mA		12.8	80	mV
				1mA < I _O < 70mA		5.8	40	
Output Voltage		V _O	8.5V < V _I < 20V, 1mA < I _O < 40mA		5.7		6.3	V
			8.5V < V _I < V _{MAX} (Note 2), 1mA < I _O < 70mA		5.7		6.3	
Quiescent Current		I _O	T _J = 25°C			3.9	6.0	mA
			T _J = 125°C				5.5	
Quiescent Current Change	With Line	ΔI _O	9V < V _I < 20V				1.5	mA
	With Load		1mA < I _O < 40mA				0.1	
Output Noise Voltage		V _N	T _A = 25°C, 10Hz < f < 100KHz			49		μV
Temperature Coefficient of V _O		$\frac{\Delta V_O}{\Delta T}$	I _O = 5mA			0.75		mV/°C
Ripple Rejection		RR	f = 120Hz, T _J = 25°C 10V < V _I < 20V		40	46		dB
Drop Voltage		V _D	T _J = 25°C			1.7		V

KA78L08A ELECTRICAL CHARACTERISTICS(V_I = 14V, I_O = 40mA, 0°C ≤ T_J ≤ 125°C, C_I = 0.33μF, C_O = 0.1μF, unless otherwise specified. (Note 1))

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V _O	T _J = 25°C		7.7	8.0	8.3	V
Line Regulation		ΔV _O	T _J = 25°C	10.5 ≤ V _I ≤ 23V		10	175	mV
				11V ≤ V _I ≤ 23V		8	125	mV
Load Regulation		ΔV _O	T _J = 25°C	1mA ≤ I _O ≤ 100mA		15	80	mV
				1mA ≤ I _O ≤ 40mA		8.0	40	mV
Output Voltage		V _O	10.5V ≤ V _I ≤ 23V, 1mA ≤ I _O ≤ 40mA		7.6		8.4	V
			10.5V ≤ V _I ≤ V _{MAX} (Note 2), 1mA ≤ I _O ≤ 70mA		7.6		8.4	V
Quiescent Current		I _O	T _J = 25°C			2.0	5.5	mA
Quiescent Current Change	with line	ΔI _O	11V ≤ V _I ≤ 23V				1.5	mA
	with load	ΔI _O	1mA ≤ I _O ≤ 40mA				0.1	mA
Output Noise Voltage		V _N	T _A = 25°C, 10Hz ≤ f ≤ 100KHz			60		μV
Temperature Coefficient of V _O		$\frac{\Delta V_O}{\Delta T}$	I _O = 5mA			-0.8		mV/°C
Ripple Rejection		RR	f = 120Hz, 11V ≤ V _I ≤ 21V, T _J = 25°C		39	70		dB
Dropout Voltage		V _D	T _J = 25°C			1.7		V

KA78L09A ELECTRICAL CHARACTERISTICS

(V_i = 15V, I_o = 40mA, 0°C ≤ T_J ≤ 125°C, C_i = 0.33μF, C_o = 0.1μF, unless otherwise specified. (Note 1))

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V _o	T _J = 25°C	8.64	9.0	9.36	V
Line Regulation	ΔV _o	T _J = 25°C	11.5V ≤ V _i ≤ 24V	90	200	mV
			13V ≤ V _i ≤ 24V	100	150	mV
Load Regulation	ΔV _o	T _J = 25°C	1mA ≤ I _o ≤ 100mA	20	90	mV
			1mA ≤ I _o ≤ 40mA	10	45	mV
Output Voltage	V _o	11.5V ≤ V _i ≤ 24V	1mA ≤ I _o ≤ 40mA	8.55	9.45	V
		11.5V ≤ V _i ≤ V _{MAX} (Note 2)	1mA ≤ I _o ≤ 70mA	8.55	9.45	V
Quiescent Current	I _o	T _J = 25°C		2.1	6.0	mA
Quiescent Current Change	with line	ΔI _o	13V ≤ V _i ≤ 24V		1.5	mA
	with load	ΔI _o	1mA ≤ I _o ≤ 40mA		0.1	mA
Output Noise Voltage	V _N	T _A = 25°C, 10Hz ≤ f ≤ 100KHz		70		μV
Temperature Coefficient of V _o	$\frac{\Delta V_o}{\Delta T}$	I _o = 5mA		-0.9		mV/°C
Ripple Rejection	RR	f = 120Hz, 12V ≤ V _i ≤ 22V, T _J = 25°C	38	44		dB
Dropout Voltage	V _D	T _J = 25°C		1.7		V

KA78L10A ELECTRICAL CHARACTERISTICS

(V_i = 16V, I_o = 40mA, 0°C < T_J < 125°C, C_i = 0.33μF, C_o = 0.1μF, unless otherwise specified. (Note 1))

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V _o	T _J = 25°C	9.6	10.0	10.4	V
Line Regulation	ΔV _o	T _J = 25°C	12.5V < V _i < 25V	100	220	mV
			14V ≥ V _i ≥ 25V	100	170	mV
Load Regulation	ΔV _o	T _J = 25°C	1mA < I _o < 100mA	20	94	mV
			1mA < I _o < 70mA	10	47	mV
Output Voltage	V _o	12.5V < V _i < 25V, 1mA < I _o < 40mA	9.5		10.5	V
		12.5V < V _i < V _{MAX} (Note 2), 1mA < I _o < 70mA	9.5		10.5	V
Quiescent Current	I _o	T _J = 25°C		4.2	6.5	mA
		T _J = 125°C			6.0	mA
Quiescent Current Change	With Line	ΔI _o	12.5V < V _i < 25V		1.5	mA
	With Load		1mA < I _o < 40mA		0.1	mA
Output Noise Voltage	V _N	T _A = 25°C, 10Hz < f < 100KHz		74		μV
Temperature Coefficient of V _o	$\frac{\Delta V_o}{\Delta T}$	I _o = 5mA		0.95		mV/°C
Ripple Rejection	RR	f = 120Hz, T _J = 25°C 15V < V _i < 25V	38	43		dB
Drop Voltage	V _D	T _J = 25°C		1.7		V

KA78L12A ELECTRICAL CHARACTERISTICS

(V_I = 19V, I_O = 40mA, 0°C ≤ T_J ≤ 125°C, C_I = 0.33μF, C_O = 0.1μF, unless otherwise specified. (Note 1))

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V _O	T _J = 25°C	11.5	12	12.5	V
Line Regulation	ΔV _O	T _J = 25°C	14.5V ≤ V _I ≤ 27V	20	250	mV
			16V ≤ V _I ≤ 27V	15	200	mV
Load Regulation	ΔV _O	T _J = 25°C	1mA ≤ I _O ≤ 100mA	20	100	mV
			1mA ≤ I _O ≤ 40mA	10	50	mV
Output Voltage	V _O	14.5V ≤ V _I ≤ 27V	1mA ≤ I _O ≤ 40mA	11.4	12.6	V
		14.5V ≤ V _I ≤ V _{MAX} (Note 2)	1mA ≤ I _O ≤ 70mA	11.4	12.6	V
Quiescent Current	I _O	T _J = 25°C		2.1	6.0	mA
Quiescent Current Change	with line	ΔI _O	16V ≤ V _I ≤ 27V		1.5	mA
	with load	ΔI _O	1mA ≤ I _O ≤ 40mA		0.1	mA
Output Noise Voltage	V _N	T _A = 25°C, 10Hz ≤ f ≤ 100KHz		80		μV
Temperature Coefficient of V _O	$\frac{\Delta V_O}{\Delta T}$	I _O = 5mA		-1.0		mV/°C
Ripple Rejection	RR	f = 120Hz, 15V ≤ V _I ≤ 25V, T _J = 25°C	37	65		dB
Dropout Voltage	V _D	T _J = 25°C		1.7		V

KA78L15A ELECTRICAL CHARACTERISTICS

(V_I = 23V, I_O = 40mA, 0°C ≤ T_J ≤ 125°C, C_I = 0.33μF, C_O = 0.1μF, unless otherwise specified. (Note 1))

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V _O	T _J = 25°C	14.4	15	15.6	V
Line Regulation	ΔV _O	T _J = 25°C	17.5V ≤ V _I ≤ 30V	25	300	mV
			20V ≤ V _I ≤ 30V	20	250	nV
Load Regulation	ΔV _O	T _J = 25°C	1mA ≤ I _O ≤ 100mA	25	150	mV
			1mA ≤ I _O ≤ 40mA	12	75	mV
Output Voltage	V _O	17.5V ≤ V _I ≤ 30V	1mA ≤ I _O ≤ 40mA	14.25	15.75	V
		17.5V ≤ V _I ≤ V _{MAX} (Note 2)	1mA ≤ I _O ≤ 70mA	14.25	15.75	V
Quiescent Current	I _O	T _J = 25°C		2.2	6.0	mA
Quiescent Current Change	with line	ΔI _O	20V ≤ V _I ≤ 30V		1.5	mA
	with load	ΔI _O	1mA ≤ I _O ≤ 40mA		0.1	mA
Output Noise Voltage	V _N	T _A = 25°C, 10Hz ≤ f ≤ 100KHz		90		μV
Temperature Coefficient of V _O	$\frac{\Delta V_O}{\Delta T}$	I _O = 5mA		-1.3		mV/°C
Ripple Rejection	RR	f = 120Hz, 18.5V ≤ V _I ≤ 28.5V, T _J = 25°C	34	60		dB
Dropout Voltage	V _D	T _J = 25°C		1.7		V

KA78L18A ELECTRICAL CHARACTERISTICS

(V_i = 27V, I_o = 40mA, 0°C ≤ T_J ≤ 125°C, C_i = 0.33μF, C_o = 0.1μF, unless otherwise specified. (Note 1))

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V _o	T _J = 25°C	17.3	18	18.7	V
Line Regulation	ΔV _o	T _J = 25°C	21V ≤ V _i ≤ 33V	145	300	mV
			22V ≤ V _i ≤ 33V	135	250	mV
Load Regulation	ΔV _o	T _J = 25°C	1mA ≤ I _o ≤ 100mA	30	170	mV
			1mA ≤ I _o ≤ 40mA	15	85	mV
Output Voltage	V _o	21V ≤ V _i ≤ 33V	1mA ≤ I _o ≤ 40mA	17.1	18.9	V
		21V ≤ V _i ≤ V _{MAX} (Note 2)	1mA ≤ I _o ≤ 70mA	17.1	18.9	V
Quiescent Current	I _q	T _J = 25°C		2.2	6.0	mA
Quiescent Current Change	with line	ΔI _q	21V ≤ V _i ≤ 33V		1.5	mA
	with load	ΔI _q	1mA ≤ I _o ≤ 40mA		0.1	mA
Output Noise Voltage	V _N	T _A = 25°C, 10Hz ≤ f ≤ 100KHz		150		μV
Temperature Coefficient of V _o	$\frac{\Delta V_o}{\Delta T}$	I _o = 5mA		-1.8		mV/°C
Ripple Rejection	RR	f = 120Hz, 23V ≤ V _i ≤ 33V, T _J = 25°C	34	48		dB
Dropout Voltage	V _D	T _J = 25°C		1.7		V

KA78L24A ELECTRICAL CHARACTERISTICS

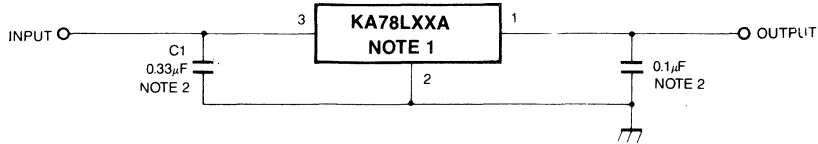
(V_i = 33V, I_o = 40mA, 0°C ≤ T_J ≤ 125°C, C_i = 0.33μF, C_o = 0.1μF, unless otherwise specified. (Note 1))

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V _o	T _J = 25°C	23	24	25	V
Line Regulation	ΔV _o	T _J = 25°C	27V ≤ V _i ≤ 38V	160	300	mV
			28V ≤ V _i ≤ 38V	150	250	mV
Load Regulation	ΔV _o	T _J = 25°C	1mA ≤ I _o ≤ 100mA	40	200	mV
			1mA ≤ I _o ≤ 40mA	20	100	mV
Output Voltage	V _o	27V ≤ V _i ≤ 38V	1mA ≤ I _o ≤ 40mA	22.8	25.2	V
		27V ≤ V _i ≤ V _{MAX} (Note 2)	1mA ≤ I _o ≤ 70mA	22.8	25.2	V
Quiescent Current	I _q	T _J = 25°C		2.2	6.0	mA
Quiescent Current Change	with line	ΔI _q	28V ≤ V _i ≤ 38V		1.5	mA
	with load	ΔI _q	1mA ≤ I _o ≤ 40mA		0.1	mA
Output Noise Voltage	V _N	T _A = 25°C, 10Hz ≤ f ≤ 100KHz		200		μV
Temperature Coefficient of V _o	$\frac{\Delta V_o}{\Delta T}$	I _o = 5mA		-2.0		mV/°C
Ripple Rejection	RR	f = 120Hz, 28V ≤ V _i ≤ 38V, T _J = 25°C	34	45		dB
Dropout Voltage	V _D	T _J = 25°C		1.7		V

Notes

- The maximum steady state usable output current and input voltage are very dependent on the heat sinking and/or lead length of the package. The data above represent pulse test conditions with junction temperatures as indicated at the initiation of tests.
- Power dissipation ≤ 0.75W.

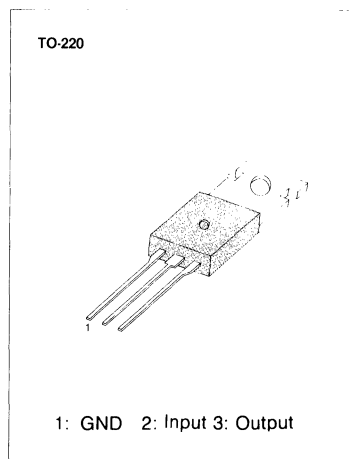
TYPICAL APPLICATION

**Notes**

1. To specify an output voltage, substitute voltage value for "xx".
2. Bypass Capacitors are recommended for optimum stability and transient response and should be located as close as possible to the regulator.

3-TERMINAL 1A NEGATIVE VOLTAGE REGULATORS

The KA79XX series of three-terminal negative regulators are available in TO-220 package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible.



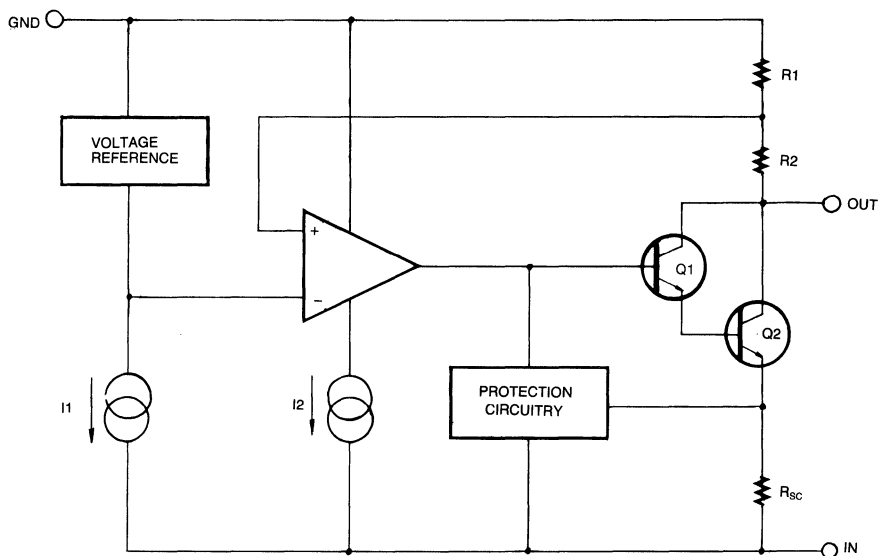
FEATURES

- Output Current in Excess of 1A
- Output Voltages of -5, -6, -8, -12, -15, -18, -24V
- Internal Thermal Overload Protection
- Short Circuit Protection
- Output Transistor Safe-Area Compensation

ORDERING INFORMATION

Device	Package	Operating Temperature
KA79XX	TO-220	0 ~ 125°C

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise specified)

Characteristic	Symbol	Value	Unit
Input Voltage	V_I	-35	V
Thermal Resistance Junction-Cases	$R_{\theta JC}$	5	$^\circ\text{C/W}$
Junction-Air	$R_{\theta JA}$	65	$^\circ\text{C/W}$
Operating Junction Temperature Range	T_{OPR}	0 ~ +125	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-65 ~ +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS KA7905

($V_I = 10\text{V}$, $I_O = 500\text{mA}$, $0^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$, $C_I = 2.2\mu\text{F}$, $C_O = 1\mu\text{F}$, unless otherwise specified.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_O	$T_J = 25^\circ\text{C}$	-4.8	-5	-5.2	V
		$I_O = 5\text{mA}$ to 1A , $P_O \leq 15\text{W}$ $V_I = -8$ to -20V	-4.75	-5	-5.25	
Line Regulation	ΔV_O	$T_J = 25^\circ\text{C}$		10	100	mV
		$V_I = -7$ to -25V $V_I = -8$ to -12V				
Load Regulation	ΔV_O	$T_J = 25^\circ\text{C}$ $I_O = 5\text{mA}$ to 1.5A		10	100	mV
		$T_J = 25^\circ\text{C}$ $I_O = 250$ to 750mA		3	50	
Quiescent Current	I_Q	$T_J = 25^\circ\text{C}$		3	6	mA
Quiescent Current Change	ΔI_Q	$I_O = 5\text{mA}$ to 1A		0.05	0.5	mA
		$V_I = -8$ to -25V		0.1	1.3	
Temperature Coefficient of V_O	$\frac{\Delta V_O}{\Delta T}$	$I_O = 5\text{mA}$		-0.4		mV/ $^\circ\text{C}$
Output Noise Voltage	V_N	$f = 10\text{Hz}$ to 100KHz $T_A = 25^\circ\text{C}$		100		μV
Ripple Rejection	RR	$f = 120\text{Hz}$, $I_O = 20\text{mA}$ $\Delta V_I = 10\text{V}$	54	60		dB
Dropout Voltage	V_D	$T_J = 25^\circ\text{C}$ $I_O = 1\text{A}$	2		V	
Short Circuit Current	I_{SC}	$T_J = 25^\circ\text{C}$, $V_I = -35\text{V}$		300		mA
Peak Current	I_{PK}	$T_J = 25^\circ\text{C}$		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

ELECTRICAL CHARACTERISTICS KA7906

(C₁ = 2.2μF, C₀ = 1μF, T_J = 0 to 125°C, I_o = 500mA, V_I = 11V, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V _o	T _J = 25°C		- 5.75	- 6	- 6.25	V
		I _o = 5mA to 1A, P _o ≤ 15W V _I = - 9 to - 21V		- 5.7	- 6	- 6.3	
Line Regulation	Δ V _o	T _J = 25°C	V _I = - 8 to - 25V		10	120	mV
			V _I = - 9 to - 13V		5	60	
Load Regulation	Δ V _o	T _J = 25°C I _o = 5mA to 1.5A			10	120	mV
		T _J = 25°C I _o = 250 to 750mA			3	60	
Quiescent Current	I _Q	T _J = 25°C			3	6	mA
Quiescent Current Change	Δ I _Q	I _o = 5mA to 1A				0.5	mA
		V _I = - 9 to - 25V				1.3	
Output Voltage Drift	$\frac{\Delta V_o}{\Delta T}$	I _o = 5mA			- 0.5		mV/°C
Output Noise Voltage	V _N	f = 10Hz to 100KHz T _A = 25°C			130		μV
Ripple Rejection	RR	f = 120Hz Δ V _I = 10V		54	60		dB
Dropout Voltage	V _D	T _J = 25°C, I _o = 1A			2		V
Short Circuit Current	I _{sc}	T _J = 25°C V _I = - 35V			300		mA
Peak Current	I _{PK}	T _J = 25°C			2.2		A

* Load and line regulation are specified at constant junction temperature. Change in V_o due to heating effects must be taken into account separately. Pulse testing with low duty is used.

ELECTRICAL CHARACTERISTICS KA7908(V_I = 14V, I_O = 500mA, 0°C ≤ T_J ≤ 125°C, C_I = 2.2μF, C_O = 1μF, unless otherwise specified.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V _O	T _J = 25°C	-7.7	-8	-8.3	V
		I _O = 5mA to 1A, P _O ≤ 15W V _I = - - 1.5 to -23V	-7.6	-8	-8.4	
Line Regulation	ΔV _O	T _J = 25°C	V _I = -10.5 to -25V	10	100	mV
			V _I = -11 to -17V	5	80	
Load Regulation	ΔV _O	T _J = 25°C I _O = 5mA to 1.5A		12	160	mV
		T _J = 25°C I _O = 250 to 750mA		4	80	
Quiescent Current	I _Q	T _J = 25°C		3	6	mA
Quiescent Current Change	ΔI _Q	I _O = 5mA to 1A		0.05	0.5	mA
		V _I = -11.5 to -25V		0.1	1	
Temperature Coefficient of V _O	$\frac{\Delta V_O}{\Delta T}$	I _O = 5mA		-0.6		mV/°C
Output Noise Voltage	V _N	f = 10Hz to 100KHz T _A = 25°C		175		μV
Ripple Rejection	RR	f = 120Hz, I _O = 20mA ΔV _I = 10V	54	60		dB
Dropout Voltage	V _D	T _J = 25°C I _O = 1A	2		V	
Short Circuit Current	I _{SC}	T _J = 25°C, V _I = -35V		300		mA
Peak Current	I _{PK}	T _J = 25°C		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

ELECTRICAL CHARACTERISTICS KA7912(V_I = 18V, I_O = 500mA, 0°C ≤ T_J ≤ 125°C, C_I = 2.2μF, C_O = 1μF, unless otherwise specified.)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V _O	T _J = 25°C		-11.5	-12	-12.5	V
		I _O = 5mA to 1A, P _O ≤ 15W V _I = -15.5 to -27V		-11.4	-12	-12.6	
Line Regulation	ΔV _O	T _J = 25°C	V _I = -14.5 to -30V		12	240	mV
			V _I = -16 to -22V		6	120	
Load Regulation	ΔV _O	T _J = 25°C I _O = 5mA to 1.5A			12	240	mV
		T _J = 25°C I _O = 250 to 750mA			4	120	
Quiescent Current	I _O	T _J = 25°C			3	6	mA
Quiescent Current Change	ΔI _O	I _O = 5mA to 1A			0.05	0.5	mA
		V _I = -15 to -30V			0.1	1	
Temperature Coefficient of V _O	$\frac{\Delta V_O}{\Delta T}$	I _O = 5mA			-0.8		mV/°C
Output Noise Voltage	V _N	f = 10Hz to 100KHz T _A = 25°C			200		μV
Ripple Rejection	RR	f = 120Hz, I _O = 20mA ΔV _I = 10V		54	60		dB
Dropout Voltage	V _D	T _J = 25°C I _O = 1A		2		V	
Short Circuit Current	I _{SC}	T _J = 25°C, V _I = -35V			300		mA
Peak Current	I _{PK}	T _J = 25°C			2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

ELECTRICAL CHARACTERISTICS KA7915(V_I = 23V, I_O = 500mA, 0°C ≤ T_J ≤ 125°C, C_I = 2.2μF, C_O = 1μF, unless otherwise specified.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V _O	T _J = 25°C	-14.4	-15	-15.6	V
		I _O = 5mA to 1A, P _O ≤ 15W V _I = -18 to -30V	-14.25	-15	-15.75	
Line Regulation	ΔV _O	T _J = 25°C	V _I = -17.5 to -30V	12	300	mV
			V _I = -20 to -26V	6	150	
Load Regulation	ΔV _O	T _J = 25°C I _O = 5mA to 1.5A		12	300	mV
		T _J = 25°C I _O = 250 to 750mA		4	150	
Quiescent Current	I _Q	T _J = 25°C		3	6	mA
Quiescent Current Change	ΔI _Q	I _O = 5mA to 1A		0.05	0.5	mA
		V _I = -18.5 to -30V		0.1	1	
Temperature Coefficient of V _O	$\frac{\Delta V_O}{\Delta T}$	I _O = 5mA		-0.9		mV/°C
Output Noise Voltage	V _N	f = 10Hz to 100KHz T _A = 25°C		250		μV
Ripple Rejection	RR	f = 120Hz, I _O = 20mA ΔV _I = 10V	54	60		dB
Dropout Voltage	V _D	T _J = 25°C I _O = 1A	2		V	
Short Circuit Current	I _{SC}	T _J = 25°C, V _I = -35V		300		mA
Peak Current	I _{PK}	T _J = 25°C		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

ELECTRICAL CHARACTERISTICS KA7918(C₁ = 2.2μF, C₀ = 1μF, T_J = 0 to 125°C, I_o = 500mA, V_I = 27V, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V _o	T _J = 25°C	- 17.3	- 18	- 18.7	V
		I _o = 5mA to 1A, P _o ≤ 15W V _I = - 22.5 to - 33V	- 17.1	- 18	- 18.9	
Line Regulation	ΔV _o	T _J = 25°C	V _I = - 21 to - 33V	15	360	mV
			V _I = - 24 to - 30V	8	180	
Load Regulation	ΔV _o	T _J = 25°C I _o = 5mA to 1.5A		15	360	mV
		T _J = 25°C I _o = 250 to 750mA		5	180	
Quiescent Current	I _q	T _J = 25°C		3	6	mA
Quiescent Current Change	ΔI _q	I _o = 5mA to 1A			0.5	mA
		V _I = - 22 to - 33V			1	
Output Voltage Drift	$\frac{\Delta V_o}{\Delta T}$	I _o = 5mA		- 1		mV/°C
Output Noise Voltage	V _N	f = 10Hz to 100KHz T _J = 25°C		300		μV
Ripple Rejection	RR	f = 120Hz ΔV _I = 10V	54	60		dB
Dropout Voltage	V _D	T _J = 25°C I _o = 1A		2		V
Short Circuit Current	I _{sc}	T _J = 25°C, V _I = - 35V		300		mA
Peak Current	I _{PK}	T _J = 25°C		2.2		A

* Load and line regulation are specified at constant junction temperature. Change in V_o due to heating effects must be taken into account separately. Pulse testing with low duty is used.

ELECTRICAL CHARACTERISTICS KA7924

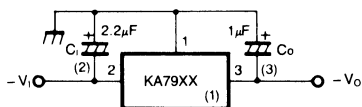
(C₁ = 2.2μF, C₀ = 1μF, T_J = 0 to 125°C, I_o = 500mA, V_I = 33V, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V _o	T _J = 25°C	- 23	- 24	- 25	V
		I _o = 5mA to 1A, P _o ≤ 15W V _I = - 27 to - 38V	- 22.8	- 24	- 25.2	
Line Regulation	ΔV _o	T _J = 25°C	V _I = - 27 to - 38V	15	480	mV
			V _I = - 30 to - 36V	8	240	
Load Regulation	ΔV _o	T _J = 25°C I _o = 5mA to 1.5A		15	480	mV
		T _J = 25°C I _o = 250 to 750mA		5	240	
Quiescent Current	I _Q	T _J = 25°C		3	6	mA
Quiescent Current Change	ΔI _Q	I _o = 5mA to 1A			0.5	mA
		V _I = - 27 to - 38V			1	
Output Voltage Drift	$\frac{\Delta V_o}{\Delta T}$	I _o = 5mA		- 1		mV/°C
Output Noise Voltage	V _N	f = 10Hz to 100KHz T _A = 25°C		400		μV
Ripple Rejection	RR	f = 120Hz ΔV _I = 10V	54	60		dB
Dropout Voltage	V _D	T _J = 25°C I _o = 1A		2		V
Short Circuit Current	I _{sc}	T _J = 25°C, V _I = - 35V		300		mA
Peak Current	I _{PK}	T _J = 25°C		2.2		A

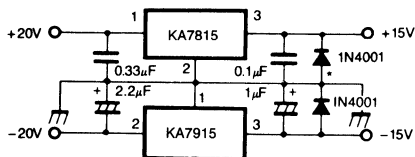
* Load and line regulation are specified at constant junction temperature. Change in V_o due to heating effects must be taken into account separately. Pulse testing with low duty is used.

APPLICATION INFORMATION

Fig. 1 — Fixed output regulator

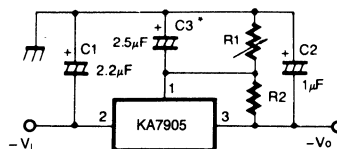
**Notes:**

- (1) To specify an output voltage, substitute voltage value for "XX".
- (2) Required for stability. For value given, capacitor must be solid tantalum. If aluminium electrolytics are used, at least ten times value shown should be selected. C_i is required if regulator is located an appreciable distance from power supply filter.
- (3) To improve transient response. If large capacitors are used, a high current diode from input to output (1N4001 or similar) should be introduced to protect the device from momentary input short circuit.

Fig. 2 — Split power supply ($\pm 15V/1A$)

* Against potential latch-up problems.

Fig. 3 — Circuit for increasing output voltage



$$V_o = V_{XX} \cdot \frac{R_1 + R_2}{R_2}$$

$$V_{XX}/R_2 > 3I_o$$

* C_3 optional for improved transient response and ripple rejection.

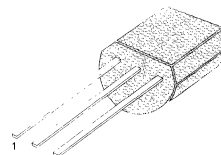
3-TERMINAL 0.1A NEGATIVE VOLTAGE REGULATORS

These regulators employ internal current limiting and thermal-shutdown, making them essentially indestructible.

FEATURES

- Output current up to 100mA
- No external components
- Internal thermal over load protection
- Internal short circuit current limiting

TO-92

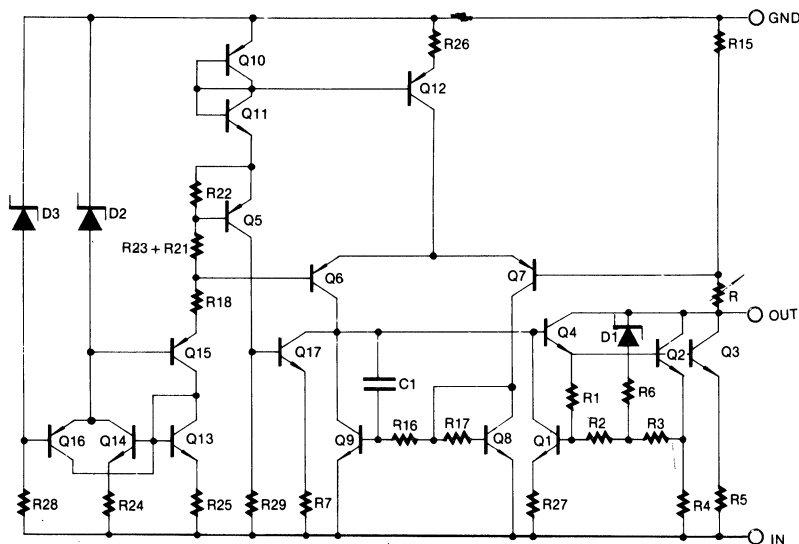


1: GND 2: Input 3: Output

ORDERING INFORMATION

Device	Package	Operating Temperature
KA79LXXAZ	TO-92	0 ~ 125°C

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise specified)

Characteristic	Symbol	Value	Unit
Input Voltage (–5V) (–12V to –18V) (–24V)	V_I	–30 –35 –40	V_{DC}
Operating Junction Temperature Range	T_{OPR}	0 ~ +125	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	–65 ~ +150	$^\circ\text{C}$

KA79L05A ELECTRICAL CHARACTERISTICS

($V_I = -10\text{V}$, $I_O = 40\text{mA}$, $C_I = 0.33\mu\text{F}$, $C_O = 0.1\mu\text{F}$, $0^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_O	$T_J = 25^\circ\text{C}$	–4.8	–5.0	–5.2	V
Line Regulation	ΔV_O	$T_J = 25^\circ\text{C}$		15	150	mV
		$-7.0\text{V} \geq V_I \geq -20\text{V}$			100	
Load Regulation	ΔV_O	$T_J = 25^\circ\text{C}$		20	60	mV
		$1.0\text{mA} \leq I_O \leq 100\text{mA}$		10	30	
Output Voltage	V_O	$-7.0\text{V} > V_I > -20\text{V}$, $1.0\text{mA} \leq I_O \leq 40\text{mA}$	–4.75		–5.25	V
		$V_I = -1.0\text{V}$, $1.0\text{mA} \leq I_O \leq 70\text{mA}$	–4.75		–5.25	
Quiescent Current	I_Q	$T_J = +25^\circ\text{C}$		2.0	6.0	mA
		$T_J = +125^\circ\text{C}$			5.5	
Quiescent Current Change	With Line	ΔI_Q			1.5	mA
	With Load				0.1	
Output Noise Voltage	V_N	$T_A = 25^\circ\text{C}$, $10\text{Hz} \leq f \leq 100\text{KHz}$		30		μV
Ripple Rejection	RR	$f = 120\text{Hz}$, $-8.0 \geq V_I \geq -18\text{V}$ $T_J = 25^\circ\text{C}$	41	60		dB
Dropout Voltage	V_D	$T_J = 25^\circ\text{C}$		1.7		V

* Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

KA79L12A ELECTRICAL CHARACTERISTICS

($V_I = -19V$, $I_O = 40mA$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, $0^\circ C \leq T_J \leq +125^\circ C$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_O	$T_J = 25^\circ C$	-11.5	-12.0	-12.5	V
Line Regulation	ΔV_O	$T_J = 25^\circ C$	-14.5V $\geq V_I \geq -27V$		250	mV
			-16V $\geq V_I \geq -27V$		200	
Load Regulation	ΔV_O	$T_J = 25^\circ C$	$1.0mA \leq I_O \leq 100mA$		100	mV
			$1.0mA \leq I_O \leq 40mA$		50	
Output Voltage	V_O	-14.5V $> V_I > -27V$, $1.0mA \leq I_O \leq 40mA$	-11.4		-12.6	V
		$V_I = -19V$, $1.0mA \leq I_O \leq 70mA$	-11.4		-12.6	
Quiescent Current	I_O	$T_J = +25^\circ C$			6.5	mA
		$T_J = +125^\circ C$			6.0	
Quiescent Current Change	With Line	ΔI_O	-16V $\leq V_I \leq -27V$		1.5	mA
	With Load				0.1	
Output Noise Voltage	V_N	$T_A = 25^\circ C$, $10Hz \leq f \leq 100KHz$		80		μV
Ripple Rejection	RR	$f = 120Hz$, $-15V \leq V_I \leq -25V$ $T_J = 25^\circ C$	37	42		dB
Dropout Voltage	V_D	$T_J = 25^\circ C$		1.7		V

* Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

KA79L15A ELECTRICAL CHARACTERISTICS

($V_I = -23V$, $I_O = 40mA$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, $0^\circ C \leq T_J \leq +125^\circ C$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_O	$T_J = 25^\circ C$	-14.4	-15.0	-15.6	V
Line Regulation	ΔV_O	$T_J = 25^\circ C$	-17.5V $\geq V_I \geq -30V$		300	mV
			-27V $\geq V_I \geq -30V$		250	
Load Regulation	ΔV_O	$T_J = 25^\circ C$	$1.0mA \leq I_O \leq 100mA$		150	mV
			$1.0mA \leq I_O \leq 40mA$		75	
Output Voltage	V_O	-17.5V $> V_I > -30V$, $1.0mA \leq I_O \leq 40mA$	-14.25		-15.75	V
		$V_I = -23V$, $1.0mA \leq I_O \leq 70mA$	-14.25		-15.75	
Quiescent Current	I_O	$T_J = +25^\circ C$			6.5	mA
		$T_J = +125^\circ C$			6.0	
Quiescent Current Change	With Line	ΔI_O	-20V $\leq V_I \leq -30V$		1.5	mA
	With Load				0.1	
Output Noise Voltage	V_N	$T_A = 25^\circ C$, $10Hz \leq f \leq 100KHz$		90		μV
Ripple Rejection	RR	$f = 120Hz$, $-18.5V \leq V_I \leq -28.5V$ $T_J = 25^\circ C$	34	39		dB
Dropout Voltage	V_D	$T_J = 25^\circ C$		1.7		V

* Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

KA79L18A ELECTRICAL CHARACTERISTICS(V_I = -27V, I_O = 40mA, C_I = 0.33μF, C_O = 0.1μF, 0°C ≤ T_J ≤ +125°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V _O	T _J = 25°C	-17.3	-18.0	-18.7	V
Line Regulation	ΔV _O	T _J = 25°C	-20.7V ≥ V _I ≥ -33V		325	mV
			-21V ≥ V _I ≥ -33V		275	
Load Regulation	ΔV _O	T _J = 25°C	1.0mA ≤ I _O ≤ 100mA		170	mV
			1.0mA ≤ I _O ≤ 40mA		85	
Output Voltage	V _O	-20.7V > V _I > -33V, 1.0mA ≤ I _O ≤ 40mA	-17.1		-18.9	V
		V _I = -27V, 1.0mA ≤ I _O ≤ 70mA	-17.1		-18.9	
Quiescent Current	I _O	T _J = +25°C			6.5	mA
		T _J = +125°C			6.0	
Quiescent Current Change	With Line	ΔI _O	-21V ≤ V _I ≤ -33V		1.5	mA
	With Load				0.1	
Output Noise Voltage	V _N	T _A = 25°C, 10Hz ≤ f ≤ 100KHz		150		μV
Ripple Rejection	RR	f = 120Hz, -23V ≤ V _I ≤ -33V T _J = 25°C	33	48		dB
Dropout Voltage	V _D	T _J = 25°C		1.7		V

* Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

KA79L24A ELECTRICAL CHARACTERISTICS(V_I = -33V, I_O = 40mA, C_I = 0.33μF, C_O = 0.1μF, 0°C ≤ T_J ≤ +125°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V _O	T _J = 25°C	-23	-24	-25	V
Line Regulation	ΔV _O	T _J = 25°C	-27V ≥ V _I ≥ -38V		350	mV
			-28V ≥ V _I ≥ -38V		300	
Load Regulation	ΔV _O	T _J = 25°C	1.0mA ≤ I _O ≤ 100mA		200	mV
			1.0mA ≤ I _O ≤ 40mA		100	
Output Voltage	V _O	-27V > V _I > -38V, 1.0mA ≤ I _O ≤ 40mA	-22.8		-25.2	V
		V _I = -33V, 1.0mA ≤ I _O ≤ 70mA	-22.8		-25.2	
Quiescent Current	I _O	T _J = +25°C			6.5	mA
		T _J = +125°C			6.0	
Quiescent Current Change	With Line	ΔI _O	-28V ≤ V _I ≤ -38V		1.5	mA
	With Load				0.1	
Output Noise Voltage	V _N	T _A = 25°C, 10Hz ≤ f ≤ 100KHz		200		μV
Ripple Rejection	RR	f = 120Hz, -29V ≤ V _I ≤ -35V T _J = 25°C	31	47		dB
Dropout Voltage	V _D	T _J = 25°C		1.7		V

* Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

TYPICAL APPLICATION

Design Considerations

The KA79LXXA Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition. Internal Short-Circuit Protection that limits the maximum current the circuit will pass.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass

capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A $0.33\mu\text{F}$ or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulator's input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

Fig. 1 POSITIVE AND NEGATIVE REGULATOR

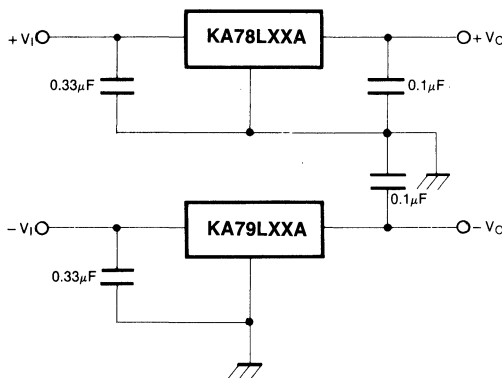
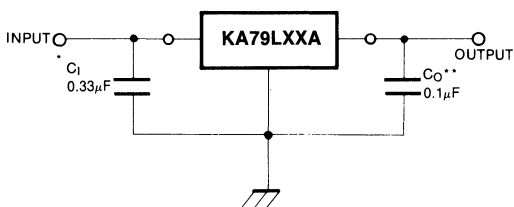


Fig. 2 TYPICAL APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0V above the output voltage even during the low point on the input ripple voltage.

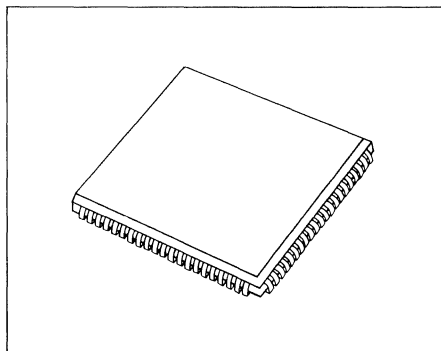
* = C_1 is required if regulator is located an appreciable distance from power supply filter.

** = C_O improves stability and transient response.

DESCRIPTION

The KDA0458 is a 256 color RAM DAC which is designed for high performance, high resolution color graphics applications. This device consists of color palette RAMs of 256×24 bit, overlay registers of 4×24 bit and triple 8-bit DACs. 4 overlay registers support overlaying cursor, grids and menus. Its frequency range can support resolution up to 1280×1024 pixels, while displaying 256 simultaneous colors out of a total palette of 16.8 million.

A 40-bit pixel ports with internal 5:1 or 4:1 multiplexer/latch allows direct connection to a frame buffer. There are only two ECL inputs (CLK, $\overline{\text{CLK}}$) which are provided for high frequency pixel rate of high resolution systems. The KDA0458 generates RS-343A compatible video outputs capable of directly driving a doubly-terminated 75Ω load without requiring external buffering.



FEATURES

- Snow-free display
- 135, 110 and 80MHz pixel rates
- Functionally compatible with Brooktree™ Bt458
- 4:1 or 5:1 input MUX
- 256×24 dual port color palette SRAM
- 4×24 dual port overlay registers
- RS-343A compatible outputs
- Standard MPU interface
- Programmable read and blink mask registers
- Internal or external voltage reference
- Single +5V power supply
- Fixed eight pipeline delay

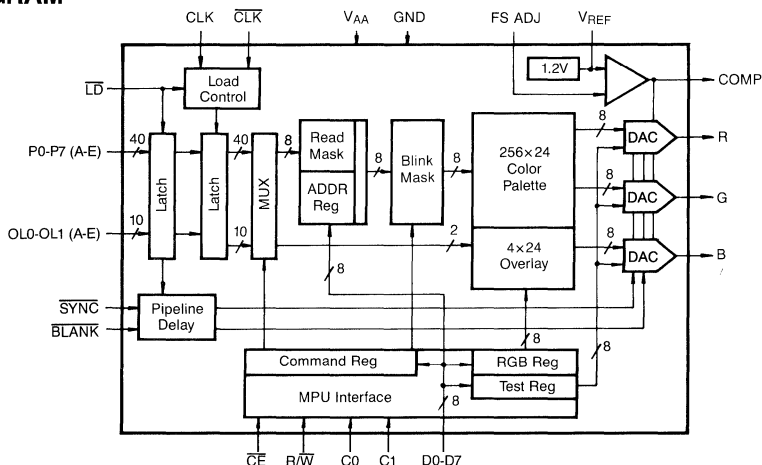
TYPICAL APPLICATIONS

- High resolution color graphics
- CAE/CAD/CAM
- Image processing
- Instrumentation

ORDERING INFORMATION

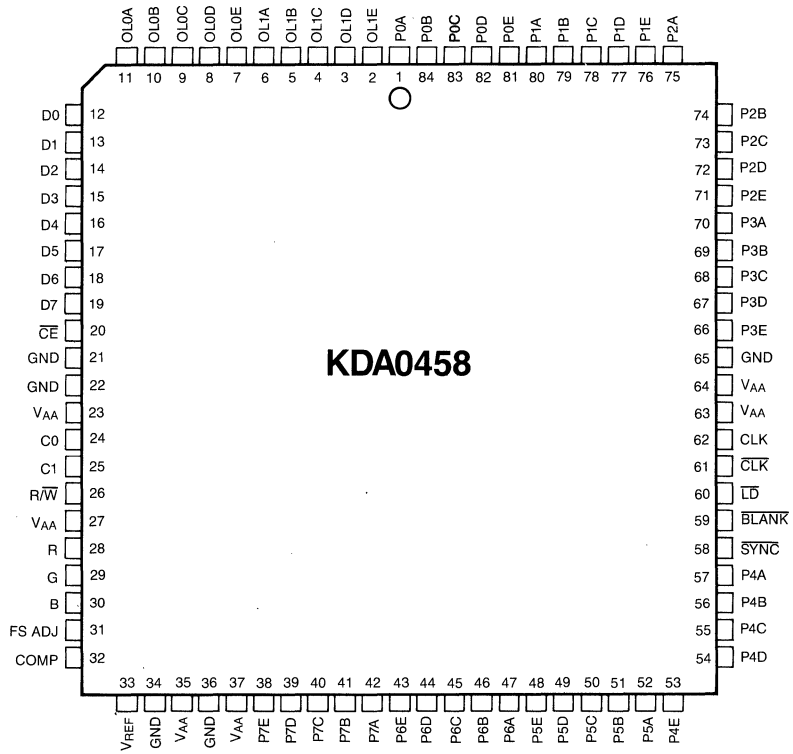
Marking Spec	RAM	DACs	Speed	Package	Temperature Range
KDA0458L-135	256×24	Triple 8-bit	135MHz	84-Pin PLCC	0~+70°C
KDA0458L-110	256×24	Triple 8-bit	110MHz	84-Pin PLCC	0~+70°C
KDA0458L-80	256×24	Triple 8-bit	80MHz	84-Pin PLCC	0~+70°C

BLOCK DIAGRAM



Brooktree™ is a registered trademark of Brooktree Corporation.

PIN CONFIGURATION



ELECTRICAL SPECIFICATIONS**Absolute Maximum Ratings**

Characteristics	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	V_{AA}			7.0	V
Voltage on Any Digital Pin	V_{IN}	GND–0.3		$V_{AA} + 0.3$	V
Analog Output Short Circuit Duration to Any Power Supply or GND	I_{SC}		Indefinite		
Operating Temperature Range (ambient)	T_O	– 55		125	°C
Storage Temperature Range	T_{Stg}	– 65		150	°C
Junction Temperature Range	T_J			150	°C
Soldering Temperature (5 seconds, 1/4" from pin)	T_{sol}			260	°C
Vapor Phase Soldering (1 minute)	T_{vsol}			220	°C

Note: 1. Absolute Maximum Ratings are limiting values applied individually while all other parameters are within specified operating conditions.
 2. Function operation under any of these conditions is not implied.
 3. Applied voltage must be current limited to specified range.
 4. Current is specified as positive when flowing into the device.

Recommended Operating Conditions

Characteristics	Symbol	Min	Typ	Max	Unit
Operating Supply Voltage	V_{AA}	4.75	5.00	5.25	V
Operating Temperature Range	T_O	0		70	°C
Output Load (effective)	R_L		37.5		Ω
Reference Voltage	V_{REF}	1.2	1.235	1.26	V
FS ADJ Resistor	R_{SET}		523		Ω

Note: It is strongly recommended that all the supply pins be powered from the same source.

DC Characteristics

Characteristics	Test Condition	Symbol	Min	Typ	Max	Unit
DAC Resolution (each DAC)		RES	8	8	8	Bits
DAC Accuracy (each DAC)						
Integral Linearity Error		IL			± 1	LSB
Differential Linearity Error		DL			± 1	LSB
Gray Scale Error					± 5	%Gray
Digital Input High Voltage	Except CLK, $\overline{\text{CLK}}$	V _{IH}	2.0		V _{AA} +0.3	V
Digital Input Low Voltage	Except CLK, $\overline{\text{CLK}}$	V _{IL}	GND-0.3		0.8	V
Digital Input High Current	Except CLK, $\overline{\text{CLK}}$, V _{IN} =2.4V	I _{IH}			1	μA
	Only CLK, $\overline{\text{CLK}}$, V _{IN} =4.0V	I _{IHC}			1	μA
Digital Input Low Current	Except CLK, $\overline{\text{CLK}}$, V _{IN} =0.4V	I _{IL}			-1	μA
	Only CLK, $\overline{\text{CLK}}$, V _{IN} =0.4V	I _{ICL}			-1	μA
Digital Input Capacitance	Except CLK, $\overline{\text{CLK}}$, V _{IN} =2.4V	C _{IN}		4	10	pF
	f=1MHz					
	Only CLK, $\overline{\text{CLK}}$, V _{IN} =4.0V	C _{INC}		4	10	pF
	f=1MHz					
Digital Output High Voltage	I _{OH} =-800 μA	V _{OH}	2.4			V
Digital Output Low Voltage	I _{OL} =6.4mA	V _{OL}			0.4	V
Digital Output 3-State Current		I _{OZ}			10	μA
Digital Output Capacitance		C _{DO}		10		pF
Analog Outputs				20		mA
Gray Scale Current Range						
White to Blank			17.69	19.05	20.40	mA
White to Black			16.74	17.62	18.50	mA
Black to Blank			0.95	1.44	1.90	mA
Blank on R, B			0	5	50	μA
Blank on G			6.29	7.62	8.96	mA
Sync on G			0	5	50	μA
LSB Size				69.1		μA
DAC to DAC Matching				2	5	%
Output Compliance		V _{OC}	- 0.4		1.2	V
Output Impedance		R _{AO}		50		K Ω
Output Capacitance	f=1MHz, I _{OUT} =0mA	C _{DO}		13	20	pF
Voltage Reference Input Current		I _{VREF}		10		μA
Power Supply Rejection Ratio	C _{COMP} =0.1 μF , f=1KHz	PSRR		0.5		%/% Δ V _{AA}

Test Conditions:

- R_{SET}=523 Ω , V_{REF}=1.235V.
- TTL input levels are 0 to 3V with less than 3ns rise/fall times between 10% and 90% points. ECL input levels are V_{AA}-0.8V to V_{AA}-1.8V with less than 3ns rise/fall times between 20% and 80% points. CLK and $\overline{\text{CLK}}$ swings are adequate for driving the KDA0458. For input and output signals, timing reference points at 50% for inputs and outputs. Analog output load < 10pF, D0-D7 output load < 40pF. (see Fig. 2)
- As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on room temperature and V_{AA}=5V.

AC Characteristics

Characteristics	Symbol	135MHz Version			110MHz Version			Unit
		Min	Typ	Max	Min	Typ	Max	
Clock Rate	f_{MAX}			135			110	MHz
Clock Cycle Time	Tclk	7.4			9.09			ns
Clock Pulse Width High Time	Tckh	3.0			4			ns
Clock Pulse Width Low Time	Tckl	3.0			4			ns
LD Rate	LD _{MAX}			33.75			27.5	MHz
LD Cycle Time	Tld	29.62			36.36			ns
LD Pulse Width High Time	Tldh	13			15			ns
LD Pulse Width Low Time	Tldl	13			15			ns
CE Low Time	TL	50			50			ns
CE High Time	Th	25			25			ns
CE Low to Data Bus Driven	Tdr	7			7			ns
CE Low to Data Valid	Tva			75			75	ns
CE Low to Data Bus 3-States	T3st			15			15	ns
R/W, C0, C1 Setup Time	Tsrs	0			0			ns
R/W, C0, C1 Hold Time	Thrs	15			15			ns
Write Data Setup Time	Tswd	35			35			ns
Write Data Hold Time	Thwd	3			3			ns
Pixel and Control Setup Time	Tsp _x	3			3			ns
Pixel and Control Hold Time	Thp _x	2			2			ns
Analog Output Delay	Td		12			12		ns
Analog Output Rise Time	Tr		2			2		ns
Analog Output Fall Time	Tf		2			2		ns
Analog Output Settling Time	Tset			8			8	ns
Clock and Data Feedthrough#	FDTHR		35			35		pV-sec
Glitch Impulse#	GI		50			50		pV-sec
DAC to DAC Crosstalk	XTAK		-23			-23		dB
Analog Output Skew	T _{SKW}		0	2		0	2	ns
Pipeline Delay	T _{DP}	8	8	8	8	8	8	Clocks
VAA Supply Current##	IAA		240	335		210	315	mA

AC Characteristics (Continued)

Characteristics	Symbol	80MHz Version			Units
		Min	Typ	Max	
Clock Rate	f_{MAX}			80	MHz
Clock Cycle Time	Tclk	12.5			ns
Clock Pulse Width High Time	Tckh	5			ns
Clock Pulse Width Low Time	Tckl	5			ns
LD Rate	LD _{MAX}			20	MHz
LD Cycle Time	Tld	50			ns
LD Pulse Width High Time	Tldh	20			ns
LD Pulse Width Low Time	Tldl	20			ns
CE Low Time	TL	50			ns
CE High Time	Th	25			ns
CE Low to Data Bus Driven	Tdr	7			ns
CE Low to Data Valid	Tva			75	ns
CE Low to Data Bus 3-Stated	T3st			15	ns
R/W, C0, C1 Setup Time	Tsrs	0			ns
R/W, C0, C1 Hold Time	Thrs	15			ns
Write Data Setup Time	Tswd	35			ns
Write Data Hold Time	Thwd	3			ns
Pixel and Control Setup Time	Tspx	4			ns
Pixel and Control Hold Time	Thpx	2			ns
Analog Output Delay	Td		12		ns
Analog Output Rise Time	Tr		2		ns
Analog Output Fall Time	Tf		2		ns
Analog Output Settling Time	Tset			8	ns
Clock and Data Feedthrough#	FDTHR		35		pV-sec
Glitch Impulse#	GI		50		pV-sec
DAC to DAC Crosstalk	XTAK		-23		dB
Analog Output Skew	TSKW		0	2	ns
Pipeline Delay	T _{DP}	8	8	8	Clocks
V _{AA} Supply Current##	IAA		200	285	mA

Test Conditions:

- R_{SET} = 523Ω, V_{REF} = 1.235V.
- TTL input levels are 0 to 3V with less than 3ns rise/fall times between 10% and 90% points. ECL input levels are V_{AA} - 0.8V to V_{AA} - 1.8V with less than 3ns rise/fall times between 20% and 80% points. CLK and CLK swings are adequate for driving the KDA0458. For input and output signals, timing reference points at 50% for inputs and outputs. Analog output load < 10pF, D0-D7 output load < 40pF. (see Fig. 2)
- # Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1KΩ resistor to ground are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough.
- ## Ai Fmax I_{AA}(Typ) at V_{AA} = 5.0V, T_O = 20°C. I_{AA} (Max) at V_{AA} = 5.25V, T_O = 0°C.
- As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on room temperature and V_{AA} = 5V.

Timing Diagram

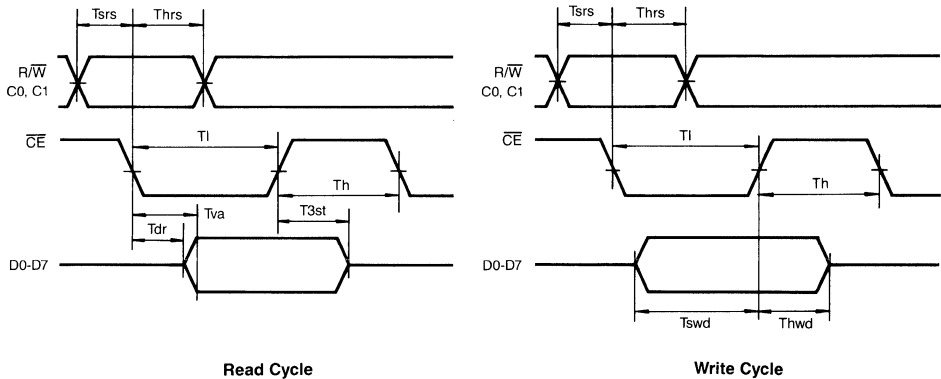


Fig. 1 MPU Read/Write Timing

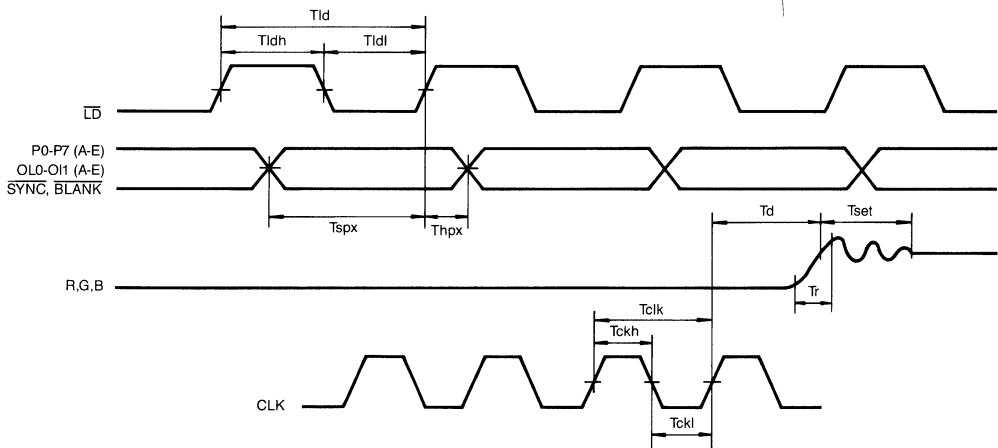


Fig. 2 Video Input/Output Timing

- Output delay is measured from the 50% point of the rising edge of CLK to the full scale transition.
- Setting time is measured from the 50% point of full scale transition to the output remaining within $\pm 1\text{LSB}$.
- Output rise/fall time is measured between the 10% and 90% point of full scale transition.

PIN DESCRIPTION

Symbol	Signal Name	I/O	Description																				
C0, C1	Command Control	I	These inputs specify the type of read or write operation being performed, as shown in Table 1. C0 and C1 are latched on the falling edge of $\overline{CE}$.																				
R/ $\overline{W}$	Read/Write Control	I	R/ $\overline{W}$ is latched on the falling edge of $\overline{CE}$. For reading data from the device, $\overline{CE}$ must be a logical 0 and R/ $\overline{W}$ must be a logical 1. For writing data to the device, $\overline{CE}$ and R/ $\overline{W}$ should be a logical 0.																				
D0-D7	Bidirectional Data Bus	I/O	D0-D7 is data port which enables the reading of data from or the writing of data to the Read Mask Register, Blink Mask Register, Command register, Test Register, Overlay Register and Color Palette RAM. The Address Register is also accessed from the D0-D7 port.																				
$\overline{CE}$	Chip Enable Control	I	To enable the device for read or write operation this input must be logical 0. During write operations, data is internally latched on the rising edge of $\overline{CE}$. $\overline{CE}$ is an edge triggered input and care should be taken to avoid glitches on this line.																				
CLK CLK	Pixel Clock Inputs	I	These differential clock inputs are driven by ECL logic which is configured CLK for single supply (5V) operation. CLK frequency is typically the pixel clock rate of the system.																				
$\overline{LD}$	Load Control Input	I	The P0-P7 (A-E), $\overline{BLANK}$, and $\overline{SYNC}$ inputs are all latched on the rising edge of $\overline{LD}$. This signal is either 1/4 or 1/5 the CLK rate and could be phase independent relative to the CLK and CLK inputs.																				
P0-P7 (A-E)	Pixel Select Inputs	I	There are five sets of pixel data (A-E). Each set has up to 8 bits (P0-P7). Either four or five consecutive pixels are input through this port. Due to the pipelined nature of the device, the (A) pixel is output first, followed by the (B) pixel etc., until all four or five pixels have been output, at which time the cycle repeats. These inputs are used to specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. They are latched on the rising edge of $\overline{LD}$. Unused inputs should be connected to GND.																				
OL0-OL1 (A-E)	Overlay Select Inputs	I	There are four overlay registers which can be selected by OL0 and OL1 for up to five consecutive pixels (A-E). When accessing the overlay palette, the P0-P7 (A-E) inputs are ignored. OL0 and OL1 (A-E) inputs are latched on the rising of $\overline{LD}$. Based on the setting of bit 6 in command register (CR6), the following color palette will be selected: <table border="1"> <thead> <tr> <th>OL1</th><th>OL0</th><th>CR6 = 1</th><th>CR6 = 0</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>Color Palette RAM</td><td>Overlay Color 0</td></tr> <tr> <td>0</td><td>1</td><td>Overlay Color 1</td><td>Overlay Color 1</td></tr> <tr> <td>1</td><td>0</td><td>Overlay Color 2</td><td>Overlay Color 2</td></tr> <tr> <td>1</td><td>1</td><td>Overlay Color 3</td><td>Overlay Color 3</td></tr> </tbody> </table> Unused inputs should be connected to GND.	OL1	OL0	CR6 = 1	CR6 = 0	0	0	Color Palette RAM	Overlay Color 0	0	1	Overlay Color 1	Overlay Color 1	1	0	Overlay Color 2	Overlay Color 2	1	1	Overlay Color 3	Overlay Color 3
OL1	OL0	CR6 = 1	CR6 = 0																				
0	0	Color Palette RAM	Overlay Color 0																				
0	1	Overlay Color 1	Overlay Color 1																				
1	0	Overlay Color 2	Overlay Color 2																				
1	1	Overlay Color 3	Overlay Color 3																				

PIN DESCRIPTION (Continued)

Symbol	Signal Name	I/O	Description
$\overline{\text{BLANK}}$	Composite Blank Control	I	A logic 0 on this input will drive the analog outputs to the blanking level (see Fig. 4) after the pipeline delay. This is latched on the rising edge of $\overline{\text{LD}}$. When the $\overline{\text{BLANK}}$ is a logical 0, the pixel and overlay inputs are ignored.
$\overline{\text{SYNC}}$	Composite Sync Control	I	A logic 0 on this input switches off a 40 IRE current source on the G output (see Fig. 4) after the pipeline delay. $\overline{\text{SYNC}}$ does not override any other control or data input, therefore, it should be asserted only during the blanking interval. $\overline{\text{SYNC}}$ is latched on the rising edge of $\overline{\text{LD}}$. If sync information is not needed on the G output, this pin should be connected to a GND.
COMP	Compensation	I	To reduce the effect of noise on power supply, this pin provides compensation for the internal reference amplifier. A bypass ceramic capacitor of 0.1 μF with the shortest lead possible must be connected between this pin and V_{AA} (Fig. 6) to improve the PSRR. The COMP capacitor must be as close to the device as possible.
FS ADJ	Full Scale Adjust Control	I	The full scale output current levels of the KDA0458 are determined by the value of the resistor (R_{SET}) which is connected between this pin and GND (Fig. 6). The relationship between R_{SET} and the full scale output current on G is: $R_{\text{SET}}(\Omega) = 11,294 \times V_{\text{REF}}(\text{V}) / I_{\text{OG}}(\text{mA})$ the full scale output current on R and B for a given is: $I_{\text{OR}}, I_{\text{OB}}(\text{mA}) = 8,067 \times V_{\text{REF}}(\text{V}) / R_{\text{SET}}(\Omega)$
R,G,B	Red, Green, Blue Outputs	O	These high impedance current sources are capable of directly driving a doubly-terminated 75 Ω coaxial cable (Fig. 6)
V_{REF}	Voltage Reference Input	I	The external reference voltage, if used, must be applied to this input such as the one shown in Fig. 6. This reference voltage is typically 1.235V. A bypass ceramic capacitor of 0.1 μF with the shortest lead must be connected between this pin and V_{AA} . This decoupling capacitor must be as close to the device as possible. The use of a resistor network to generate the reference voltage is not recommended. When internal voltage reference is used, this pin should be left open.
V_{AA}	Analog Power	I	All V_{AA} pins must be connected together.
GND	Analog Ground	I	All GND pins must be connected together.

DEVICE DESCRIPTION

MPU Interface

The C0 and C1 control inputs analog with the address register (AD) indicate which internal register or color palette location is being accessed (Table 1).

The address register is loaded through the D0-D7 pins with D0 being the LSB (Fig.3). This is a continuous counter and rolls over from 00h to FFh when incremented. The address register has two additional bits (a0, a1). The bits a0 and a1 repeatedly count 00, 01 and 10, maintaining the sequence of red, green and blue read/write cycles.

To read data from the overlay register or color palette RAM, the MPU must first load the address register with the address of the overlay register or color palette RAM location to be read. The color content from the location pointed to by AD is copied into the RGB registers. Three successive read cycles 8-bits each, for red, green and blue respectively, are required to read one location of the color palette. After the Blue read cycle the address register is auto-incremented to the next location. The MPU can perform continuous block read cycles simply by specifying the block start address and continuously reading red, green and blue data.

To write color data to the overlay register or color palette RAM, the MPU must first write the address location specified by the address register. Then, three successive write cycles are performed. After the blue write cycle, the three byte of color data are combined into a 24-bit word and written to the location specified by the address register. Then the address register is auto-incremented to the next location.

The MPU can perform continuous block write cycles simply by specifying the block start address and continuously writing red, green and blue data.

C1	C0	Address Register		Addressed by MPU
		AD0-AD7	a1, a0	
			0 0 0 1 1 0	Red Green Blue
0	0	XXh		Address Register
0	1	00h - FFh		Color Palette RAM
1	1	00h - 03h		Overlay Register
1	0	04h 05h 06h 07h		Read Mask Register Blink Mask Register Command Register Test Register

Table 1. Address Register Operation

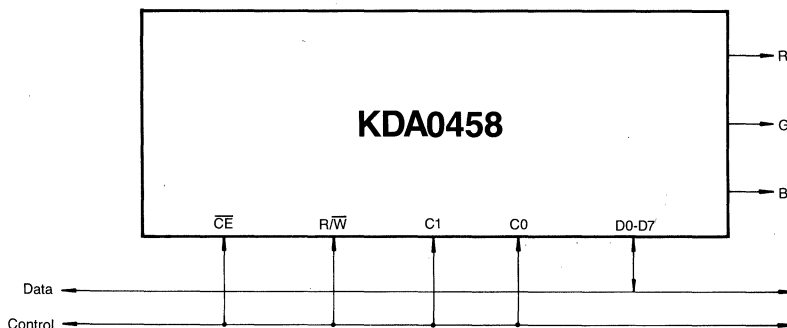


Fig. 3. MPU Interface

Initializing the KDA0458

Upon power-up, the state of the internal registers, overlay registers, and color palette RAM are not defined. Therefore, the KDA0458 must be initialized before any display operation may begin. To initialize the internal registers and color palette, the host computer writes data into the internal registers, overlay registers, and color palette RAM using the C0, C1, and D0-D7 inputs.

Since the pipeline delay of the KDA0458 is fixed at eight CLK cycles, there is no need to perform the pipeline reset functions upon power-up. Performing pipeline reset operations on KDA0458 will have no effect on its operation. The command register must be re-initialized any time the multiplex selection is changed (i.e., from 4:1 to 5:1 input multiplexing).

The following sequence of write commands will initialize a KDA0458 to 4:1 multiplexing, no overlays, and no blinking.

C1	C0	Operation	Function
0	0	Write 04h to Address Register	Access Read Mask Register
1	0	Write FFh to Read Mask Register	Enable All Pixel Inputs
0	0	Write 05h to Address Register	Access Blink Mask Register
1	0	Write 00h to Blink Mask Register	Disable All Blinking
0	0	Write 06h to Address Register	Access Command Register
1	0	Write 40h to Command Register	Initialize Command Register
0	0	Write 07h to Address Register	Access Test Register
1	0	Write 00h to Test Register	Initialize Test Register
0	0	Write 00h to Address Register	Access Color Palette RAM
0	1	Write Red Value to RAM Location 00h	Write Red Value
0	1	Write Green Value to RAM Location 00h	Write Green Value
0	1	Write Blue Value to RAM Location 00h	Write Blue Value
0	1	Write Red Value to RAM Location 01h	Write Red Value
0	1	Write Green Value to RAM Location 01h	Write Green Value
0	1	Write Blue Value to RAM Location 01h	Write Blue Value
0	1	Write Red Value to RAM Location FFh	Write Red Value
0	1	Write Green Value to RAM Location FFh	Write Green Value
0	1	Write Blue Value to RAM Location FFh	Write Blue Value
0	0	Write 00h to Address Register	Access Overlay Register
1	1	Write Red Value to Overlay Location 00h	Write Red Value
1	1	Write Green Value to Overlay Location 00h	Write Green Value
1	1	Write Blue Value to Overlay Location 00h	Write Blue Value
1	1	Write Red Value to Overlay Location 00h	Write Red Value
1	1	Write Green Value to Overlay Location 03h	Write Green Value
1	1	Write Blue Value to Overlay Location 03h	Write Blue Value

Table 2. Initialization Routine for KDA0458

Snow-Free Operation

In most RAM DAC's frequent accesses (Reads or Writes) to the color palette RAM or overlay registers (e.g., Block writes) during display refresh result in noticeable disturbances on the screen. This is referred to as "SNOW". To avoid this, programmers resorted to polling for the blanking interval before making such accesses, resulting in less than optimum system performance. Since Samsung's design of KDA0458 use dual ported color palette and overlay registers, programmers are free from this restriction. Any number of accesses to the color palette RAM and overlay registers can be made during screen refresh without screen disturbances.

Frame Buffer Interface

The input architecture of the KDA0458 compensates for the slower pixel data output rates of the frame buffer in very high resolution graphics systems. The internal latches and multiplexers allow several pixels to be loaded at frame buffer output rates and shifted out one by one at pixel clock rates. On the rising edge of the load control input ($\overline{LD}$) (see Fig. 2), the following information is latched: SYNC and BLANK information, pixel input data (P0-P7) (A-E) and overlay input data (OL0-OL1) (A-E)). The number of pixels being stored is either four or five, depending on mux selection criteria (4:1 or 5:1). During each pixel clock cycle, the KDA0458 outputs color information based on previous pixel inputs (A-E). Once all four or five pixels are sent to the display unit, the cycle repeats itself by loading the next set of pixel inputs. Signal relative to the clock, makes the design of frame buffer easier. This is done by externally dividing the CLK signal by four or five to generate the $\overline{LD}$ signal, eliminating the skew that is usually generated by propagation delays of the $\overline{LD}$ control logic. So, independent of clock phase, the pixel and overlay data are latched on the rising edge of the $\overline{LD}$. Internal logic generates a pseudo LOAD signal that is synchronous to CLK. This signal is guaranteed to follow the $\overline{LD}$ signal by at least one clock cycle and not more than three. The main function of this pseudo LOAD signal is to transfer the latched pixel and overlay data into a second set of latches, which are internally multiplexed at the pixel rate. For the cases where 4:1 multiplexing is specified, only one rising edge of $\overline{LD}$ should occur every four Pixel clock cycles. Similarly for 5:1 multiplexing scheme, only one rising edge of $\overline{LD}$ should occur every five clock cycles. Otherwise, the internal LOAD generation circuitry will not be able to synchronize and lock to external $\overline{LD}$.

Color Selection

Table 3 shows the color palette and overlay selection criteria. There are eight bits of color(P0-P7)and two bits of overlay information(OL0-OL1) for each pixel that needs to be processed every clock cycle by the read mask, blink mask and command register. These programmable registers not only control the display of individual bit planes but also the rate at which they blink. During active display time, accessing the blink mask register could cause an undesirable color change. To eliminate this artifact, the KDA0458 checks the video timing for vertical retrace intervals and allows the change to be made only during blanking time. A vertical retrace interval is identified by monitoring the BLANK input signal and detecting that the BLANK signal has been logically low for a minimum of $256 \times (\overline{LD} \text{ cycles})$.

CR6	OL1	OL0	P0-P7	Color Information
1	0	0	00h	Color Palette Location 00h
1	0	0	01h	Color Palette Location 01h
:	:	:	:	:
1	0	0	FFh	Color Palette Location FFh
0	0	0	xxh	Overlay Color 0
x	0	1	xxh	Overlay Color 1
x	1	0	xxh	Overlay Color 2
x	1	1	xxh	Overlay Color 3

Table 3. Color Palette & Overlay Selection

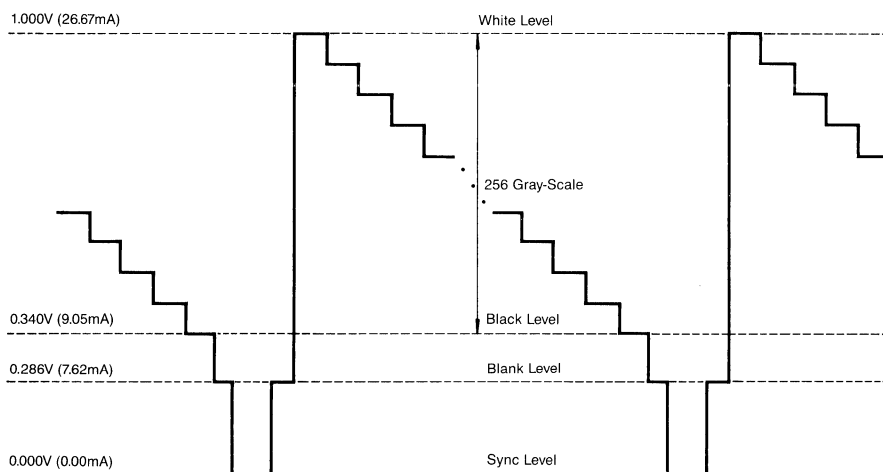
Video Output

The data from color palette RAMs or overlay registers are supplied to internal DAC every pixel clock. The KDA0458 uses a segmented architecture for its internal DACs. As a result, the switching transient response is in essence reduced and monotonicity and low glitch are guaranteed.

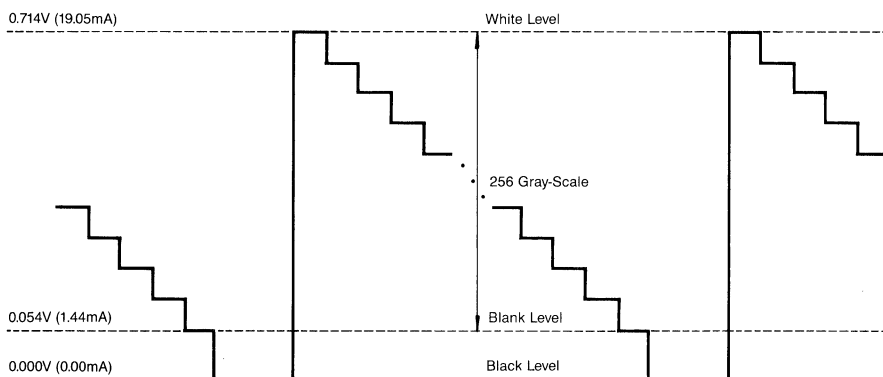
By pipelining the SYNC and BLANK inputs, synchronization with pixel data is maintained and current output is internally adjusted to generate the specific levels required for composite video output waveforms (see Fig. 4).

The KDA0458 contains the SYNC information only on the output of the green DAC (G). Fig 4 shows how the SYNC inputs modify the output level.

G Output Waveforms



R and B Output Waveforms



Note: $R_L = 75\Omega$ (doubly-terminated), $R_{SET} = 523\Omega$, $V_{REF} = 1.235V$

Fig. 4. Composite Video Output Waveforms

INTERNAL REGISTER

Command Register

The Command Register is 8 bits wide and its content can be written to or read by the MPU. The purpose of the Command Register is to select various functions within the RAM DAC such as: Overlay display enable, Overlay blink enable, Overlay blink rate, Color palette RAM enable, and Multiplex ratio.

A detailed description of bit functions within the command register is shown below:

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0	(CR0 corresponds to LSB on the data bus (D0))
Bit	Function		Comments					
CR0	OL0 Display Enable 0: Disable 1: Enable		If this bit is set to 1, there is no impact on the value of the OL0 (A-E) inputs. If this bit is set to 0, it forces the OL0 (A-E) inputs to be logical zero prior to selecting the palettes.					
CR1	OL1 Display Enable 0: Disable 1: Enable		If this bit is set to 1, there is no impact on the value of the OL1 (A-E) inputs. If this bit is set to 0, it forces the OL1 (A-E) inputs to be logical zero prior to selecting the palettes.					
CR2	OL0 Blink Enable 0: Disable 1: Enable		This bit when to 1, forces the OL0 (A-E) inputs to toggle between a logical 0 and the input value at the selected blink rate prior to selecting the palettes. In order for overlay 0 bit plane to blink, bit CR0 must be set to a logical one. If this bit is set to 0, there is no effect on the value of the OL0 (A-E) inputs.					
CR3	OL1 Blink Enable 0: Disable 1: Enable		This bit when to 1, forces the OL1 (A-E) inputs to toggle between a logical 0 and the input value at the selected blink rate prior to selecting the palettes. In order for overlay 1 bit plane to blink, bit CR1 must be set to a logical one. If this bit is set to 0, there is no effect on the value of the OL1 (A-E) inputs.					
CR4 CR5	Blink Rate Selection		CR4 and CR5 control the duty cycle time and blink rate cycle time. The numbers in parentheses specify the duty cycle, and the number of vertical retrace intervals are also shown. 0 0 16 on, 48 off (25% duty cycle every 64 vertical intervals) 0 1 16 on, 16 off (50% duty cycle every 32 vertical intervals) 1 0 32 on, 32 off (50% duty cycle every 64 vertical intervals) 1 1 64 on, 64 off (50% duty cycle every 128 vertical intervals)					
CR6	RAM Enable 0: Use Overlay Color 0 1: Use Color Palette RAM		When the overlay select bits are OL0=0, OL1=0 this bit specifies whether to use the color palette RAM (1) or overlay color (0) for providing color data.					
CR7	Multiplex Select		This bit specifies whether 4:1 or 5:1 multiplexing is to be used for the pixel and overlay inputs. For 4:1 case, the (E) pixel and (E) overlay inputs are ignored. However, all of the pixel data and overlay inputs associated with (E) should be grounded. LD input signal should also be 1/4 the CLK rate. If 5:1 is selected, all of the pixel data and overlay inputs are used and the LD input should be 1/5 the CLK rate.					

Read Mask Register

This register is used to enable or disable a bit plane from addressing the color palette RAM. D0 corresponds to bit plane 0 (P0 (A-E)) and D7 corresponds to bit plane 7 (P7 (A-E)). Each register bit is logically ANDed with the corresponding bit plane input, therefore, setting a bit to one it would enable the matching bit plane. Read mask register may be written to or read by the MPU at any time and is not initialized.

Blink Mask Register

This register is used to enable or disable a bit plane from blinking at the blink rate and duty cycle specified by the command register. D0 corresponds to bit plane 0 (P0 (A-E)) and D7 corresponds to bit plane 7 (P7 (A-E)). Setting a bit in this register would be enable the matching bit plane to blink if the corresponding bit in read mask register is also set. This register may be written to or read by the MPU and must be initialized for correct operation.

Test Register

This register facilitates observation of the digital data presented to the DAC. The four LSBs, D0-D3, of the test register are used to select which data is to be presented at the D0-D7 port. When writing to this register, D4-D7 are discarded. The contents of the test register are defined as follows:

	Bit Functions	Write Value (D0-D7)	Data Selected for D4-D7
D7-D4	Read Data (one nibble of red, green or blue)	01h (0001)	Read red MSB nibble
D3	Upper (logical 0) or Lower (logical 1) nibble select	02h (0010)	Read green MSB nibble
D2	Blue Enable	04h (0100)	Read blue MSB nibble
D1	Green Enable	09h (1001)	Read red LSB nibble
D0	Red Enable	0Ah (1010)	Read green LSB nibble
		0Ch (1100)	Read blue LSB nibble

Table 4. Functional Description of Test Register

LSBs or MSBs are selected by the state of D3 when writing to the Test Register. Red, green, blue data is selected by D0-D2. Only one bit of D0-D2 should be logical one for each read operation. When the MPU reads the test register, the 4 bits of color information from the DAC inputs are contained in the upper 4 bits, and lower 4 bits contain the enable information previously written. Note that either the CLK must be slowed down to the MPU cycle time, or the same pixel and overlay data must be presented to the device during the entire MPU read cycle.

DESIGNING WITH THE KDA0458

Board Layout

The KDA0458 is a high speed CMOS RAM DAC. CMOS device may draw large transient currents from the power supply. To supply the transient currents present in high speed video circuitry it is necessary for layout and decoupling circuitry to optimize. The optimum layout enables and KDA0458 to be located as close to the power supply connector and as close to the video output connector as possible.

Power and Ground Plane

The digital power plane powers all digital logic on the PCB, and the analog plane powers all KDA0458 power pins (V_{AA}) and reference circuitry. The digital power plane (V_{CC}) and analog power plane (V_{AA}) are connected through a ferrite bead (see Fig. 6). This ferrite should be located within 3 inches of the KDA0458. Ground plane should not be intersected each other. Connections to the ground plane should have very short lead lengths.

Power Supply Decoupling

Decoupling capacitors should be applied liberally to the V_{AA} pins of KDA0458. For the decoupling capacitor between the power line and ground line, a 0.1μF ceramic capacitor is used in parallel with a 0.01μF chip capacitor (for high frequency power supply noise rejection). The 33μF capacitor is for low frequency power supply ripple rejection. The lead lengths of the capacitors should be minimized.

Device Decoupling

To reduce the lead inductance, all capacitors are should be located as close to the device as possible. Chip capacitors are recommended for minimum lead inductance. The COMP pin must be decoupled to V_{AA}, typically using a 0.1μF ceramic capacitor. Low frequency supply noise will require a larger value. If the ghosting phenomenon is displayed, additional capacitance in parallel with the 0.1μF capacitor may help to fix the problem. The pixel clock should have the shortest possible traces. Longer traces can produce undesirable effects such as overshoot, undershoot, and ringing.

Digital Input Termination

Most noise on the analog outputs will be caused by excessive edge speeds, overshoot, undershoot, and ringing on the digital inputs. The PCB line between the TTL driver (which drive KDA0458) and the input to the KDA0458 have a low impedance source and are terminated with a high impedance. They behave like low impedance transmission lines, so signal transitions will be reflected from the high impedance input of the KDA0458. Transmission line mismatch will exist if the line length reflection time is greater than $1/4$ the signal edge time, resulting in ringing, overshoot, and undershoot that can generate noise onto the analog outputs. To reduce ringing, overshoot and undershoot caused by transmission line mismatch, either line length should be shortened or the line termination method should be used. The line termination method includes serial and parallel terminations. The recommended technique is to use serial termination. Serial termination is achieved by installing a resistor of about 50Ω between the TTL driver output and the KDA0458 digital input.

Analog Output

The line between DAC output and monitor R, G and B inputs should be regarded as a transmission line. As it is, it also causes problems of transmission line mismatch. As a solution to these problems, the double-termination method is used. By using this, both ends of the transmission lines are matched, providing an ideal, non-reflective system.

To maximize high-frequency supply voltage rejection, the video output signals should overlay the device ground plane.

Reference Voltage Source

The three DACs of the KDA0458 use a single external reference voltage and current-setting resistor to determine analog output levels. Noise and other signals on the V_{REF} input will be amplified and added to the outputs of the DACs. To degrade the noise effects of V_{REF} input, it is important that the applied reference voltage be as stable as possible. The preferred method is to generate the reference with a 1.2V bandgap reference voltage source.

Pixel Clock Generation

The pixel clock, CLK and $\overline{CLK}$, is a differential clock input that is designed to be driven by ECL circuitry powered from V_{AA} and GND. The CLK and $\overline{CLK}$ inputs should be terminated as close to the KDA0458 as possible with $220\Omega/330\Omega$ resistor pairs. $\overline{LD}$ is typically generated by dividing the clock frequency by 4 (4:1 multiplexing) or 5 (5:1 multiplexing) and it is translated to TTL levels. Any propagation delay in $\overline{LD}$ caused by the divider circuitry will not affect device performance. $\overline{LD}$ may be used as the shift clock for the video DRAMs. The Bt438 clock generator (from Brooktree) is recommended. It supports both 4:1 and 5:1 multiplexing (see Fig. 5)

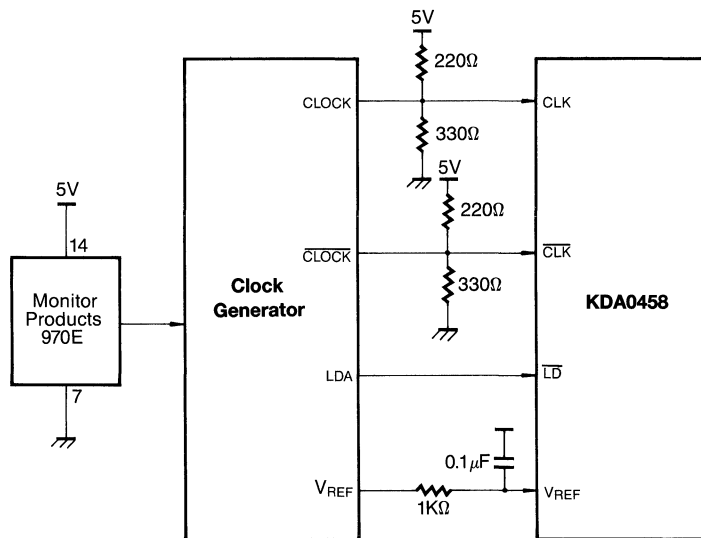


Fig. 5. Generating the KDA0458 Clock Signals

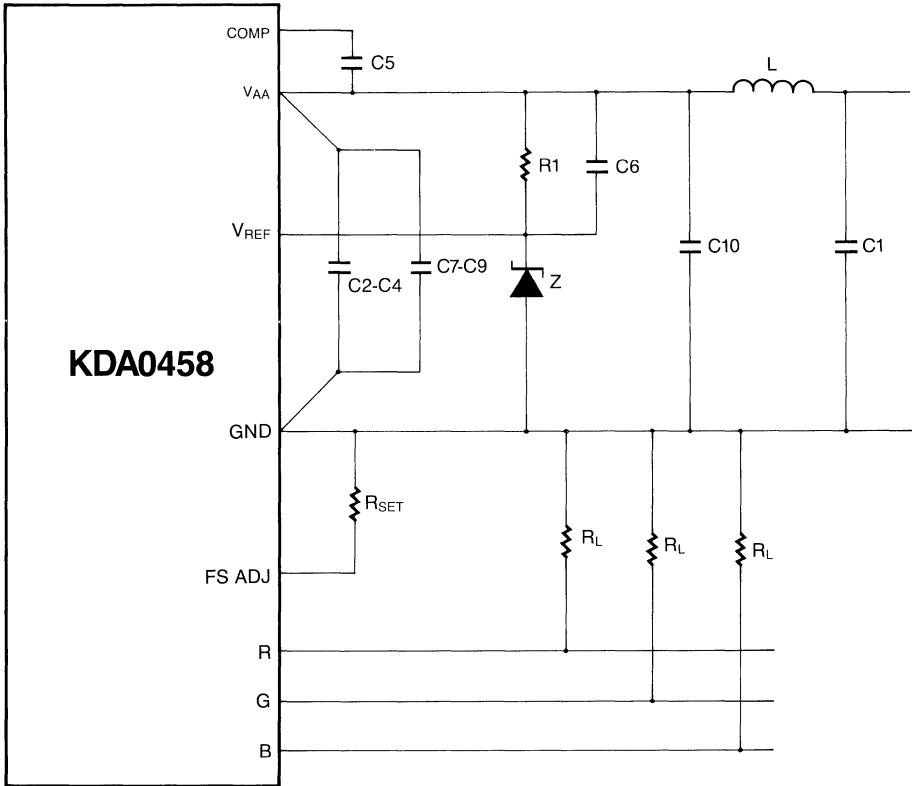


Fig. 6. Typical Connection Diagram

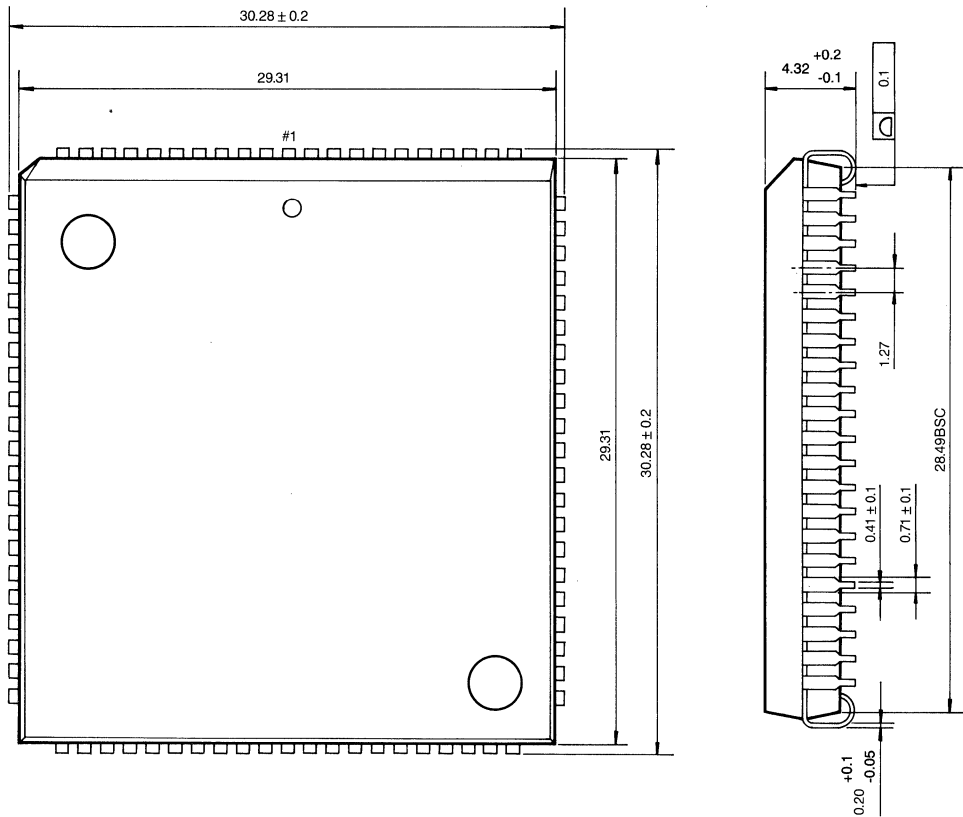
Location	Description	Vendor Part Number
C1-C6	0.1 μ F Ceramic Capacitor	Erie RPE 112Z5U104M50V
C7-C9	0.01 μ F Ceramic Capacitor	AVX 12102T 103 DA1018
C10	33 μ F Tantalum Capacitor	Mallory CSR 13F336KM
Z	1.2V Voltage Reference	National Semiconductor LM385Z-1-2
L	Ferrite Bead	Fair-Rite 2743001111
R	75 Ω 1% Metal Film Resistor	Dale CMF-55C
R1	1K Ω 1% Metal Film Resistor	Dale CMF-55C
RSET	523 Ω 1% Metal Film Resistor	Dale CMF-55C

Table5. External Voltage Reference Part List

PACKAGE DIMENSIONS

84-PLCC-SQ

Unit : mm



Description

KDA0471/0476/0478 support Personal System/2® compatible color graphic applications. The KDA0471/0478 come in a 44-pin PLCC package. The KDA0476 come in 32,44-pin PLCC and 28-pin DIP package. KDA0471 consists of color palette RAMs of 256×18 bits, overlay registers of 15×18 bit and triple 6-bit DACs. KDA0476 consists of color palette RAMs of 256×18 bits and triple 6-bit DACs. KDA0478 consists of color palette RAMs of 256×24 bit, overlay registers of 15×24 bit and triple 8-bit DACs. Fifteen overlay registers support overlaying cursors, grids, menus, and EGA emulation. KDA0471/0478 support generation of sync signal on all three channels, and programmable pedestal (0 or 7.5 IRE). The KDA0471/0476/0478 generate RS-343A compatible video outputs capable of directly driving a doubly-terminated 75 Ohms load, and RS-170 compatible video outputs capable of directly driving singly-terminated 75 Ohms load without the need for external buffers.

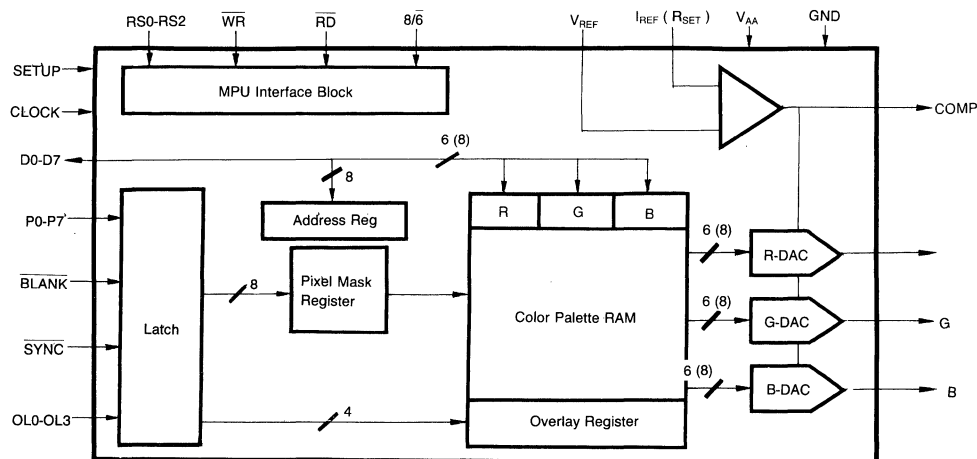
Features

- Personal System/2® compatible.
- Snow-free display.
- 50, 66, 80, 100 and 120MHz operation.
- Triple 6/8 bit high performance DAC.
- $256 \times 18/24$ color palette SRAM.
- $15 \times 18/24$ overlay palette SRAM (KDA0471/0478).
- RS-343/RS-170 compatible outputs.
- Standard MPU interface.
- External voltage or current reference.
- Single +5V power supply.
- 44-pin PLCC, 32-pin PLCC or 28-pin DIP Package

Ordering Information

Marking Spec	Speed	Package	Remark
KDA0476BCN-50/66/80	50/66/80MHz	28DIP	Only I_{REF} Mode
KDA0476BPJ-50/66/80	50/66/80MHz	32PLCC	Only I_{REF} Mode
KDA0476BPL-50/66/80	50/66/80MHz	44PLCC	I_{REF} Mode
KDA0476BPL-50/66/80	50/66/80MHz	44PLCC	V_{REF} Mode
KDA0471BPL-50/66/80/100/120V	50/66/80MHz	44PLCC	I_{REF} Mode
KDA0471BPL-50V/66V/80V	50/66/80MHz	44PLCC	V_{REF} Mode
KDA0478BPL-50/66/80/100/120V	50/66/80/100/120MHz	44PLCC	I_{REF} Mode
KDA0478BPL-50V/66V/80V/100V/120V	50/66/80/100/120MHz	44PLCC	V_{REF} Mode

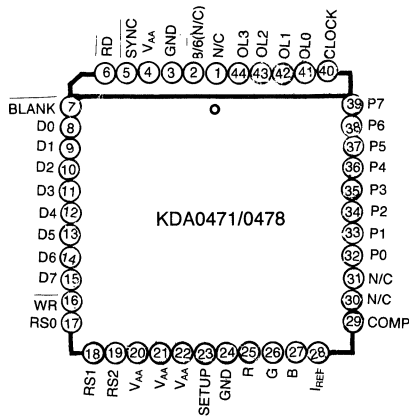
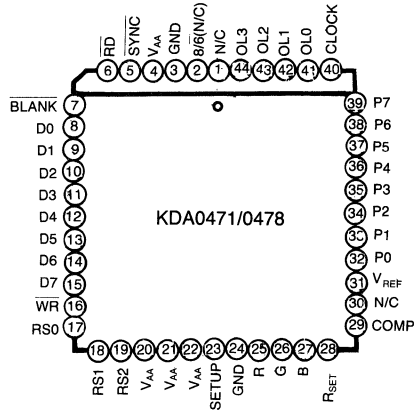
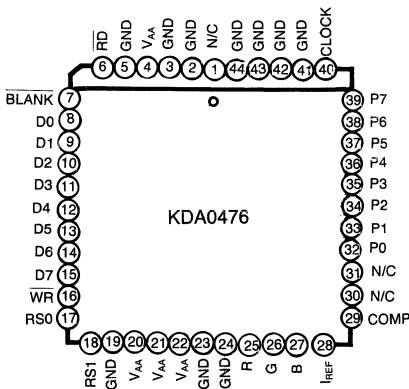
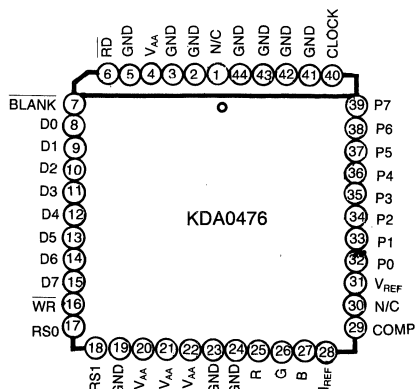
Block Diagram



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() for the V_{REF} Mode

Pin Configurations

44-Pin Plastic J-Lead (PLCC)

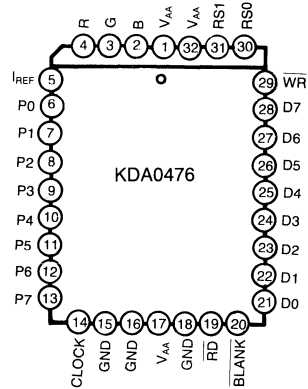
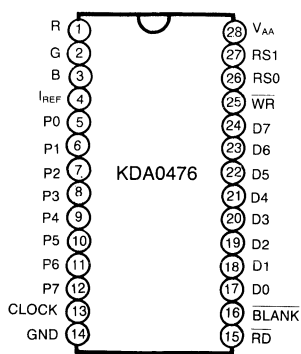
 I_{REF} Mode V_{REF} Mode I_{REF} Mode V_{REF} Mode

Notes:

1. N/C pins may be left unconnected without affecting the performance of the KDA0471/0476/0478.
2. () for the KDA0471.

28-Pin DIP

32-Pin Plastic J-Lead (PLCC)



Electrical Specifications**Absolute Maximum Ratings**

Characteristics	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	V_{AA}			7.0	V
Voltage on Any Digital Pin		GND-0.5		$V_{AA} + 0.5$	V
Analog Output Short Circuit Duration to any Power Supply or Common	I_{sc}		Indefinite		
Operating Temperature (ambient)	T_o	- 55		+ 125	°C
Storage Temperature	T_{stg}	- 65		+ 150	°C
Junction Temperature	T_J			+ 150	°C
Soldering Temperature (5 seconds, 1/4" from pin)	T_{sol}			260	°C
Vapor Phase Soldering (1 minute)	T_{vsol}			220	°C

Note: 1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions.

2. Functional operation under any of these conditions is not implied.

3. Applied voltage must be current limited to specified range.

4. Current is specified as positive when flowing into the device.

Recommended Operating Conditions

Characteristics	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	V_{AA}				
50MHz parts		4.50	5.00	5.50	V
66,80MHz parts		4.75	5.00	5.25	V
Operating Temperature (ambient)	T_o	0		+ 70	°C
Output Load (effective)	R_L		37.5		Ω
Reference Voltage	V_{REF}	1.14	1.235	1.26	V
I_{REF} current	I_{REF}				
RS-343A standard		- 3	- 8.39	- 10	mA
PS/2 compatible		- 3	- 8.88	- 10	mA

DC Characteristics

Characteristics	Symbol	Min	Typ	Max	Units
DAC Resolution: KDA0478		8	8	8	Bits
KDA0471/0476		6	6	6	Bits
DCA Accuracy					
Integral Linearity Error : KDA0478	IL			± 1	LSB
KDA0476				± 1/2	LSB
KDA0471				± 1/4	LSB
Differential Linearity Error : KDA0478	DL			± 1	LSB
KDA0476				± 1/2	LSB
KDA0471				± 1/4	LSB
Gray Scale Error				± 5	% Gray
Monotonicity			Guaranteed		
Coding					Binary
Digital Input High Voltage	V _{IH}	2.0		V _{AA} + 0.5	V
Digital Input Low Voltage	V _{IL}	GND-0.5		0.8	V
Digital Input High Current (V _{in} = 2.4V)	I _{IH}			1	μA
Digital Input Low Current (V _{in} = 0.4V)	I _{IL}			-1	μA
Digital Input Capacitance (f = 1MHz, V _{in} = 2.4V)	C _{IN}			7	pF
Digital Output High Voltage (I _{oh} = -400μA)	V _{OH}	2.4			V
Digital Output Low Voltage (I _{ol} = 3.2mA)	V _{OL}			0.4	V
Digital Three-State Current	I _{OZ}			50	μA
Digital Output Capacitance	C _{DO}			7	pF
Analog Outputs					
Gray Scale Current Range				20	mA
Output Current (RS-343A Standard)			17.62		mA
White Level relative to Black*					
Black Level relative to Blank					
KDA0471/0478: Setup = V _{AA}		0.95	1.44	1.90	mA
Setup = GND		0	5	50	μA
KDA0476		0	0	0	μA
Blank Level: KDA0471/0478		6.29	7.62	8.96	mA
KDA0476		0	5	50	μA
Sync Level (KDA0471/0478 Only)		0	5	50	μA
LSB: KDA0478			69.1		μA
KDA0471/0476			279.68		μA
DAC to DAC Matching			2	5	%
Output Impadence	R _{AO}		10		KΩ
Output Capacitance (f = 1MHz, I _{OUT} = 0mA)	C _{AO}			30	pF
Output Compliance	V _{OC}	-1.0		+1.5	V
Voltage Reference Input Current	I _{VREF}		10		μA
Power Supply Rejection Ratio (f = 1KHz, COMP = 0.1μF)	PSRR		0.5		%/%ΔV _{AA}

Test conditions to generate RS-343A standard video signals (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with R_{SET} = 147Ω, V_{REF} = 1.235V, SETUP = V_{AA}, 8/6 = logical 1. For 28-pin DIP version of the KDA0476, I_{REF} = -8.39mA.

As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

* Since the KDA0471/0476 have 6-bit DACs (and the KDA0478 in the 6-bit mode), the output levels are approximately 1.5% lower than these values.

Analog Output Levels—PS/2 Compatibility

Characteristics	Symbol	Min	Typ	Max	Units
Analog Output Current					
White Level relative to Black		18.00	18.65	20.00	mA
Black Level relative to Black					
KDA0471/0478: Setup = V_{AA}		1.01	1.51	2.0	mA
: Setup = GND		0	5	50	μA
KDA0476		0	5	50	μA
Blank Level: KDA0471/0478		6.6	8	9.4	mA
:KDA0476		0	5	50	mA
Sync Level (KDA0471/0478 Only)		0	5	50	μA

Test conditions to generate PS/2 compatible video signals (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with $R_{SET} = 140\Omega$, $V_{REF} = 1.235V$, $SETUP = A_{AA}$, 8/6 = logical 1. For 28-pin DIP version of the KDA0476, $I_{REF} = -8.88mA$.

AC Characteristics

Parameters	Symbols	50MHz			66MHz			80MHz			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Clock Rate	F _{max}			50			60			80	MHz
RS0-RS2 Setup Time	T _{srs}	10			10			10			ns
RS0-RS2 Hold Time	T _{hrs}	10			10			10			ns
RD Asserted to Data Bus driven	T _{dr}	5			5			5			ns
RD Asserted to Data Valid	T _{va}			40			40			40	ns
RD Negated to Data Bus 3-States	T _{3st}			20			20			20	ns
Read Data Hold Time	T _{hrd}	5			5			5			ns
Write Data Setup Time	T _{swd}	10			10			10			ns
Write Data Hold Time	T _{hwd}	10			10			10			ns
RD, WR Pulse Width Low	T _{pwl}	50			50			50			ns
RD, WR Pulse Width High	T _{pwh}	6*T _{clk}			6*T _{clk}			6*T _{clk}			ns
Pixel and Control Setup Time	T _{spx}	3			3			3			ns
Pixel and Control Hold Time	T _{hpx}	3			3			3			ns
Clock Cycle Time (T _{CLK})	T _{clk}	20			15.15			12.5			ns
Clock Pulse Width High Time	T _{ckh}	6			5			4			ns
Clock Pulse Width Low Time	T _{ckl}	6			5			4			ns
Analog Output Delay	T _d			30			30			30	ns
Analog Output Rise/Fall Time	T _r /T _f		3			3			3		ns
Analog Output Settling Time*	T _{set}		20			13			13		ns
Clock and Data Feedthrough*	FDTHR		-30			-30			-30		dB
Glitch Impluse*	GI		75			75			75		pV-sec
DAC to DAC crosstalk	XTAK		-23			-23			-23		dB
Analog Output Skew	T _{skw}			2			2			2	ns
Pipeline Delay	T _{dp}	4	4	4	4	4	4	4	4	4	Clocks
V _{AA} Supply Current**	I _{AA}		180	220		180	220		180	220	mA

Note:

Recommended Operating Conditions using external voltage reference with $R_{SET} = 147\Omega$, $V_{REF} = 1.235V$, $SETUP = V_{AA}$, $8/6 = \text{logical 1}$. For 28-pin DIP (KDA0476), $I_{REF} = -8.39mA$ and TTL input value are 0 to 3 volts with input rise/fall times $\leq 3ns$ (measured between 10% and 90% points). The timing reference point at 50% for inputs and outputs. Analog output load $\leq 10pF$, D0-D7 output load $\leq 50pF$. (Refere to timing chart-Figure 2)

* Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a $1K\Omega$ resistor to ground and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impluse includes clock and data feedthrough, $-3dB$ test bandwidth $= 2 \times \text{clock rate}$.

** At F_{max} I_{AA} (Typ) at V_{AA} = 5.0V. I_{AA} (Max) at V_{AA} (Max).

AC Characteristics

Parameters	Symbols	100MHz			120MHz			Units
		Min	Typ	Max	Min	Typ	Max	
Clock Rate	Famx			50			60	MHz
RS0-RS2 Setup Time	Tsrs	10			10			ns
RS0-RS2 Hold Time	Thrs	10			10			ns
RD Asserted to Data Bus driven	Tdr	5			5			ns
RD Asserted to Data Valid	Tva			40			40	ns
RD Negated to Data Bus 3-States	T _{3st}			20			20	ns
Read Data Hold Time	Thrd	5			5			ns
Write Data Setup Time	Tswd	10			10			ns
Write Data Hold Time	Thwd	10			10			ns
RD, WR Pulse Width Low	Twpl	50			50			ns
RD, WR Pulse Width High	Twph	6*Tclk			6*Tclk			ns
Pixel and Control Setup time	Tspx	3			3			ns
Pixel and Control Hold Time	Thpx	3			3			ns
Clock Cycle Time (T _{CLK})	Tclk	10			8.33			ns
Clock Pulse Width High Time	Tckh	6			5			ns
Clock Pulse Width Low Time	Tckl	6			5			ns
Analog Output Delay	Td			30			30	ns
Analog Output Rise/Fall Time	Tr/Tf		3			3		ns
Analog Output Setting Time*	Tset		20			13		ns
Clock and Data Feedthrough*	FDTHR		-30			-30		dB
Glitch Impulse*	GI		75			75		pV-sec
DAC to DAC crosstalk	XTAK		-23			-23		dB
Analog Output Skew	Tskw			2			2	ns
Pipeline Delay	Tdp	4	4	4	4	4	4	Clocks
V _{AA} Supply Current**	I _{AA}		180	220		180	220	mA

Note:

Recommended Operating Conditions using external voltage reference with $R_{SET} = 147\Omega$, $V_{REF} = 1.235V$, $SETUP = V_{AA}$, 8/6 = logical 1. For 28-pin DIP (KDA0476), $I_{REF} = -8.39mA$ and TTL input value are 0 to 3 volts with input rise/fall times $\leq 3ns$ (measured between 10% and 90% points). The timing reference point at 50% for inputs and outputs. Analog output load $\leq 10pF$, D0-D7 output load $\leq 50pF$. (Refers to timing chart-Figure 2)

* Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a $1K\Omega$ resistor to ground and are driven by 74HC logic. Setting time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, -3dB test bandwidth = $2 \times$ clock rate.

** At F_{max} I_{AA} (Typ) at $V_{AA} = 5.0V$. I_{AA} (Max) at V_{AA} (Max).

Timing Waforms

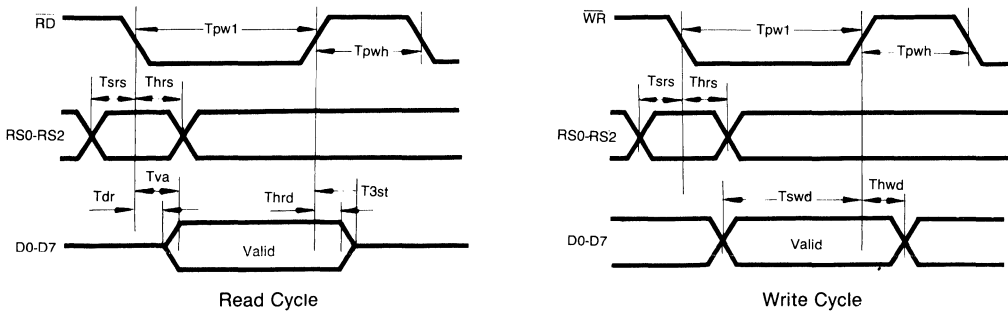


Figure 1. MPU Read/Write Timing

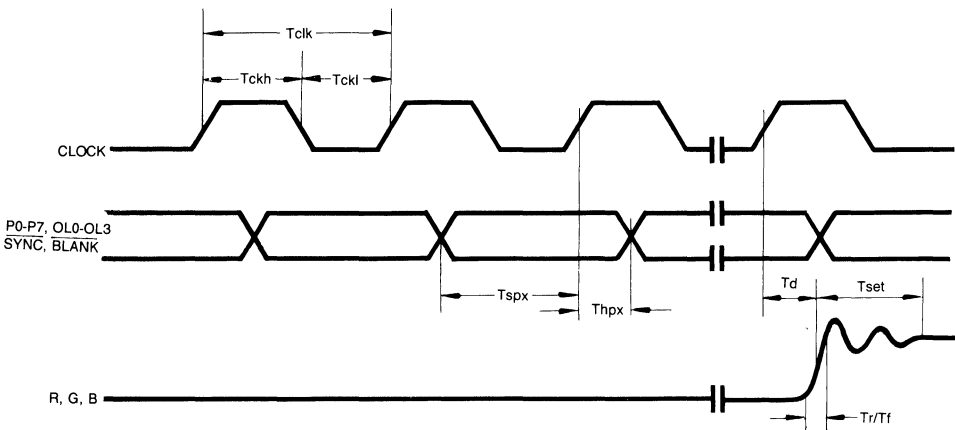


Figure 2. Video Timing Diagram

- Note 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full scale transition.
- Note 2: Settling time measured from the 50% point of full scale transition to the output remaining within ± 1 LSB (KDA0478), $\pm 1/4$ LSB (KDA0471), or $\pm 1/2$ LSB (KDA0476).
- Note 3: Output rise/fall time measured between the 10% and 90% points of full scale transition.

Pin Description

Section	Symbol	Signal Name	I/O	Description
MPU Interface	RS0-RS2	Register Select	I	These inputs are used to specify the internal register to be accessed, as shown in Table 2. These inputs are latched at the falling edge of the $\overline{RD}$ or $\overline{WR}$ signals.
	$\overline{RD}$, $\overline{WR}$	Read enable, Write enable	I	$\overline{RD}$ and $\overline{WR}$ signals control the timing of the MPU Read and Write operations respectively. The D0-D7 and RS0-R2 are latched on the rising and falling edges of the signal respectively. $\overline{RD}$ and $\overline{WR}$ should not be asserted simultaneously.
	D0-D7	Data Bus	I/O	MPU data is transferred between 8 bit data bus and internal register under control of $\overline{RD}$ or $\overline{WR}$ signal.
	8/ $\overline{6}$	6-bit/8-bit DAC Select	I	With logical 1 on this input, the MPU performs 8-bit operations and D7 is the MSB. With logical 0 on this input the MPU performs 6-bit operations and D5 is the MSB.
Pixel Interface	CLOCK	Pixel Clock	I	P0-P7, OL0-OL3, SYNC and BLANK inputs are latched on the rising edge of the clock. The input should be driven by a TTL buffer.
	P0-P7	Pixel Address	I	These inputs specify one of the 256 color data entries in the color palette RAM to be used for color information. Unused pins should be connected to GND.
	OL0-OL3	Overlay Select	I	These inputs specify one of the 15 overlay palette. When an overlay register is accessed, P0-P7 are ignored. Unused pins should be connected to GND.
	SETUP	Setup Control	I	This pin control 7.5IRE or 0IRE blanking pedestal when SETUP is logic 1 or 0. This pin should not be in the floating condition.
	BLANK	Composite Blank Control	I	When logical 0 is input on this pin, the outputs of the DACs are driven to blanking level, regardless of concurrent P0-P7 or OL0-OL3 values.
	SYNC	Composite Sync Control	I	When logical 0 is input on this pin, the current source 40 IRE in the DAC is switched off. When logical 1 is input, current as high as 40 IRE is added to the DAC output. The SYNC does not override any other control or data input, so it must be activated only during the blanking interval. If sync information is not needed in the analog output this input should be connected to GND.

Section	Symbol	Signal Name	I/O	Description
Analog Interface	R, G, B	Red, Green, Blue Current Output	O	R, G and B are respectively the analog currents output of 3 DACs. These high impedance current source are capable of directly driving a doubly-terminated 75Ω coaxial cable. (See Figures 5, 6 and 7)
	COMP	Compensation		When using the KDA0471/0476/0478 of I _{REF} mode, this pin should be connected to the I _{REF} pin. When using the KDA0471/0476/0478 of V _{REF} mode, this pin should be connected to the V _{AA} , through the bypass capacitor.
	V _{REF}	Voltage Reference	I	In the KDA0471/0476/0478 of V _{REF} mode, the pin should be supplied with 1.2V reference voltage. A bypass capacitor of 0.1μF with shortest possible lead lengths should be connected between this pin and the V _{AA} . (See the figures 7)
	I _{REF} (R _{SET})	Full Scale Adjust Control	I	This setting will not change the I_{REF} relationship shown in Figure 3 and 4. When using the KDA0471/0476/0478 of V_{REF} mode, this input should be connected to GND through the R_{SET}. The magnitude of the full scale video outputs is controlled by the R_{SET} Resistor. The relationship between the R_{SET} and full scale output current on each output is given by: $R_{SET} = \frac{K \times 1000 \times V_{REF}}{I_{OUT}}$ (R_{SET} in Ohms, recommended 147Ω, V_{REF} in Volts, and I_{OUT} in mA) When using the KDA0471/0476/0478 of I_{REF} mode, the relationship between I_{REF} and the full scale output current on each output is: $I_{REF} = \frac{I_{OUT}}{K} \text{ (I}_{OUT} \text{ in mA)}$ Constant K is listed on Table 1 for 37.5Ω loads.
Power Supply	V _{AA}	Analog Power		
	GND	Ground		

Part		Pedestal	K (With sync)	K (Without sync)
KDA0478	6-bit Mode	7.5 IRE 0 IRE	3.170 3.000	2.26 2.10
	8-bit Mode	7.5 IRE 0 IRE	3.195 3.025	2.28 2.12
KDA0471		7.5 IRE 0 IRE	3.170 3.000	2.26 2.10
KDA0476		0 IRE	3.000	2.10

Table 1. Constant K for 37.5Ω Loads

Device Description

KDA0471/0476 Data Bus

Internal data bus is 6-bits and the lower 6-bits of the 8 bit input bus contain the color data. In this case, D0 is the LSB and D5 is the MSB of the color data. D6 and D7 are ignored during write cycle and they are zero during read cycle.

KDA0478 Data Bus

The function of the control input "8/6" on this device is to specify whether the MPU reads and writes 8 bits ($8/6$ = logical 0 of data in each cycle. For 8 bit operation, the data bit D0 is the LSB and the data bit D7 is the MSB of the color data. In case of 6 bit operation, lower 6 bits contain color data with D0 being the LSB and D5 being the MSB as stated before. D6 and D7 are ignored while writing the data. During read cycles, D6 and D7 are logical zero.

Microprocessor Interface

The KDA0471/0476/0478 support standard MPU interfaces which allows a microprocessor to access the color palette RAM and overlay registers. Microprocessor can access the address register, color palette RAM, overlay registers or read mask register and the selection is done by the RS0-RS2 input shown in Table 2. The address register is used to address the color palette RAM and overlay registers, without requiring any external address multiplexers. The data bit D0 is the LSB and it corresponds to the address bit ADDR0.

RS2	RS1	RS0	Register Name
0	0	0	Address Register (SRAM Write Mode)
0	1	1	Address Register (SRAM Read Mode)
0	0	1	Color Palette RAM
0	1	0	Pixel Read Mask Register
1	0	0	Address Register (Overlay Write Mode)
1	1	1	Address Register (Overlay Read Mode)
1	0	1	Overlay Register
1	1	0	Reserved

Table 2. Register select input truth table

Writing to the color palette RAM

For writing data into the color palette RAM, the MPU must first write the address of the color palette RAM location to be modified into the Write-mode address register. The MPU will have to perform three successive write cycles each, one for red, green and blue color information are combined internally to make a 24-bit word (18-bit word in case of KDA0471/0476) and written to the RAM location given by the address register. The address register is auto-incremented to the next location. This allows consecutive update of the color palette RAM locations, for which the MPU can continue supplying sequences of red, green and blue data until the entire block has been written.

Reading from the color palette RAM

For reading data from the color palette RAM, the MPU must first writes the address of the color palette RAM location, which is to be read into the Read-mode address register. The color contents from this location are copied into the RGB registers and the address register is auto-incremented to the next location. The MPU will have to perform three successive read cycles each for red, green and blue color, using RS0-RS2 to select the color palette RAM. After the last (blue) read cycle, the contents of the specified color palette location are copied into the RGB registers and address register is once more auto-incremented. This allows reading consecutive locations of the color palette. In this way, the MPU continues to perform red, green and blue read cycles until the entire block has been read.

Writing on the Overlay Register

For writing data into overlay registers, the MPU must first write the address of the overlay register location to be modified into the Write-mode address register. The MPU will have to perform three successive write cycles each, one for red, green and blue color, using RS0-RS2 to select overlay register. After the last (blue) write cycle, all three bytes of color information are combined internally to make a 24-bit word (18-bit word in case of KDA0471/0476) and written to the overlay register location given by the address register. The address register is auto-incremented to the next location. This allows consecutive update of the overlay registers, for which the MPU can continue supplying sequences of red, green and blue data until the entire block has been written.

Reading from the Overlay Register

For reading data from the overlay registers, the MPU must first write the address of the overlay register location, which is to be read into the Read-mode address register. The color contents from this location are copied into the RGB registers and the address register is auto-incremented to the next location. The MPU will have to perform three successive read cycles each for red, green and blue color, using RS0-RS2 to select overlay registers. After the last (blue) read cycle, the contents of the specified overlay register location are copied into the RGB registers and address register is once more autoincremented. This allows reading consecutive locations of the overlay registers. In this way, the MPU continues to perform red, green and blue read cycles until the entire block has been read.

Address Register

The address register has two additional bits (a0, a1). The bits a0 and a1 repeatedly count 00, 01 and 10, maintaining the sequence of Red, Green and Blue Read/Write cycles.

The MPU can access the eight bits AD0-AD7 which are used to address the color palette RAM and overlay register as shown in Table 2. The MPU can read the address register at any time without modifying its contents or modifying the read/write mode.

when the overlay register is accessed, the 4 MSB (AD4-AD7) of the Address Register are ignored, and only the 4 LSB (AD0-AD3) are used to address the overlay register.

Address Register		RS2 RS1 RS0	Addressed by MPU
a0 a1	AD0-AD7		
0 0			Red Data
0 1			Green Data
1 0			Blue Data
	00h-FFh	0 0 1	Color Palette RAM
	x0h	1 0 1	Reserved
	x1h-xFh	1 0 1	Overlay Register

Table 3. Address Register Operation

OL0-OL3	P0-P7	Addressed by Frame Buffer
0h	0 0 h	Color Palette Location 00h
0h	0 1 h	Color Palette Location 01h
•	•	•
•	•	•
0h	F F h	Color Palette Location FFh
1h	x x h	Overlay Color 1
•	•	•
•	•	•
Fh	x x h	Overlay Color 15

Table 4. Pixel and Overlay Control Truth Table

Graphics Controller Interface

On this interface, the pixel inputs P0-P7 and overlay inputs OL0-OL3 are used to address the color palette RAM and overlay registers as shown in Table 4. These inputs are update from the graphics controller as shown in the application example. Also, BLANK and SYNC signals are provided by the VGA controller. The data bit D0 of the pixel read mask register corresponds to pixel input P0 the color palette RAM location addressed by the pixel inputs, provides 24 bits of color information to three DACs. In the case of the KDA0471/0476, these are 18 bits.

As illustrated in Figures 1 and 2, the SYNC and BLANK inputs are latched on the rising edge of the CLOCK to:

1. Keep synchronization with the color data
2. Add weighted currents to the analog outputs and
3. Generate specific output level for video applications.

Modifications of the output levels by these signals are shown in Tables 5 and 6.

The SETUP input specifies whether 0 IRE or 7.5 IRE blanking pedestal is used.

SETUP = GND for 0 IRE

SETUP = V_{AA} for 7.5 IRE

The analog outputs of all three devices are capable of directly driving a 37.5Ω load without any buffering.

ITEM	KDA0471/0478 I_{OUT} (mA)	SYNC	BLANK	DAC Input Data
WHITE	26.67	1	1	FFh
DATA	Data + 9.05	1	1	Data
DATA-SYNC	Data + 1.44	0	1	Data
BLACK	9.05	1	1	00h
BLACK-SYNC	1.44	0	1	00h
BLANK	7.62	1	0	xxh
SYNC	0	0	0	xxh

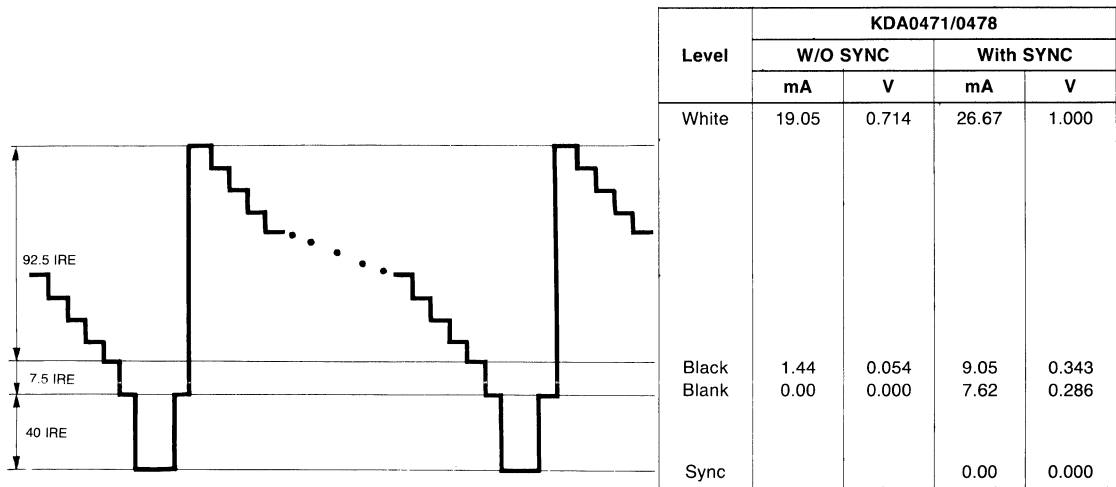
Note: Doubly-terminated load of 75Ω , SETUP = V_{AA} , $V_{REF} = 1.235V$, $R_{SET} = 147\Omega$

Table 5. Video Output Truth Table (SETUP = V_{AA})

ITEM	KDA0476 I_{OUT} (mA)	KDA0471/0478 I_{OUT} (mA)	SYNC	BLANK	DAC Input Data
WHITE	17.62	25.24	1	1	FFh
DATA	Data	Data + 7.62	1	1	Data
DATA-SYNC	Data	Data	0	1	Data
BLACK	0	7.62	1	1	00h
BLACK-SYNC	0	0	0	1	00h
BLANK	0	7.62	1	0	xxh
SYNC	0	0	0	0	xxh

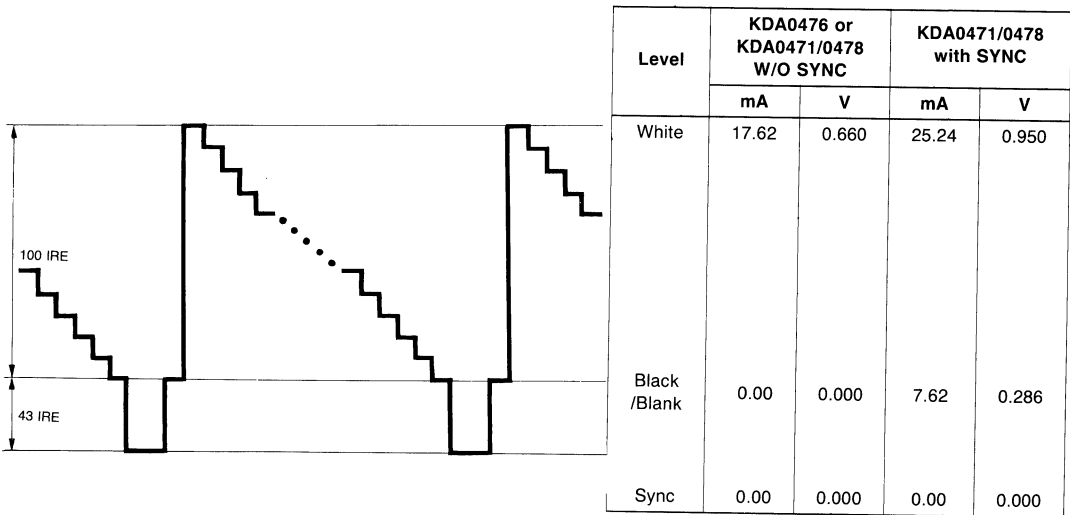
Note: Doubly-terminated load of 75Ω , SETUP = GND, $V_{REF} = 1.235V$, $R_{SET} = 147\Omega$

Table 6. Video Output Truth Table (SETUP = GND)



Note: 75Ω doubly-terminated load, SETUP = V_{AA}, V_{REF} = 1.235V, R_{SET} = 147Ω
RS-343A levels and tolerances assumed on all levels.

Figure 3. Composite Video Output Waveforms (SETUP = V_{AA})



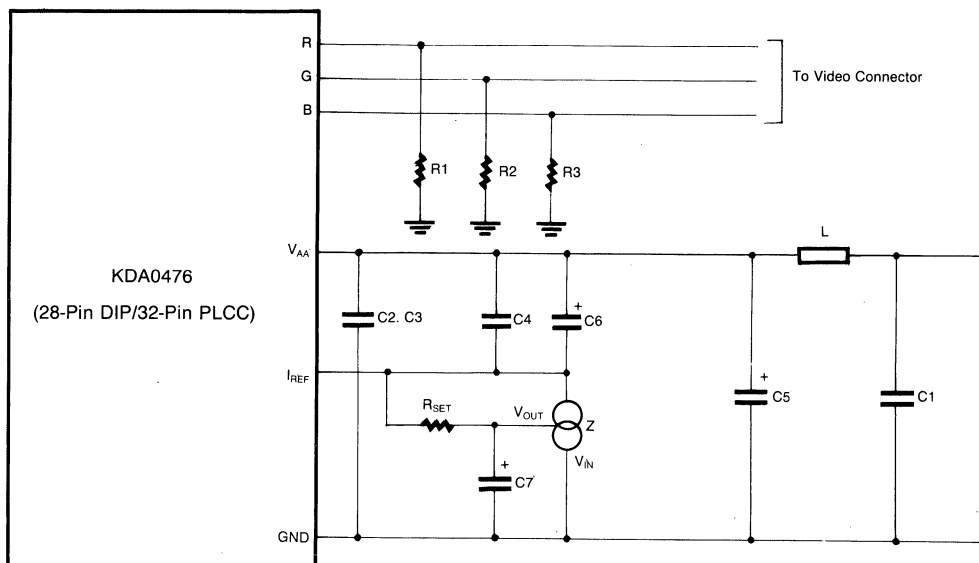
Note: 75Ω doubly-terminated load, SETUP = GND, V_{REF} = 1.235V, R_{SET} = 147Ω
RS-343A levels and tolerances assumed on all levels.

Figure 4. Composite Video Output Waveforms (SETUP = GND)

PC Board Layout Considerations

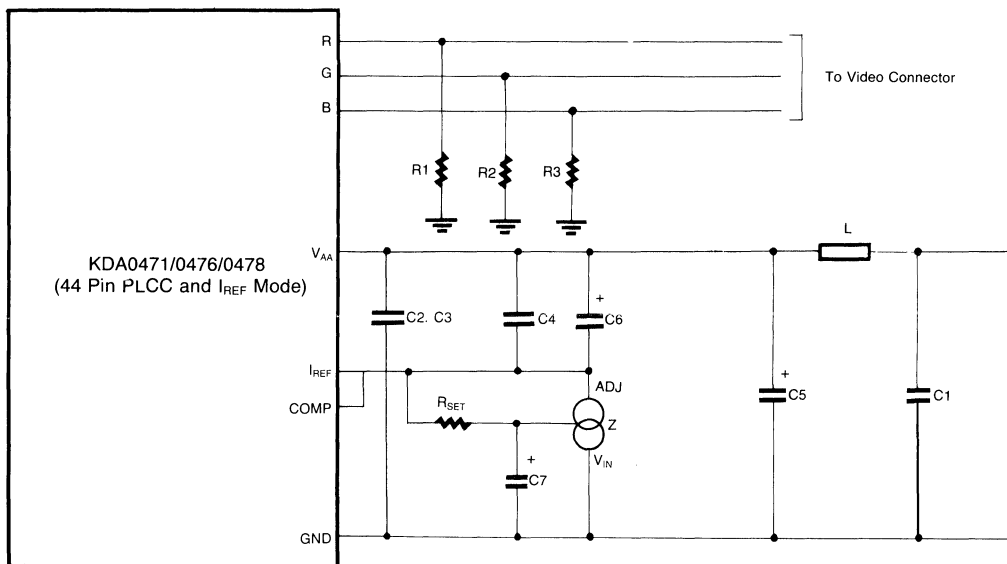
To minimize noise on the power lines and ground lines, the digital inputs require to be shielded and decoupled. For the decoupling capacitor between the power line and ground line, a $0.1\mu\text{F}$ ceramic capacitor is used in parallel with a $10\mu\text{F}$ tantalum capacitor. The digital power plane (V_{CC}) and analog power plane (V_{AA}) are connected through a ferrite bead. (refer to Figure 5, 6 and 7) This ferrite bead should be located within 3 inches of the KDA0471/0476/0478. The analog power plane supplies power to KDA471/0476/0478 of the analog output pins and related devices. (refer to Figure 5, 6 and 7) The PCB line between the TTL driver (which drive KDA0471/0476/0478) and the input to the KDA0471/0476/0478 have a low impedance source and are terminated with a high impedance. They behave like low impedance transmission lines, so signal transitions will be reflected from the high impedance input of the KDA0471/0476/0478. To reduce ringing caused by transmission line mismatch, either line length should be shortened or the line termination method should be used. The line termination method includes serial and parallel terminations. The recommended technique is to use serial termination. Serial termination is achieved by installing a resistor of about 50Ω between the TTL driver output and the KDA0471/0476/0478 digital input.

The line between DAC output and monitor R, G and B inputs should be regarded as a transmission line, too. As it is, it also causes problems of transmission line mismatch. As a solution to these problems, the double-termination method is used. By using this, both ends of the transmission lines are matched, providing an ideal, non-reflective system.



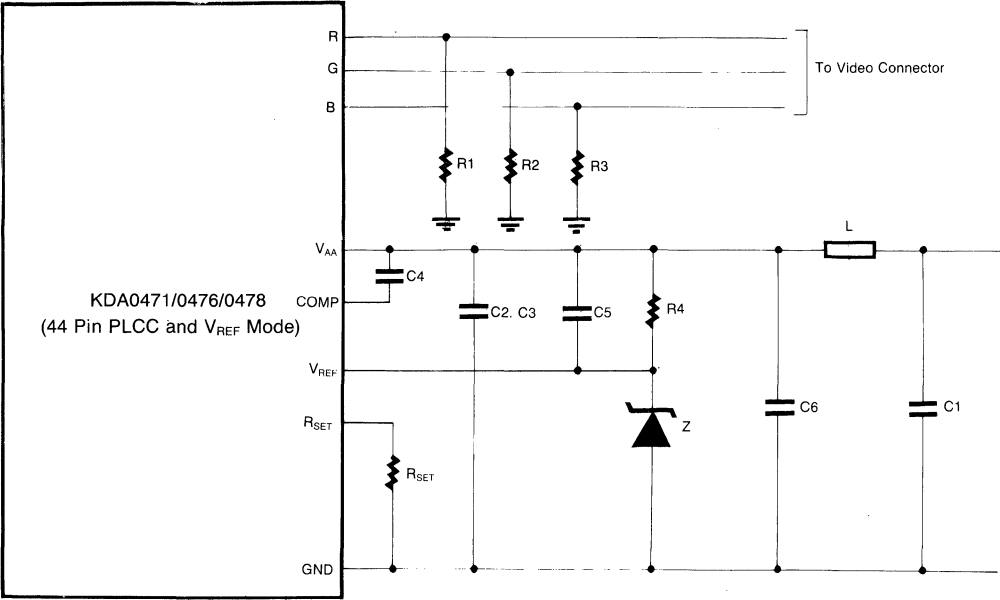
Location	Description
C1-C4	$0.1\mu\text{F}$ Ceramic Capacitor
C5	$10\mu\text{F}$ Capacitor
C6	$47\mu\text{F}$ Capacitor
C7	$1\mu\text{F}$ Capacitor
L	Ferrite Bead
Z	Adjustable Regulator (LM337-LZ)
R1, R2, R3	75Ω 1% Metal Film Resistor
RSET	1% Metal Film Resistor

Figure 5. External Current Reference Circuit



Location	Description
C1-C4	0.1 μ F Ceramic Capacitor
C5	10 μ F Capacitor
C6	47 μ F Capacitor
C7	1 μ F Capacitor
L	Ferrite Bead
Z	Adjustable Regulator (LM337-LZ)
R1, R2, R3	75 Ω 1% Metal Film Resistor
R _{SET}	1% Metal Film Resistor

Figure 6. External Current Reference Circuit



Location	Description
C1-C5	0.1 μ F Ceramic Capacitor
C6	10 μ F Capacitor
L	Ferrite Bead
Z	Voltage Reference (LM 385BZ-1.2)
R1, R2, R3	75 Ω 1% Metal Film Resistor
R4	1% Metal Film Resistor
R_{SET}	1% Metal Film Resistor

Figure 7. External Voltage Reference Circuit

HIGH-SPEED A/D-D/A CONVERTER (20MHz 8-bit A/D + 10-bit D/A)

The KSV3110 consists of high speed low glitch 10-bit DAC and high speed flash 8-bit ADC with the various auxiliary circuits (reference voltage source, pre buffer amp, input clamp circuit and feed-in output amp).

The KSV3110 is suitable for video application, capable of converting an analog signal with full power frequency components up to 6MHz into 8-bit digital signals.

All digital inputs and outputs are TTL compatible.

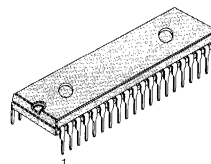
FEATURES

- 8-bit A/D + 10 bit D/A resolution
- TTL digital interface
- Internal input buffer amp
- Internal clamp circuit (Peak, Keyed)
- 20MSPS conversion rate
- Internal reference voltage (2V)
- Internal feed-in amp
- Few external components for application
- Easy and simple video application

APPLICATIONS

- Medical image processor
- Data acquisition systems
- Radar data conversion
- Video data conversion

40 DIP



BLOCK DIAGRAM

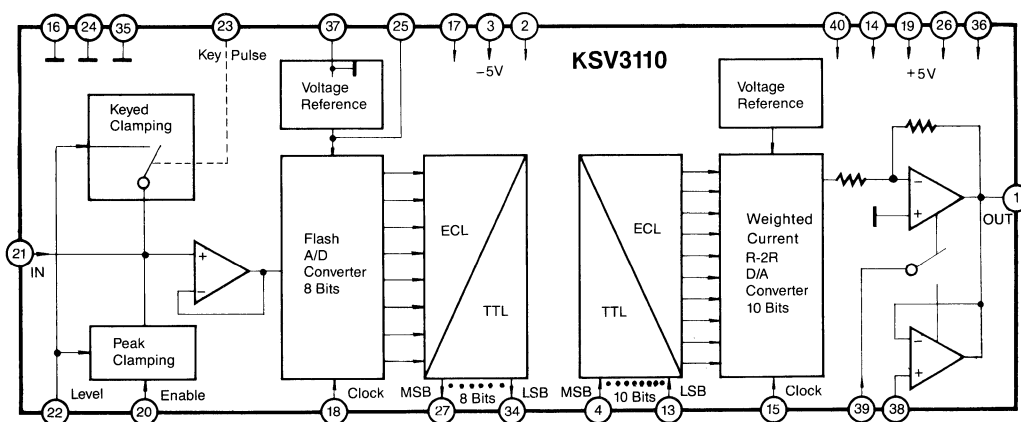


Fig. 1

PIN DESCRIPTION

Pin No.	Description	Pin No.	Description
1	Analog Output D/A Converter	21	Analog Input A/D Converter
2	-5V Supply D/A-Analog	22	Clamping Level Input
3	-5V Supply D/A Converter-Digital	23	Clamping Pulse Input
4	Digital Input Bit 9 (MSB)	24	Analog Ground A/D Converter
5	Digital Input Bit 8	25	Reference Voltage A/D Converter
6	Digital Input Bit 7	26	+5V Supply A/D Converter-Digital
7	Digital Input Bit 6	27	Digital Output Bit 7 (MSB)
8	Digital Input Bit 5	28	Digital Output Bit 6
9	Digital Input Bit 4	29	Digital Output Bit 5
10	Digital Input Bit 3	30	Digital Output Bit 4
11	Digital Input Bit 2	31	Digital Output Bit 3
12	Digital Input Bit 1	32	Digital Output Bit 2
13	Digital Input Bit 0 (LSB)	33	Digital Output Bit 1
14	+5V Supply D/A Converter-Analog-Digital	34	Digital Output Bit 0 (LSB)
15	Clock Input D/A Converter-Analog	35	Digital Ground A/D Converter
16	GND D/A Conv. & Clock A/D Converter	36	+5V Supply A/D Converter-Analog
17	-5V Supply A/D Converter-Analog	37	GND of Ref. Voltage A/D Converter
18	Clock Input A/D Converter-Analog	38	External Analog Input
19	+5V Supply A/D Converter	39	Output Signal Switchover Input
20	Peak Clamping Enable Input	40	+5V Supply D/A-Analog

EVALUATION CIRCUIT

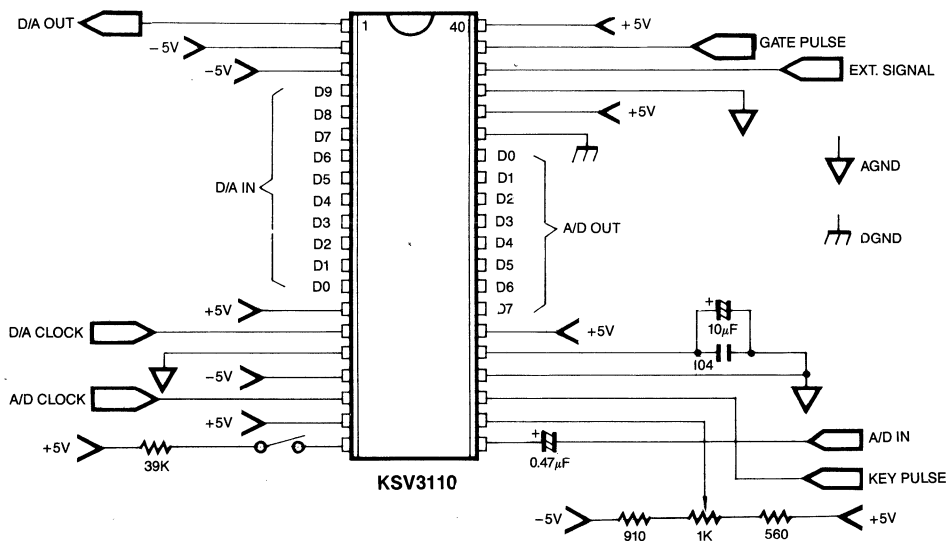


Fig. 2

ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Positive Supply Voltage	V_{CC}	- 0.5 to + 6	V
Negative Supply Voltage	V_{EE}	+ 0.5 to - 6	V
Input Voltages (digital)	V_{DI}	- 0.5 to + 5.5	V
Input Voltages (analog)	V_{AI}	- 0.5 to + 5.5	V
Digital Output Applied Voltage	V_{DO}	- 0.5 to + 5.5	V
Digital Output Forced Current	I_{DO}	- 2.0 to + 6.0	mA
Digital Output Short Time	t_{SHORT}	1	sec
Analog Output Applied Voltage	V_{AO}	- 0.5 to + 5.5	V
Analog Output Forced Current	I_{AO}	- 10 to + 0.5	mA
Ambient Operating Temperature	T_A	- 25 to + 85	degree
Storage Temperature Range	T_{SIG}	- 40 to + 125	degree

NOTE: 1. Absolute maximum ratings are limiting values applied individually, while all other parameters are within specified operating conditions.

2. Functional operation under any of these conditions is not implied.

3. Applied voltage must be current limited to specified range.

4. Current is specified as positive when flowing into the device.

OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Positive Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Negative Supply Voltage	V_{EE}	- 4.75	- 5.0	- 5.25	V
A/D Converter					
Clock High Time (1)	t_{CKH1}	15			ns
Clock Low Time (1)	t_{CKL1}	25			ns
Clamping Pulse High Time	t_{CLPH}	1			μ s
Clamping Pulse Low Time	t_{CLPL}	1			μ s
Digital Input High Voltage (1)	V_{DIH1}	2.0			V
Digital Input Low Voltage (1)	V_{DIL1}			0.8	V
Digital Output High Current	I_{DOH}			- 400	μ A
Digital Output Low Current	I_{DOL}			2.4	mA
Peak Clamping Resistance	R_{20}	20	39	60	Kohm
Analog Input Voltage	V_{AI}	0		V_{ref}	V
Clamping Level	V_{22}	- 1		2	V
D/A Converter					
Clock High Time (2)	t_{CKH2}	20			ns
Clock Low Time (2)	t_{CKL2}	20			ns

(Continue)

OPERATING CONDITIONS (Continued)

Characteristics	Symbol	Min	Typ	Max	Unit
Switch Over Pulse High Time	t_{39H}	1			μs
Switch Over Pulse Low Time	t_{39L}	1			μs
Digital Input High Voltage (2)	V_{DIH2}	2.0			V
Digital Input Low Voltage (2)	V_{DIL2}			0.8	V
Digital Input Set-up Time	t_{SET}	15			ns
Digital Input Hold Time	t_{HOLD}	12			ns
External Analog Input Voltage	V_{38}	-1		3	V
Ambient Temperature	T_A	0		70	degree

ELECTRICAL CHARACTERISTICS (within specified operation condition)

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Positive Supply Current	I_{CC}	$V_{CC} = \text{Max}$		105	140	mA
Negative Supply Current	I_{EE}	$V_{EE} = \text{Max}$		-95	-130	mA
A/D Converter						
Analog Input Bias Current	I_{AIN}	$V_{AI} = 2.0V, V_{EE} = \text{Max}$			5	μA
Analog Input Capacitance	C_{AIN}			5		pF
Analog Input Resistance	R_{AIN}	$F_{AIN} = 100\text{KHz}$		100		Kohm
Total String Resistance	R_{STRING}	$R_{(pin\ 25 - pin\ 37)}$	350	450	550	ohm
Reference Voltage	V_{REF}	$V_{pin\ 25}$	1.8		2.2	V
Clock High Current	I_{CKH1}	$V_{CK} = 2.4V, V_{CC} = \text{Max}$			50	μA
Clock Low Current	I_{CKL1}	$V_{CK} = 0.4V, V_{CC} = \text{Max}$			-800	μA
Clamping Pulse High Current	I_{CLPH}	$V_{CLP} = 2.4V, V_{CC} = \text{Max}$		8	50	μA
Clamping Pulse Low Current	I_{CLPL}	$V_{CLP} = 0.4V, V_{CC} = \text{Max}$			-500	μA
Digital Output High Voltage	V_{DOH}	$I_{DOH} = 0.4\text{mA}, V_{CC} = \text{Min}$	2.4			V
Digital Output Low Voltage (1)	V_{DOL1}	$I_{DOL} = 1.6\text{mA}, V_{CC} = \text{Min}$			0.5	V
Digital Output Low Voltage (2)	V_{DOL2}	$I_{DOL} = 2.4\text{mA}, V_{CC} = \text{Min}$			0.7	V
Maximum Conversion Rate	F_{AS}	$V_{CC}, V_{EE} = \text{Min}$	20			MSPS
Aperture Delay Time	t_{AP}	$V_{CC}, V_{EE} = \text{Min}$	-10		0	ns
Digital Output Delay	t_D	$V_{CC}, V_{EE} = \text{Min}$		15	20	ns
Clamp Level Sink Current	I_{22}	Peak: off, Keyed: off	0		150	μA
Peak Clamp Level Difference	ΔV_{PEAK}	V_{22}, V_{21}	-250	-100	0	mV
Keyed Clamp Level Difference	ΔV_{KEY}	V_{22}, V_{21}	-60			mV
Peak Clamp Charge Resistance	R_{PEAK}	$\Delta V_{21}/\Delta I_{22}, V_{21} < V_{22}$		150		ohm
Keyed Clamp Charge Resistance	R_{KEY}	$\Delta V_{21}/\Delta I_{22}, V_{21} < V_{22}$		150		ohm
Keyed Clamp Discharge Current	I_{KEY}	$V_{21} > V_{22}$		100		μA
Static Diff. Nonlinearity	SDNL1	$F_{IN} = 1\text{KHz}, CK = 1\text{MHz}$		0.2		%

ELECTRICAL CHARACTERISTICS (Continued)

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Dynamic Diff. Nonlinearity	DDNL	$A_{IN} = 1.02\text{MHz}$ $CK = 10\text{MHz}$ $A_{IN} = 6.0018\text{MHz}$ $CK = 25\text{MHz}$ (37.5% DUTY)		0.3		%
Dynamic Integral Nonlinearity	DINL	$A_{IN} = 1.02\text{MHz}$ $CK = 10\text{MHz}$		0.8	0.6	%
Full Power Input Band Width	BW		6			MHz
Full Code Offset Error	E_{FULL}	(Full Code Input) $- V_{REF}$	0	+ 100	+ 200	mV
Zero Code Offset Error	E_{ZERO}	(Zero Code Input) $- V_{REF}$	- 100	+ 40	+ 100	mV
Signal to Noise Ratio	SNR	$A_{IN} = 1.02\text{MHz}$ $CK = 10\text{MHz}$		42		dB
(RMS Signal/RMS Noise)		$A_{IN} = 1.02\text{MHz}$ $CK = 20\text{MHz}$ $A_{IN} = 3.601\text{MHz}$ $CK = 25\text{MHz}$ (37.5% DUTY)		35		dB
Differential Gain Error	DG	$A_{IN} = 3.579545\text{MHz}$ $CK = 14.318\text{MHz}$	30	34		dB
Differential Phase Error	DP	$A_{IN} = 3.579545\text{MHz}$ $CK = 14.318\text{MHz}$	- 1		3	%
			- 2		2	degree
D/A Converter						
Digital Input High Current	I_{DIH2}	$V_{CC} = \text{Max}$, $V_{DIH2} = 2.4\text{V}$			50	μA
Digital Input Low Current	I_{DIL2}	$V_{CC} = \text{Max}$, $V_{DIL2} = 0.4\text{V}$			- 500	μA
External Input Bias Current	I_{38}	$V_{CC} = \text{Max}$, $V_{38} = 3\text{V}$			10	μA
External Input Capacitance	C_{38}			5		pF
External Input Equ. Resistance	R_{38}	$F_{38} = 10\text{KHz}$		1		Mohm
External Amp. Offset Error	E_{OFFSET}	$V_{38} = - 1\text{V}$	- 100		100	mV
External Amp. Gain Error	E_{GAIN}	$\{(V1/V38) - 1\} * 100$	- 5		5	%
Max. Data Conversion Rate	F_{DC}		20			MSPS
Analog Output Delay	t_D				25	ns
Settling Time	t_{SET}	settle to 0.2%			40	ns
Rising Time	t_R	10% to 90%			50	ns
Falling Time	t_F	90% to 10%			35	ns
Glitch Amplitude	G_A				80	mV
Glitch Duration	G_D				7	ns
Glitch Energy	G_E				250	pV-sec
Static Diff. Nonlinearity	SDNL2	KSV3110-10			0.05	%
		KSV3110-9			0.1	%
		KSV3110-8			0.2	%
Static Integral Nonlinearity	SINL				1	%
Full Scale Output Voltage	V_{FULL}	$V_{CC} = \text{typ}$, $V_{EE} = \text{typ}$	1.8		2.2	V
Zero Scale Output Voltage	V_{ZERO}	$V_{CC} = \text{typ}$, $V_{EE} = \text{typ}$	- 60		+ 60	mV

MARKING SPECIFICATIONS (Ordering Information)

The KSV3110 has three versions according to the accuracy bit (so-called 'precision') of the D/A Converter, and their marking specifications are as follows:

Marking Spec.	D/A Converter		A/D Converter	Package	Temp. Range
	Accuracy Bit	Diff. Nonlinearity	Diff. Nonlinearity		
KSV3110-10	10-bit	0.05%	0.2%	40 DIP	0 ~ +70°C
KSV3110-9	9-bit	0.1%			
KSV3110-8	8-bit	0.2%			

TIMING DIAGRAM

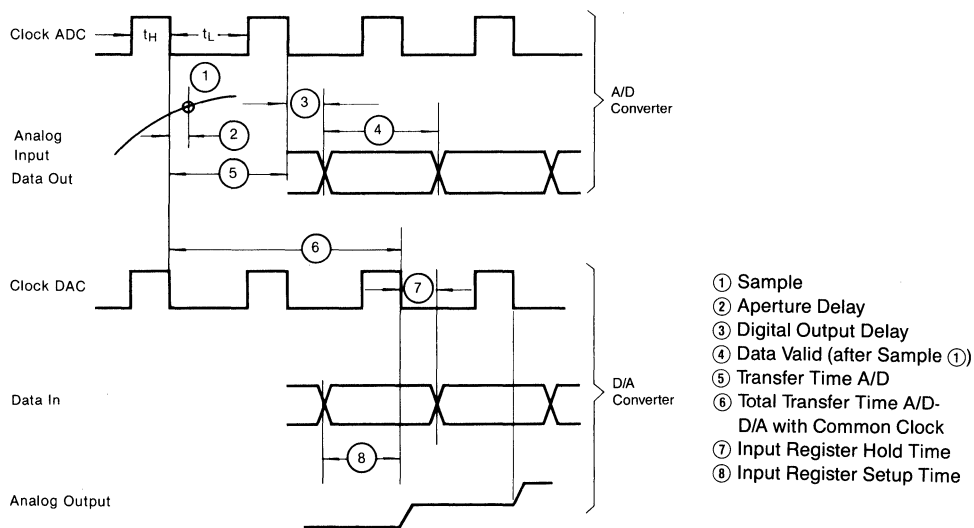


Fig. 3

PACKAGE LAYOUT

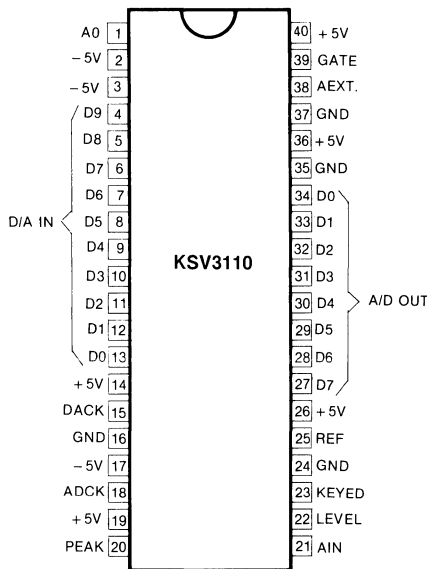


Fig. 4

DESCRIPTION OF THE CONNECTION AND THE SIGNALS

Pin No.	Description
Pin 1	Analog Output D/A Converter This pin, whose diagram is shown in Fig. 7, is the output for the processed analog signal either originating from the D/A converter or from the external analog input Pin 38.
Pin 2	- 5-volt Supply D/A Converter, Analog This pin gets the negative supply for the analog part of the D/A converter
Pin 3	- 5-volt Supply D/A Converter, Digital This pin gets the negative supply for the digital part of the D/A converter.
Pin 4 to 13	Digital Inputs Bit 9 to Bit 0 This diagram of these pins is shown in Fig. 5. They are the inputs of the D/A converter and not-used inputs should be connected to the ground.
Pin 14	+ 5-volt Supply D/A Converter, Digital This pin gets the positive supply for the digital part of the D/A converter.
Pin 15	Clock Input D/A Converter This pin, whose diagram is shown in Fig. 5, must be supplied with the clock signal for the D/A converter.
Pin 16	Ground D/A Converter and Clock A/D Converter This pin serves as ground pin for the D/A converter and for the clock of the A/D converter.

DESCRIPTION OF THE CONNECTION AND THE SIGNALS (Continued)

Pin No.	Description
Pin 17	– 5-volt Supply A/D Converter, Analog This pin is the negative supply pin for the analog part of the A/D Converter.
Pin 18	Clock Input A/D Converter The diagram of this pin is shown in Fig. 5. Pin 18 is supplied with the clock of the A/D converter.
Pin 19	+ 5-volt Supply A/D Converter Via this pin the A/D converter gets its positive supply.
Pin 20	Peak Clamping Enable Input Via Pin 20, whose diagram is shown in Fig. 6, the peak clamping facility can be enabled.
Pin 21	Analog Input A/D Converter Fig. 7 is the diagram of this input. To Pin 21 is applied the analog signal to be converted into digital.
Pin 22	Clamping Level Input Via this pin, whose diagram is shown in Fig. 6, the input of the A/D converter is supplied with the desired clamping level.
Pin 23	Clamping Pulse Input Pin 23 must be supplied with the key pulse if keyed clamping is required.
Pin 24	Analog Ground A/D Converter This pin serves as the ground pin for the analog part of the A/D converter.
Pin 25	Reference-voltage A/D Converter This pin, whose diagram is shown in Fig. 8, is intended for connecting a decoupling capacitor to the A/D converter's reference voltage, the other end of this capacitor to Pin 37.
Pin 26	+ 5-volt Supply A/D Converter, Digital This pin is the positive supply pin for the digital part of the A/D converter.
Pin 27 to 34	Digital Outputs Bit 7 to Bit 0 Fig. 11 shows the diagram of these outputs which supply the digitized analog signal in parallel 8-bit code.
Pin 35	Digital Ground A/D Converter This pin is the ground connection for the digital part of the A/D converter.
Pin 36	+ 5-volt Supply A/D Converter, Analog This pin is the positive supply pin for the analog part of the A/D converter.
Pin 37	Ground of Reference-voltage A/D Converter To this pin must be connected the ground end of the decoupling which is at Pin 25.
Pin 38	External Analog Input The diagram of this input is shown in Fig. 10. Pin 38 serves for feeding an external analog signal into the output amplifier of the KSV3110 instead of the D/A-converted signal originating from Pins 4 to 13.
Pin 39	Output Signal Switchover Input This pin, whose diagram is shown in Fig. 5, is intended for enabling the external analog signal fed to Pin 38.
Pin 40	+ 5-volt Supply Converter, Analog This pin is the negative supply pin for the analog parts of the D/A converter.

INNER CONFIGURATION OF THE CONNECTION PINS

The following figures schematically show the circuitry at the various pins.

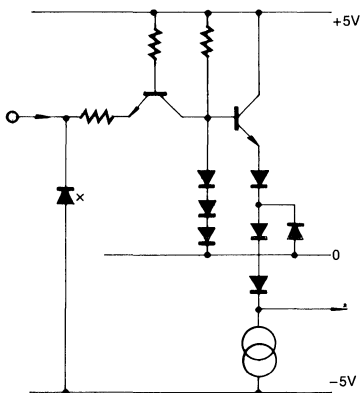


Fig. 5: Pins 4 to 13, 15, 18, 23 and 39, Inputs

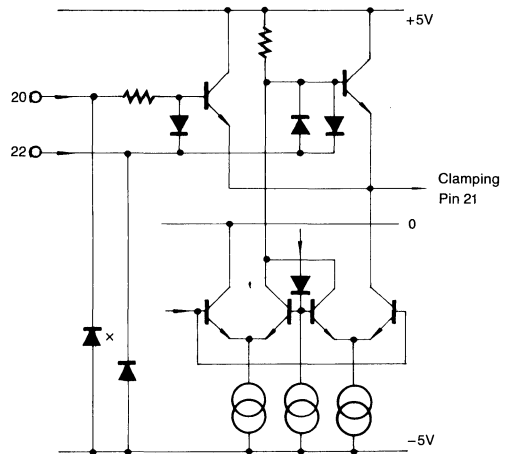


Fig. 6: Pins 20 and 22, Inputs

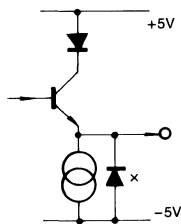


Fig. 7: Pin 1, Output
x = protection diode

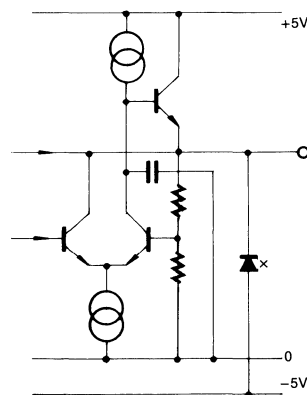


Fig. 8: Pin 25, Reference Voltage Pin

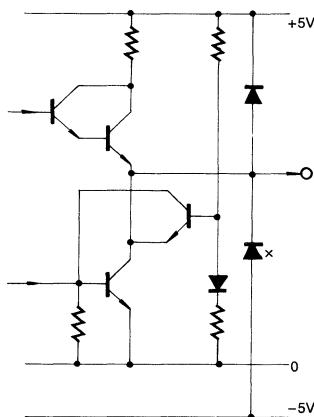
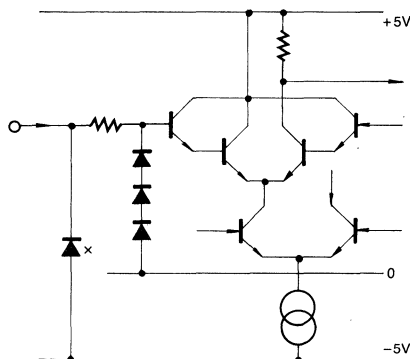


Fig. 9: Pins 27 to 34, Outputs

Fig. 10: Pin 38, Input
x=protection diode

RECOMMENDED APPLICATION CIRCUIT

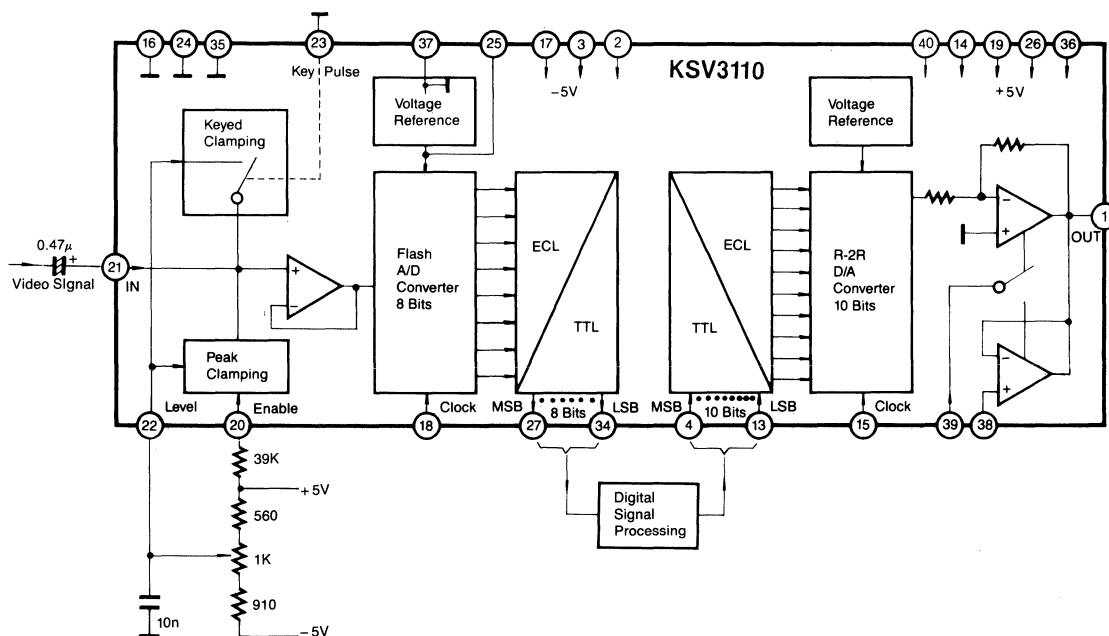


Fig. 11: Operation with peak clamping

The input signal is clamped automatically to the negative peak value. Pin 20 is connected to +5V via a 39KΩ resistor, and Pin 22 (clamping level input) is connected, as desired, to zero or a voltage between -1 and +2V. The input signal is fed to Pin 21 by way of a coupling capacitor, and no key pulse (clamping pulse) is needed.

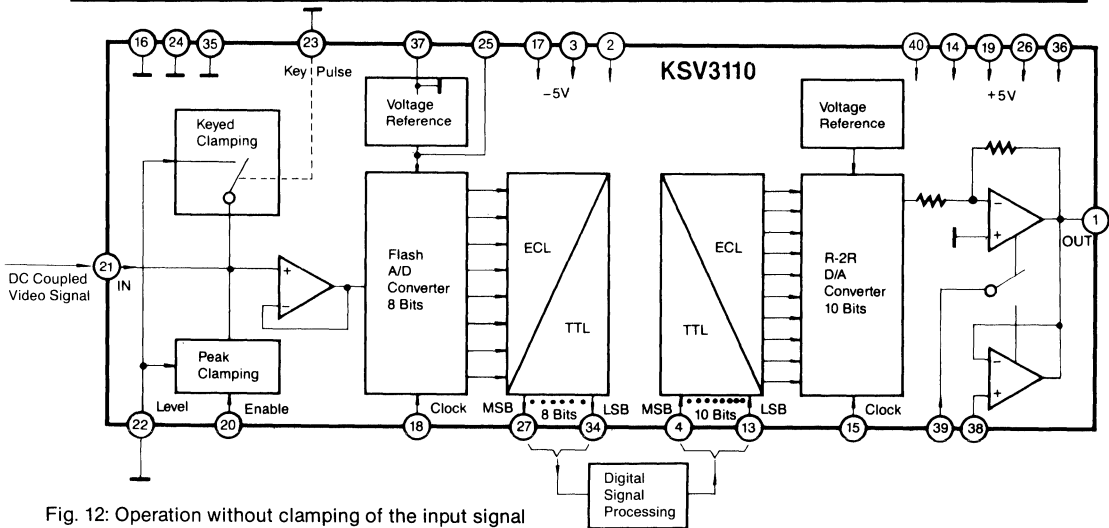


Fig. 12: Operation without clamping of the input signal

Pin 20 (peak clamping enable input) should be opened, while Pin 23 (clamping pulse input) remains at 0V. The input signal is applied to the analog input, Pin 21, without a coupling capacitor such that it lies between 0 and + 2V.

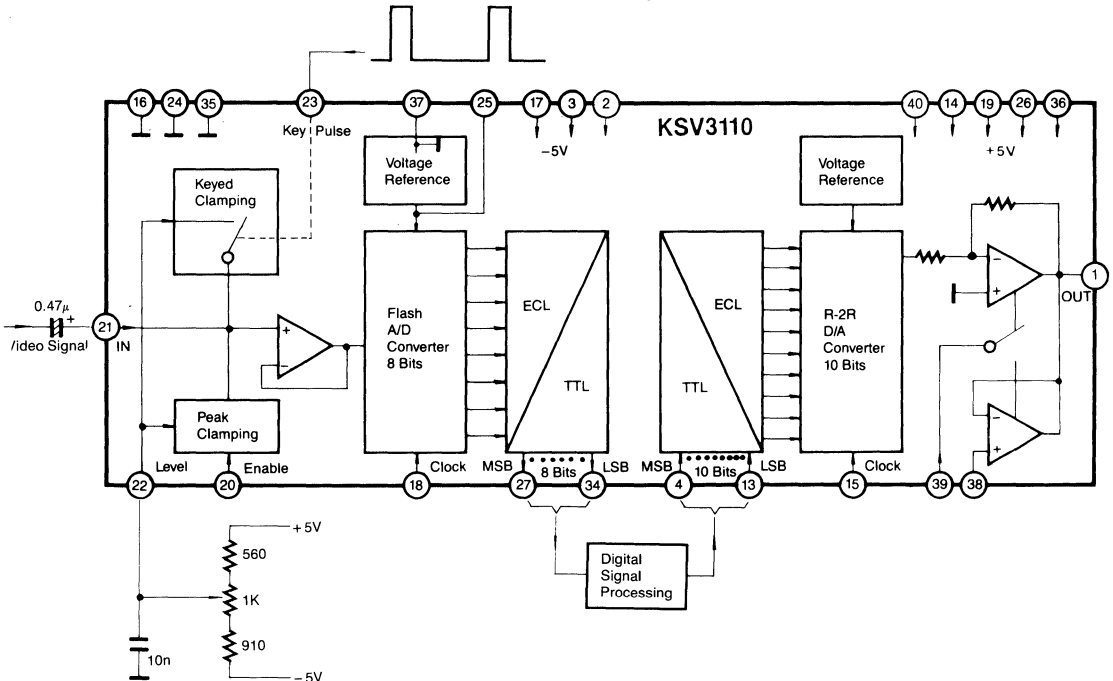


Fig. 13: Operation with keyed clamping

The input signal is applied to Pin 21 through a coupling capacitor. Pin 20 must not be connected. While the input signal is at the desired clamping level, a high-level is applied at the clamping pulse input, Pin 23. By this means the clamping switch in the KSV3110 connects the input with the clamping level at Pin 22 and recharges the coupling capacitor accordingly. The clamping level can be set to zero or, by means of an external voltage divider, to any desired value between - 1 and + 2V.

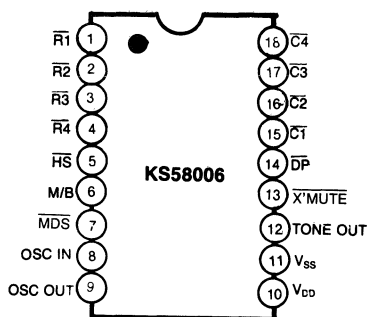
TONE/PULSE DIALER WITH REDIAL

The KS58006 is DTMF/PULSE switchable dialer with a 32-digit redial can be done using a slide a switch. All necessary dual-tone frequencies are derived from a 3.579545 MHz TV crystal or ceramic resonator providing very high accuracy and stability. The required sinusoidal wave form for each individual tone is digitally synthesized on the chip. The wave form so generated has very low total harmonic distortion (7% max). A voltage reference is generated on the chip which is stable over the operating voltage and temperature range and regulates the single levels of the dual tone to meet telephone industry specifications. CMOS technology is applied to this device, for very low power requirements high noise immunity, and easy interface to a variety of telephones requiring external components.

FEATURES

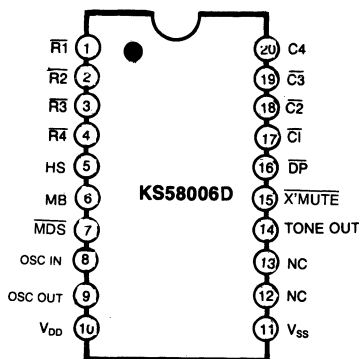
- Tone/Pulse switchable (slide switch).
- 32-digit capacity for redial
- Automatic mix redialing (last number dial) of PULSE→DTMF with multiple auto access pause
- PABX auto-pause for 3.5 sec.
- 4 × 4 or (2 of 8) keyboard available
- Two key single tone operation
- Operating Voltage: 2.0 ~ 5.5V
- Numbers dialed manually after redial are cascadable and stored as additional numbers for next redialing
- Uses inexpensive TV crystal or ceramic resonator (3.579545MHz)
- Make/Break ratio (33 1/3 ~ 66 2/3 or 40/60) pin selectable
- Touch key hooking (604ms)
- Low standby current
- Improved EMI characteristic
- Improved redial memory quality

PIN CONFIGURATION



(DIP)

Fig. 1



(SOP)

Fig. 2

18 DIP

20 SOP

ORDERING INFORMATION

Device	Package	Operating Temperature
KS58006	18 DIP	- 20 ~ 70°C
KS58006D	20 SOP	

BLOCK DIAGRAM

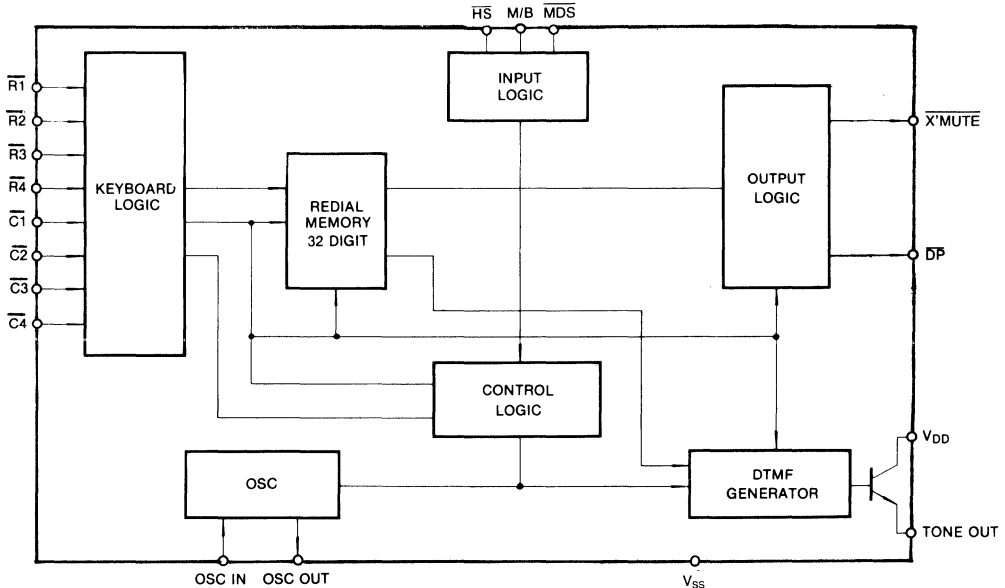
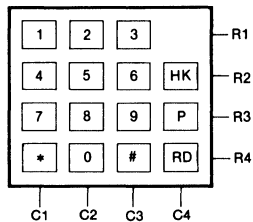


Fig. 3

ARRANGEMENT OF KEYBOARD



*KEYBOARD DESCRIPTION

HK : HOOKING (604ms)

P : PAUSE (3.5 second)

RD : REDIAL

TONE FREQUENCIES

Input	Specified	Actual	% Error
R1	697	699.1	+ 0.31
R2	770	766.2	- 0.49
R3	852	847.4	- 0.54
R4	941	948.0	+ 0.74
C1	1209	1215.7	+ 0.57
C2	1336	1331.7	- 0.32
C3	1477	1471.9	- 0.35

PIN DESCRIPTION

Pin No	Symbol	Description									
1-4 15-18	$\overline{R1-R4}$ $\overline{C1-C4}$	Keyboard ($\overline{R1}$, $\overline{R2}$, $\overline{R3}$, $\overline{R4}$, $\overline{C1}$, $\overline{C2}$, $\overline{C3}$, $\overline{C4}$) These inputs can be interfaced to an XY matrix keyboard. $\overline{C1-C4}$ & $\overline{R1-R4}$ are set to low at On Hook ($\overline{HS}$ = high). $\overline{C1-C4}$ key inputs are set to low and $\overline{R1-R4}$ are set to high at OFF HOOK ($\overline{HS}$ = low) which enables the key-input operation. The oscillator starts running when a keypress is detected. Scanning signals are presented at both column and row inputs (TYP: 437Hz) until the input key is released. Key inputs are compatible with standard 2-of-8 form or single-contact keyboard. Debouncing is provided to avoid false entry (TYP: 4mS).									
5	$\overline{HS}$	Hook Switch This input detects the state of the hook switch contact. "Off Hook" corresponds to V_{SS} condition. "On Hook" corresponds to V_{DD} condition.									
6	M/B	Make/Break Ratio This input provides the selection of the Make/Break ratio (33.3: 66.6/40:60) when M/B is connected to V_{DD}/V_{SS} .									
7	$\overline{MDS}$	Mode Select Input Pulse/DTMF mode is selected as shown in the following table. Initial Mode means the state after going Off Hook ($\overline{HS} \rightarrow "V_{SS}"$) <table><tr><th>$\overline{MDS}$</th><th>INITIAL MODE</th><th>SWITCHING ENTRY MODE</th></tr><tr><td>V_{DD}</td><td>Pulse</td><td>$\overline{MDS}$ Input = V_{SS}</td></tr><tr><td>V_{SS}</td><td>Tone</td><td>N/A</td></tr></table>	$\overline{MDS}$	INITIAL MODE	SWITCHING ENTRY MODE	V_{DD}	Pulse	$\overline{MDS}$ Input = V_{SS}	V_{SS}	Tone	N/A
$\overline{MDS}$	INITIAL MODE	SWITCHING ENTRY MODE									
V_{DD}	Pulse	$\overline{MDS}$ Input = V_{SS}									
V_{SS}	Tone	N/A									
8-9	OSC IN OSC OUT	Oscillator Input/Output These pins are provided to connect an external 3.58MHz crystal. Oscillator starts (at Off Hook) and is sustained until pulse or DTMF signals are finished.									
10-11	V_{DD} , V_{SS}	Power These are the power supply inputs. The device is designed to be operated on 2.0V to 5.5V.									
12	TONE OUT	DTMF Signal Output When a valid keypress is detected in DTMF mode appropriate low and high group frequencies are generated which hybrid the Dual Tone Output. Tone out is Off State in pulse mode.									
13	$\overline{X'MUTE}$	$\overline{X'MUTE}$ Output <table><tr><th>$\overline{HS}$</th><th>$\overline{X'MUTE}$ Output</th></tr><tr><td>V_{DD}</td><td>"ON"</td></tr><tr><td>V_{SS}</td><td>Normally "OFF" "ON" during pulse and DTMF dialing</td></tr></table> (N channel open drain)	$\overline{HS}$	$\overline{X'MUTE}$ Output	V_{DD}	"ON"	V_{SS}	Normally "OFF" "ON" during pulse and DTMF dialing			
$\overline{HS}$	$\overline{X'MUTE}$ Output										
V_{DD}	"ON"										
V_{SS}	Normally "OFF" "ON" during pulse and DTMF dialing										
14	$\overline{DP}$	Dial Pulse Out $\overline{DP}$: The normal output will be "ON" during break and "OFF" during make at "OFF HOOK." The output will be "OFF" at "ON HOOK."									

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V _{DD}	6.0	V
Input Voltage	V _I	V _{SS} - 0.3, V _{DD} + 0.3	V
Output Voltage	V _O	V _{SS} - 0.3, V _{DD} + 0.3	V
Output Voltage	V _{O(DXM)}	≤ V _{DD} (DP, X'MUTE, MUTE)	V
Tone Output Current	I _{O (TONE)}	50	mA
Power Dissipation	P _D	500	mW
Operating Temperature	T _{OPR}	- 20 ~ + 70	°C
Storage Temperature	T _{STG}	- 40 ~ + 125	°C

ELECTRICAL CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 3.5V, f_{X'TAL} = 3.579545MHz, Ta = 25°C, unless otherwise noted)

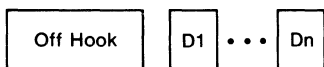
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Voltage Range	V _{DD}		2.0		5.5	V
Memory Retention Voltage	V _{MR}		1.0			V
Memory Retention Current	I _{MR}	HS = V _{DD} = 1.0V		0.05	0.1	μA
Operating Current	I _{DD (PULSE)}	MDS = V _{DD} One key selected HS = V _{SS} . All outputs unloaded		0.1	0.3	mA
	I _{DD (TONE)}	MDS = V _{SS}		0.4	0.7	
Standby Current	I _{SB}	HS = V _{SS} No key selected. All outputs unloaded		10	50	μA
Output Current	I _{OL1}	DP, V _{OL} = 0.4V V _{DD} = 3.5V	1.7	5.0		mA
	I _{OL2}	X'MUTE V _{DD} = 2.5V	0.5	1.5		
Input Voltage	V _{IH}	R1-R4, C1-C3, HS, M/B MDS	0.8V _{DD}		V _{DD}	V
	V _{IL}		V _{SS}		0.2V _{DD}	
Input Current	I _{L1}	V _{DD} = 3.5V V _{IN} = 0V			50	μA
	I _{L2}	V _{DD} = 2.5V V _{IN} = 0V			30	
Valid Key Entry Time	t _{KD}			23		mS
Key Release Time	t _{KR}			5		mS
Tone Duration	t _{TD}			110		mS
Tone Interdigit Pause Time	t _{TIDP}			110		mS
Column and Row Scanning Frequency	f _{CR}			437		Hz
Auto Access Pause Time	t _{AP}			3.5		sec
Tone Output	V _{O (TONE)}	ROW TONE ONLY V _{DD} = 2.5V, R _L = 5KΩ	- 14.0		- 12.0	dBV
		V _{DD} = 3.5V, R _L = 5KΩ	- 14.0		- 12.0	
Ratio of Column to Row Tone	dB _{CR}	V _{DD} = 3.5V	1.0	2.0	3.0	dB
Distortion	THD	V _{DD} = 3.5V			7	%
Tone Output Delay Time	t _{D (TONE)}			1.5		mS

APPLICATION INFORMATION

KEYBOARD OPERATION

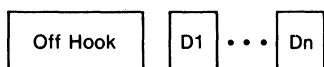
1. SINGLE MODE OPERATION

• Pulse Mode Operation



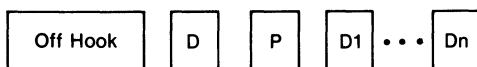
The pulse mode is defined by the initial mode after going Off Hook and latched at $\overline{D1}$ key entry. This is the condition under $\overline{MDS} = V_{DD}$.

• Tone Mode Operation



The tone mode is defined by the initial mode after going Off Hook and latched at $\overline{D1}$ key entry. This is the condition under $\overline{MDS} = V_{SS}$.

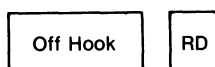
• Manual Dialing with Automatic Access Pause



Multiple Pause key entries can be accepted and stored in the redial memory, each as a digit. Each $\overline{P}$ key provides 3.5 seconds pause time, but the $\overline{P}$ key entry as the first digit after going Off Hook is ignored. The $\overline{P}$ key can also be used as a pause key in the pulse mode. Pause (2) can be cancelled with the $\overline{P}$ or $\overline{RD}$ key during pause time in redialing.

$\overline{D}$ = Any numeric key.

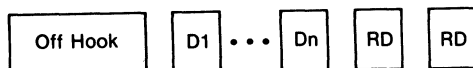
• Redialing



Up to 32 digits can be dialed with the $\overline{RD}$ key. The $\overline{RD}$ key is disabled while pulse or DTMF signals are transmitted. When more than 32 digits are stored, redial is also inhibited.

The $\overline{\#}$ key can be used as the $\overline{RD}$ key in the pulse mode.

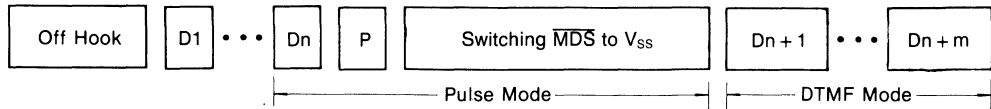
• Inhibiting Redial



Redial can be inhibited by depressing the $\overline{RD}$ key twice after DTMF or pulse signals are transmitted.

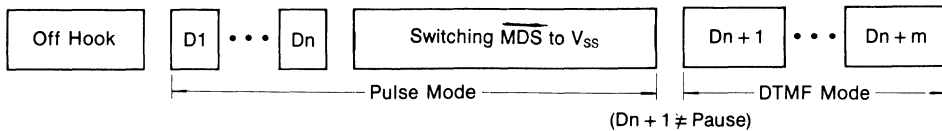
2. PULSE/TONE SWITCHABLE OPERATION

• Mode Switching by MDS Input



The pulse mode is initially defined $\overline{\text{MDS}} = V_{DD}$, mode switching to the DTMF mode can be accepted by $\overline{\text{MDS}} = V_{SS}$, the DTMF mode will be set up after the pulse mode is finished. In this mode, digits $D_{n+1} \dots D_{n+m}$ are transmitted from Tone Out as DTMF signals by depressing the corresponding keys.

If no P key is contained serially before or after mode switching, the following condition is obtained.



If digit D_{n+1} is depressed after the pulse mode is finished, the DTMF mode will be set up after last the pulse signal (D_n) is generated. In this mode, digits $D_{n+1} \dots D_{n+m}$ are transmitted from Tone Out as DTMF signals by depressing the corresponding keys. If digit D_{n+1} is depressed during dialing pulse signals. What happens? When the DTMF mode is set the Hold State will be set after last pulse signal D_n is finished. $\overline{\text{MDO}}$ will flash to indicate this Hold State. $D_{n+1} \dots D_{n+m}$ are stored in redial memory as DTMF DATA and not transmitted from Tone Out. When it is ready to transmit DTMF data in redial memory, the $\overline{\text{RD}}$ or $\overline{\text{P}}$ key is depressed to reset this Hold State and $D_{n+1} \dots D_{n+m}$ data are serially transmitted.

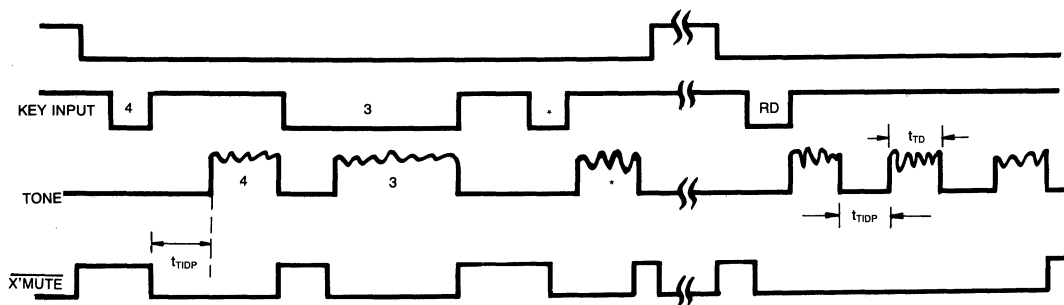
TONE MODE TIMING ($\overline{\text{MDS}} = V_{SS}$)

Fig. 4

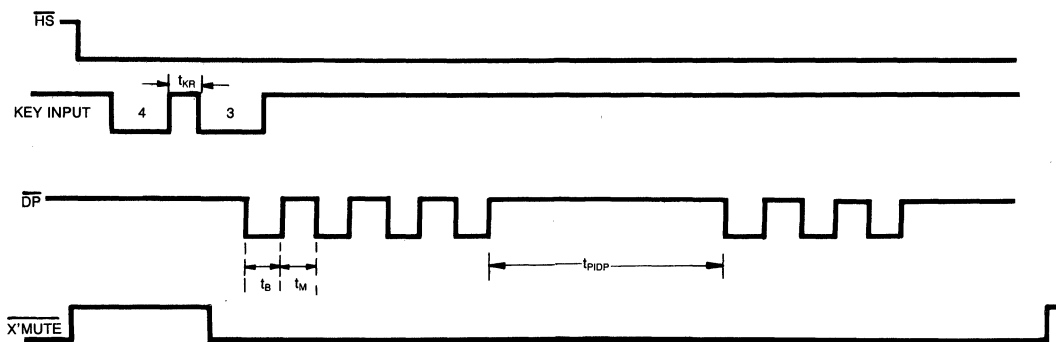
PULSE MODE TIMING ($\overline{\text{MDS}} = V_{DD}$)

Fig. 5

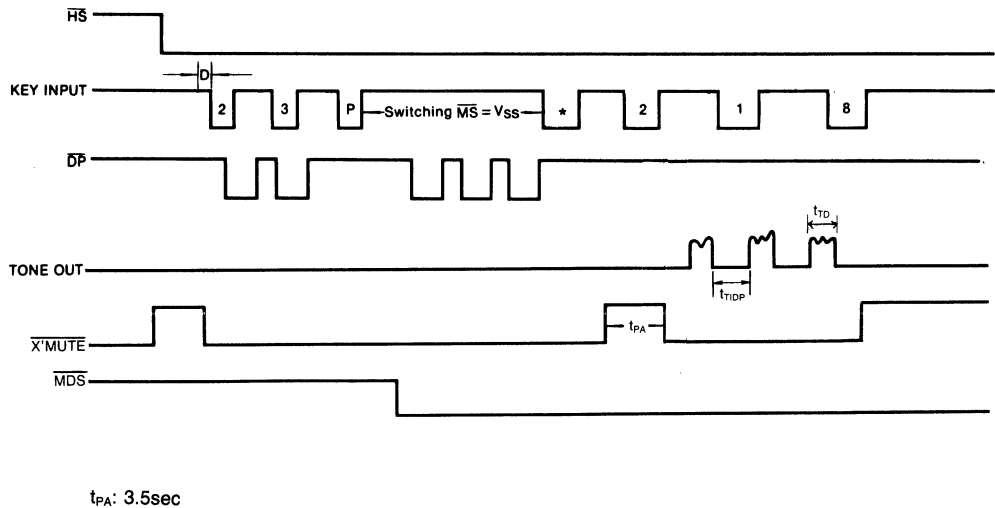
TIMING DIAGRAM (for Switching Mode Operation by $\overline{\text{MDS}}$ Input)

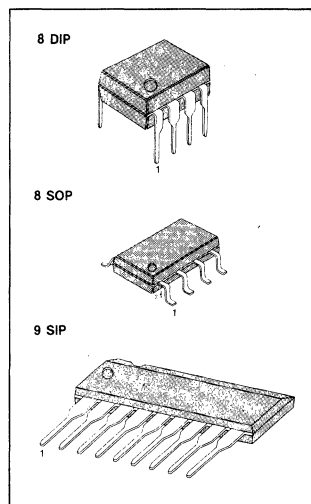
Fig. 6

LOW VOLTAGE AUDIO POWER AMPLIFIER

The KA386/S/D is a power amplifier designed for use in low voltage consumer applications. The gain is internally set to 20 to keep the external part count low, but the addition of an external resistor and capacitor between Pins 1 and 8 will increase the gain to any value up to 200.

FEATURES

- Battery operation.
- Minimum external parts.
- Wide supply voltage range: 4V ~ 12V (KA386)
4V ~ 9V (KA386S/D)
- Low quiescent current drain (4mA.)
- Voltage gains : 20 ~ 200.
- Ground referenced input.
- Self-centering output quiescent voltage.
- Low distortion.
- 3 kinds of package types
KA386 (8 Dip), KA386S (9 Sip), KA386D (8 Sop)



ORDERING INFORMATION

Device	Package	Operating Temperature
KA386	8 DIP	- 20°C ~ + 70°C
KA386S	9 SIP	
KA386D	8 SOP	

BLOCK DIAGRAM

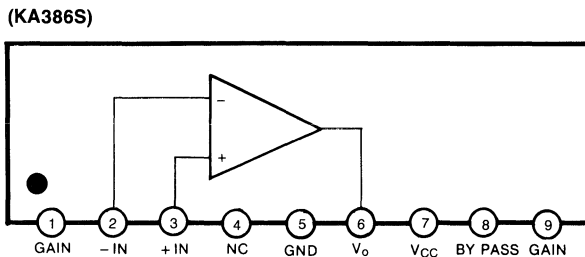
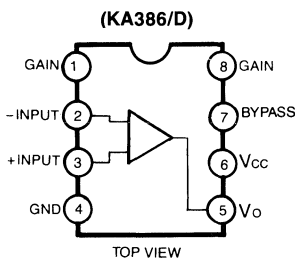


Fig. 1

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Characteristic		Symbol	Value	Unit
Supply Voltage		V_{CC}	15	V
Power Dissipation	KA386	P_D	660	mW
	KA386S		500	
	KA386D		300	
Input Voltage		V_I	± 0.4	V
Operating Temperature		T_{OPR}	$-20 \sim +70$	$^\circ\text{C}$
Storage Temperature		T_{STG}	$-40 \sim +125$	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS

($T_a = 25^\circ\text{C}$, $V_{CC} = 6\text{V}$, $R_L = 8\Omega$, $f = 1\text{KHz}$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CCQ}	$V_I = 0$		4	8	mA
Output Power	P_o	$V_{CC} = 6\text{V}$, THD = 10%	250	325		mW
		$V_{CC} = 9\text{V}$, THD = 10%	500	700		mW
Voltage Gain	G_V	Pins 1 and 8 Open		26		dB
		$10\mu\text{F}$ from Pin 1 to 8		46		
Bandwidth	BW	Pins 1 and 8 Open		300		KHz
		$10\mu\text{F}$ from Pin 1 to 8		60		
Total Harmonic Distortion (D-Type)	THD	$P_o = 125\text{mW}$, Pins 1 and 8 Open		0.2		%
Input Resistance	R_i			50		$\text{K}\Omega$
Input Bias Current	I_{BIAS}	Pins 1 and 8 Open		250		nA

APPLICATION CIRCUIT

Amplifier with Gain=50 (34 dB)

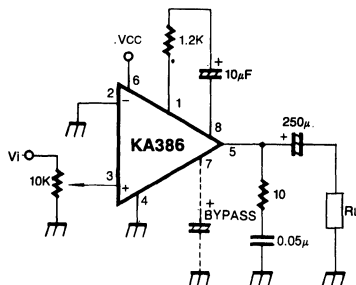


Fig. 2

APPLICATIONS 3



MOSFET RUGGEDNESS
PWM CONTROL ICs
PWM SWITCHING REGULATOR DEVICES
DATA CONVERTERS
FLASH CONVERTERS

MOSFET RUGGEDNESS

Application Note

PREFACE

INTRODUCTION

This application note discusses why and how MOSFET devices fail in switch-mode applications. It deals with the issue of ruggedness in the design of the device, and with system design strategies that can minimize the impact of MOSFET failure in the field. The term 'ruggedness' as applied to MOSFET devices relates to the capability of the device to resist catastrophic failure under dynamic electrical stress. The ruggedness of the device is an indication of the quality and reliability of the component.

At one time, many MOSFET failures were inexplicable, and dismissed as random. However, since failures continued, designers realised that recurrent failure patterns required investigation. Specific failure mechanisms were identified that link the physics inside the MOSFET and the operating environment of the device.

CONTENTS

The note is divided into three major parts:

Part 1 describes failure mechanisms, as they relate to the physics of the MOSFET in a circuit environment. This is the starting point for a fundamental understanding of the variables in the ruggedness equation.

Part 2 discusses ruggedness testing issues; looks at how the parameters are measured, and what they mean.

Part 3 deals with MOSFET applications. It takes the information presented in Parts 1 and 2 to address design considerations, and the design problems caused by dynamic electrical stresses. It presents circuit design strategies that eliminate ruggedness related MOSFET failures in the field.

In addition:

Appendix A describes the design, manufacturing and testing techniques that Samsung uses to ensure that their devices meet stringent performance requirements.

Appendix B lists the abbreviations used in the note.

References lists other related reading material.

About the author is a brief biographical profile of the author.

PURPOSE

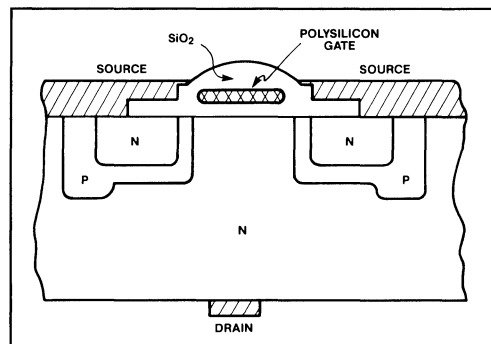
This application note is intended primarily for design engineers who are using MOSFETs in power systems. It also contains information useful to components engineers and quality control staff who are responsible for qualifying and testing incoming MOSFET devices.

PART 1-FAILURE MECHANISMS

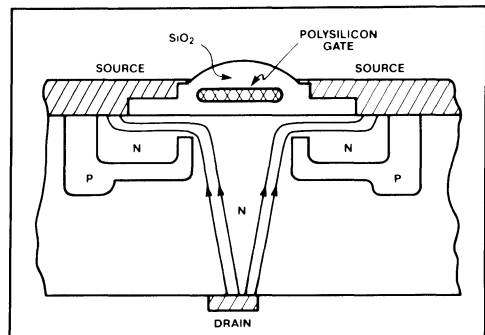
INTRODUCTION

Ruggedness related failures in the MOSFET are caused by electrical stresses that occur when the device is used in switchmode power applications. These stresses come in several easily distinguishable forms, each capable of destroying a working MOSFET, and seriously damaging the instrument in which the MOSFET is being used.

To understand what these stresses are, and how they cause failures, we have to look inside the MOSFET. There we see that the device consists of many active cells, all in parallel and each identical in form. Figure 1 shows the cross section of a cell in a double-diffused vertical MOSFET (VDMOS). (There are several different types of MOSFET structures, but the VDMOS is by far the most popular, representing about 85% of the devices manufactured.) Figure 1a shows the channel open, with conventional current flowing from



a. Channel closed



b. Channel open

Figure 1. Cross Sections of MOSFET VDMOS Cell

drain to source. Ruggedness issues involve only the closed channel or blocking state shown in Figure 1a. The physics of MOSFET operation lends itself to straightforward electrical equivalent circuits. The device is composed of alternating sections of 'p' and 'n' materials: precisely the composition of a bipolar (npn) transistor. The overlay in Figure 2a identifies the lumped equivalent circuit components. Figure 2b shows the lumped circuit in detail. What we have is an identifiable parasitic bipolar junction transistor (PBJT) intrinsic to the MOSFET cell structure. If this cellular transistor is turned on in any of the hundreds of cells, the entire MOSFET fails. This leads to a definition: ruggedness is the ability of a MOSFET to operate in an environment of *dynamic electrical stresses*, without activating any of the parasitic bipolar junction transistors (PBJT).

The *dynamic electrical stresses* can be subdivided into three distinct types:

1. Avalanche energy injection. (Referred to in the text as Mode 1.)
2. Diode recovery dv/dt . (Referred to in the text as Mode 2.)
3. Static dv/dt . (Referred to in the text as Mode 3.)

AVALANCHE ENERGY INJECTION—MODE 1

In the off or blocking state, with voltage on the drain of the MOSFET, a small leakage current (I_{dss}) flows through the device. As the voltage increases, the current remains relatively small, until the drain voltage approaches the breakdown voltage (BV_{dss}) of the device. At this voltage level, there is a rapid increase in

current through the MOSFET caused by the avalanche (reverse breakdown) of the body diode. This is fundamental to avalanche injection energy stress, hence the name.

This stress is not necessarily destructive to the device. Impact depends upon the size of the avalanche current, and the junction temperature. Both R_{be} and the forward bias level of the PBJT are temperature dependent. Therefore, to characterize the avalanche capability of the device, both the current level and the junction temperature must be specified. There are no 'wear-out' mechanisms in the cell structure that are susceptible to body diode avalanche. So turning on the PBJT, not avalanching the body diode, is the major problem.

With avalanche current passing through R_{be} in the direction shown in Figure 3, the PBJT will turn on if the voltage across R_{be} is approximately 0.7 volts. When this happens, the blocking voltage capability of the PBJT drops from BV_{ces} to BV_{ceo} , usually allowing high current conduction to the point where a second breakdown is usually unavoidable. Breakdown is a certainty if BV_{ceo} is less than the applied voltage.

Because of the poor avalanche energy capability of early MOSFET devices, past theory implied that MOSFETs were extremely prone to failure from high voltage spikes on the drain. After extensive research, we now know that they are not drain voltage sensitive, but rather avalanche current sensitive. In fact, recalling that the DC voltage safe-operating area (SOA) boundary (V_{dss}) is set approximately 15-20% below breakdown (BV_{dss}), under some prescribed conditions, which we will discuss below, operation with the device in breakdown is permitted.

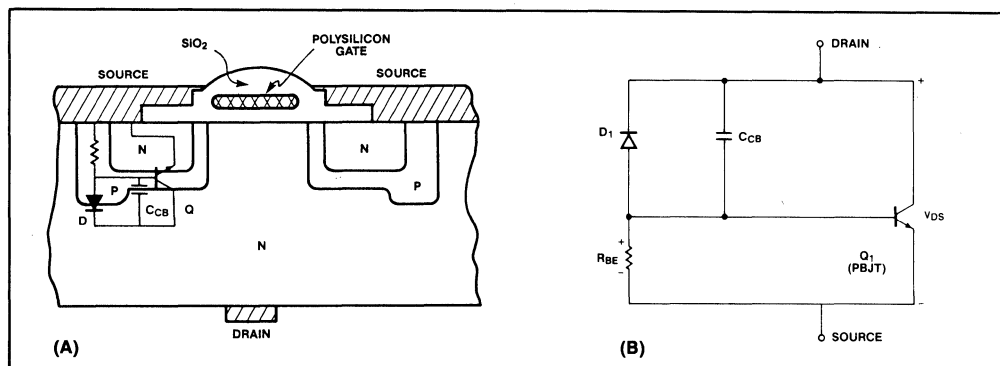


Figure 2. Lumped Equivalent Circuit Components

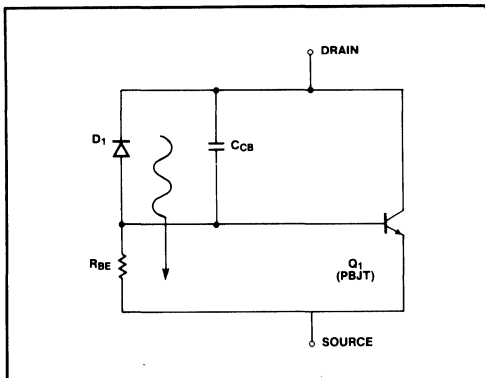


Figure 3. Avalanche Current Injection

DIODE RECOVERY dv/dt RATING—MODE 2

This problem is known by several names: commutating dv/dt ; di/dt ; commutating safe operating area (CSOA); and others.

Unlike avalanche injection, this failure mode cannot be directly linked to the DC safe operating area (SOA) curves. It is characterized by the load current conduction in the body diode (BD), as required by freewheeling inductance loads.

To explain the basic failure mechanism, Figure 4 shows a circuit that provides pulse DC drive voltage to an inductive load. Defining the system as being initially at rest, turning on Q2, while Q1 remains off applies power to the load, causing current (I_L) to ramp up. When Q2 turns off, current commutates through the body diode of Q1.

Assuming steady state periodic application of this

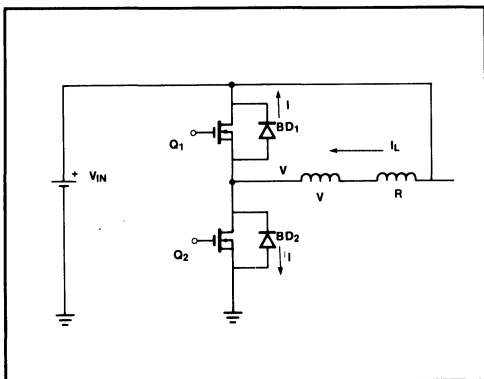


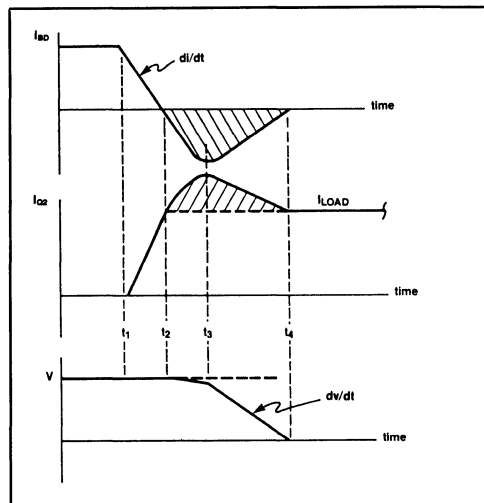
Figure 4. DC Drive Voltage Applied to Inductive Load

pulse drive, the timing relationship between Q1 body diode current, Q2 drain current, and drain voltage, are illustrated in Figure 5.

When Q2 turns on at time t_1 , load current begins to commute from Q1 to Q2. At time t_2 , load current is fully committed to Q2, and the charge is beginning to flow out of the body diode pn junction. This flow takes on the form of additional current that adds to the current in Q2. An interesting and important point is that I_L remains constant over the entire switching interval. That is, the sum of the body diode current in Q1 (I_L) summed with the drain current in Q2, remains a constant, equal to the inductive (motor) load.

At time t_2 , drain voltage on Q2 (V_{ds2}) begins to fall. This continues at a very slow rate until t_3 , which is the peak of the reverse recovery current from the body diode in Q1. At time t_3 , the voltage across Q2 falls very fast. This rate of voltage change is one of the critical parameters, and is the dv/dt referred to in the name for Mode 2 stress.

The important variables, as defined in Figure 5, are dv/dt , di/dt , I_{BD} , and though not explicitly shown, T_r . Their magnitude levels determine the degree of Mode 2 stress and whether or not the PBJT will turn on. To explain this, we can refer to Figure 6, which illustrates the circuit showing the body diode and the PBJT.



NOTES:

The shaded area represents the charge, Q_{rr} , accumulated in the body diode pn junction.

T_{rr} , the reverse recovery time, is from t_2 to t_4 .

Q_{rr} and T_{rr} tend to increase with forward current and with junction temperature.

Figure 5. Timing Relationships— Reverse Recovery Current

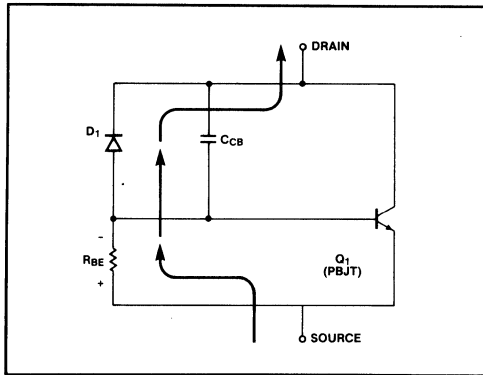


Figure 6. Freewheeling Stage

During the freewheeling stage, the current flows through the body diode in a forward sense (I_s). It is during this time that the body diode junction establishes a stored charge, Q_m , in junction capacitance C_{cb} . When Q1 is turned on, the current at first ramps down (di/dt) in the body diode, passes through zero, reverses direction as it heads up in magnitude, to a maximum of I_{sm} . Note that when it passes through zero, the voltage drop across R_{be} reverses polarity (Figure 7). Once again, based upon a combination of the above variables, if the voltage across R_{be} is sufficient to forward bias the PBJT, the MOSFET will fail.

The reverse recovery time of the body diodes is influenced by the amount of forward current. As forward current increases, the charge gradient stored in the depletion region increases. Temperature has an effect on charge storage as well. As temperature increases, stored charge and reverse recovery times all increase.

STATIC dv/dt —MODE 3

Static dv/dt can theoretically occur whenever there is more than one fast switching power device in the circuit. Recalling that ruggedness stresses occur in the off stage, the active device would be the source of stress on the static device.

Characterized by displacement current through C_{cb} (Figure 8), as voltage slews (dv/dt) at the drain, a current is induced through C_{cb} :

$$i = C_{cb} \cdot dv_{ds}/dt.$$

For any given MOSFET cell structure, there exists a current level, generated in this fashion, that will create a voltage across R_{be} greater than approximately 0.7 Volts, a deadly situation for a power MOSFET.

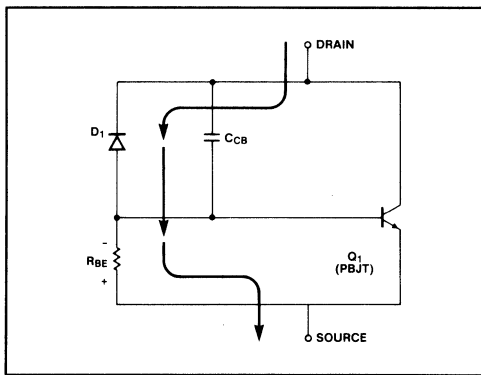


Figure 7. Reverse Recovery Current

An empirically based equation for Samsung SFETs operating at a T_j of 100 deg. C, can be approximated by:

$$V_{ds}/ns = .35V_{ds} + 10$$

where ns = nanoseconds, and V_{ds} = breakdown voltage rating of the SFET.

Example:

Samsung device IRF320

$$V_{dss} = 400 \text{ Volts}$$

$$v_{ds}/ns = (.35 \cdot 400) + 10 = 150 \text{ volts/ns}$$

Note that the switching speeds required to cause this type of failure are extremely fast, and are not normally seen in practical switching applications. Therefore,

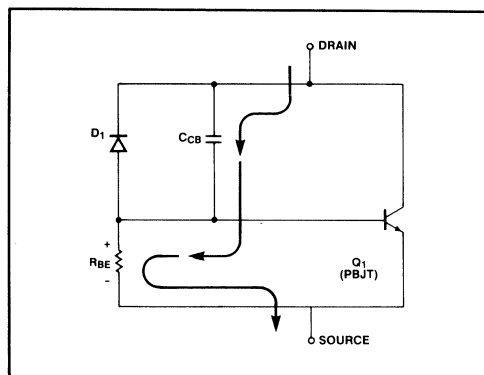


Figure 8. Typical MOSFET Circuit Showing Displacement Current through C_{cb}

although initially thought to be the primary failure mode, this type of failure is now one of theoretical interest, rather than practical concern. For this reason, the balance of the application note is limited to a discussion of Mode 1 and Mode 2 failures only.

PART 2—RUGGEDNESS TESTING INTRODUCTION

At the time of writing, power semiconductor manufacturers have not officially adopted a set of Ruggedness Test Standards. There is still much discussion about what should be tested, how it should be tested, and what the resulting test data mean. The forum for this dialog is the JEDEC, JC-25 Committee.

Two tests seem to be gaining acceptance however:

- Unclamped Inductive Switching (UIS);
- Diode recovery dv/dt.

The tests establish screening levels and design limitations for Mode 1 and Mode 2 stresses. The following sections discuss these important tests in detail, and list test data for some representative Samsung SFETS.

UNCLAMPED INDUCTIVE SWITCHING (UIS) TEST METHOD

Purpose

UIS testing was conceived as a method for setting the parameters for safe avalanche energy stress levels. The test records the level of energy (E_{ab}) and the peak current (I_a) that the device under test (DUT) can withstand without failing.

Early use of this test placed an emphasis on the energy capability of the device. However, because it was determined that the test was not related very strongly to inductance, the idea of energy capability was dropped in favor of unclamped inductive switching (UIS). This notion was supported by research at the National Bureau of Standards by D. Blackburn (Reference No. 1).

Test Description

The test circuit (Figure 9a) consists simply of a power source (V_{dd}), inductor (L), and the MOSFET being tested, referred to as the device under test (DUT). The waveforms shown in Figure 9b, reveal the dynamics of the test.

A pulse (V_g) applied to the gate of the DUT turns the device on for a predetermined time. With the device on, drain current ramps up to test current level (I_p). When V_g returns to zero, the channel resistance in

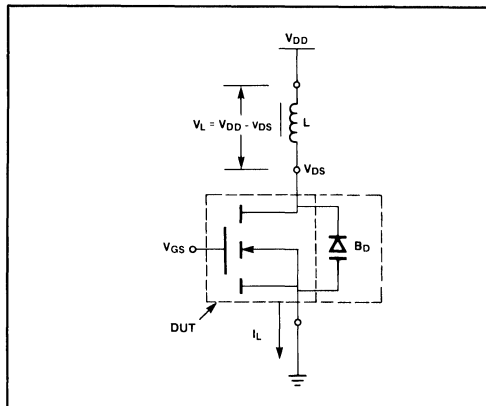


Figure 9a. UIS Test Circuit

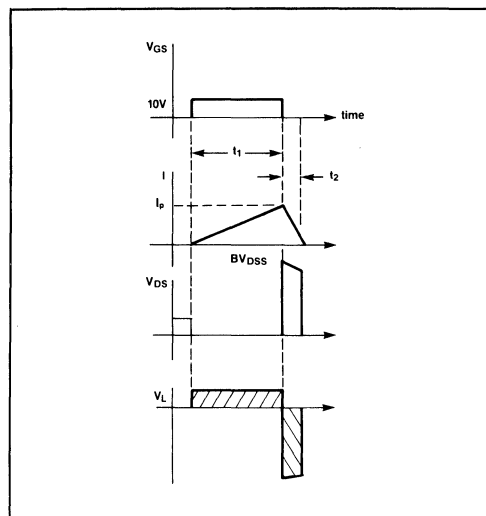


Figure 9b. UIS Test Timing Dynamics

the DUT jumps in a step fashion to a very high level, causing a flyback voltage effect on the inductor. The flyback voltage is limited by the breakdown voltage of the body diode thus clamping the voltage across the inductor. The time in avalanche is set by the inductor, as the volt seconds of the applied voltage must be balanced by the volt seconds in reset. That is:

$$V_L \cdot t_1 = (BV_{DS} - V_{DD}) \cdot t_2$$

DESIGN RELIABILITY

Table 1. UIS Test Parameters

Parameters	Symbols		Units
	Single	Repetitive	
Avalanche Current	I_{as}	I_{ar}	Amperes
Avalanche Energy	E_{as}	E_{ar}	Millihenries
Source Voltage	V_{dd}	V_{dd}	Volts
Junction Temperature	T_j (max)	T_j (max)	Degrees Centigrade

The test may be done as a single event or repetitively. The parameters used in specifying the UIS test method are shown in Table 1.

Figure 10 shows seven devices that were stressed to current levels just shy of avalanche failure. Increasing only the inductance, thus increasing the energy, did not cause the devices to fail initially. For example, a device tested with a $100\mu\text{h}$ inductor had a failure threshold of four amperes. Taking the same MOSFET and testing with a $500\mu\text{h}$ inductor showed that the device still had a failure threshold of four amperes indicating that the critical parameter is avalanche current (I_a) and not energy (E_{as}). Continued increases in the inductance eventually led to failure at the four ampere level, but this was caused by increased junction temperature, owing to extended time in avalanche.

The influence of junction temperature on UIS testing is profound. Increases in R_{be} and decreases in V_{be} tend to reduce the turn on immunity of the PBJT (1).

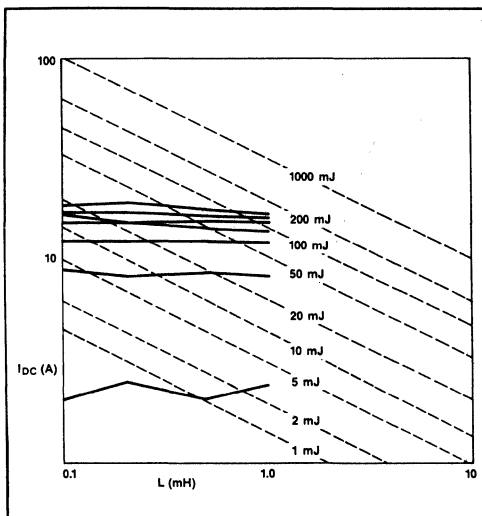


Figure 10. Comparative Avalanche Failure Thresholds

Acknowledgements to D. Blackburn

Figure 11 shows the results of data collected on four devices that were stressed to a point just shy of destructive avalanche. Establishing a baseline at a junction temperature of 25 degrees Centigrade for critical avalanche current, we observed that as the junction temperature increased, the critical avalanche current level went down.

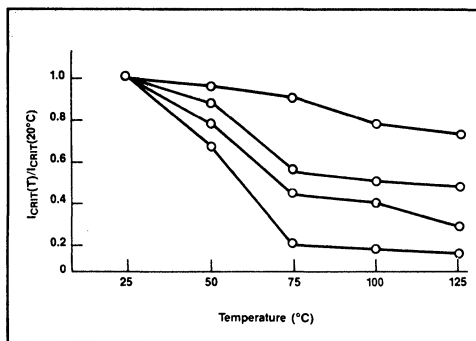


Figure 11. Comparative Avalanche Failure Test Data

Test Data

Data collected from extensive UIS testing of Samsung's MOSFETs establishes the dynamic safe operating area of the devices for Mode 1 stresses.

Conclusions

The conclusion to be drawn from UIS testing is that avalanche energy injection failure is a function of *peak current* and *junction temperature*, and not a direct function of inductance or energy, as was originally thought. Inductance does influence avalanche energy capability, in that it increases junction temperature because of the longer reset time required for higher inductances.

DIODE RECOVERY dv/dt TEST METHOD

Purpose

The diode recovery dv/dt test method is aimed at characterizing the MOSFET's ability to withstand Mode 2 dynamic electrical stresses. As with the UIS test method, the official details of the test are still to be ironed out by the JEDEC, JC-25 Committee, but the essential features as described below are gaining acceptance.

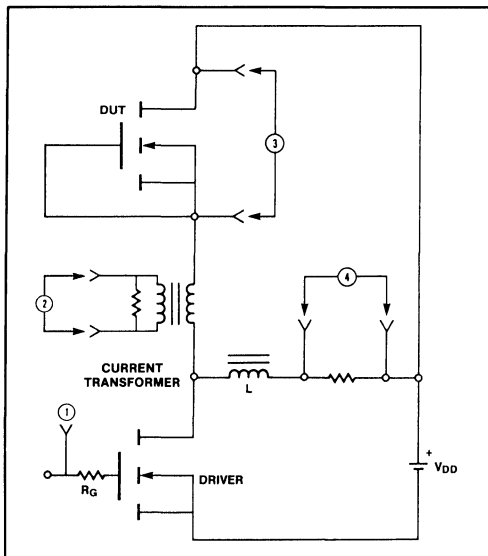


Figure 12. Diode Recovery dv/dt Test Circuit

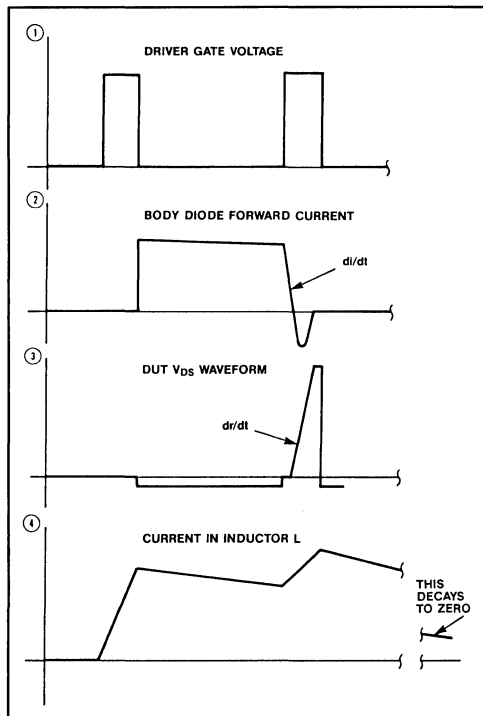


Figure 13. Timing Relationships for dv/dt Test

Test Description

The test circuit shown in Figure 12 is very straightforward. Using a 10 Volt power supply, two pulses (Figure 13) of preset duration and spaced at preset time intervals are applied to the gate of the driver MOSFET. The first pulse lays the ground work for application of Mode 2 stress by establishing current in the inductor to a specified peak level. During the delays between pulses the current commutates from the driver to the body diode of the DUT, and allows charge in the junction of the body diode to reach equilibrium. Application of the second pulse then establishes the reverse recovery dv/dt stress.

The forward current on the DUT body diode, I_{SD} , is controlled by the duty cycle of the PWM. The duty cycle is defined by the ratio of 'on' time divided by the 'on + off' time. Temperature is independently controlled by external ambient regulation. Table 3 summarizes the test parameters.

DESIGN RELIABILITY

Table 3. Diode Recovery dv/dt Test Parameters

Symbol	Name	Unit	Comments
dv/dt	dv/dt	volts/ns	Peak dv/dt applies to drain
di/dt	di/dt	amps/us	
I _s	Body diode forward conductive test current.	Amps	Usually set at DC current rating of MOSFET drain current.
T _j	Junction temperature	°C	Usually set at a maximum junction temperature.

Test Data

A large sample of Samsung's MOSFETs was tested using this method, and the data collected establishes the 'safe' level of Mode 2 stress that can be applied to these devices. Table 4 provides a summary of the data.

Table 4. Samsung's SFET Diode Recovery dv/dt Ratings

Device	Peak dv/dt V/ns	di/dt A/us	I _{sd} A	T _j deg. C
IRF510	5.4	80	5.6	150
IRF710	4.2	45	2.0	150
IRF520	5.5	120	9.2	150
IRF720	3.7	60	3.3	150
IRF820	3.7	55	2.5	150
IRF530	5.8	145	14.0	150
IRF730	4.2	95	5.5	150
IRF830	3.4	80	4.5	150
IRF540	5.3	165	28.0	150
IRF740	4.3	115	10.0	150
IRF840	3.7	95	8.0	150
IRF450	3.2	135	13.0	150
IRF640	5.0	150	18.0	150

Conclusions

There are four application variables that can contribute to Mode 2 MOSFET failure: di/dt, dv/dt, t_j and I_{sd}. This test establishes upper boundaries that must be applied simultaneously to the MOSFET to eliminate fear of turning on the PBJT.

The crucial parameter, dv/dt, is controlled by the gate driver resistor, R_g. Although it appears in Figure 13 as a constant, close observation on the oscilloscope reveals that it is not. The peak dv/dt value is the measurement of most interest and this occurs approximately midway in the switching interval.

The circuit layout considerations are more critical for this test than for the UIS test, making the method test-set sensitive. Important design and layout considerations are:

- Keep stray inductance to a minimum.
- Use ground plane.
- Keep leakage inductance very low for the current transformer.

PART 3—APPLICATIONS INTRODUCTION

The design engineer's goal when using MOSFET devices, is to design the devices into a circuit in such a way that ruggedness related failures are eliminated. This section provides representative application examples, from which the engineer can extrapolate to solve specific design problems.

Before we start, we should review some major simplifying assumptions associated with MOSFET ruggedness failure mechanisms:

- Such failures occur only in switch-mode applications.
- They occur only when the device channel is in the off or blocking state.
- We are concerned only with Mode 1 and Mode 2 stresses.
- Only one type of stress (Mode 1 or Mode 2) will be significant in any one application.

APPLICATION #1—FLYBACK POWER SUPPLY

Transformer leakage inductance combined with primary switching current form a reservoir of energy that must go somewhere when it is released. For a flyback design, this means that the MOSFET will absorb this energy unless some snubbing or clamping circuit is added. Absorption will occur on every cycle. In some applications, depending on the peak current and the magnitude of the leakage inductance, the MOSFET, if sufficiently rugged, may absorb all the avalanche energy. This is because, as was pointed out earlier,

DESIGN RELIABILITY

Mode 1 capability is based on peak current and junction temperature. Beyond this, no destructive mechanism is involved.

The flyback power supply (discontinuous mode), and its switching waveforms, are shown in Figures 14 and 15. L_p is the primary inductance, while L_1 is the leakage inductance.

The stress that may cause failure occurs during turn-off. As described in the UIS test method, when a MOSFET switches from on to off, the gate does not have control of the drain current. The electrical inertia of the inductor makes it look like a constant current source. The gate does, however, have control of the channel impedance, and, as the gate voltage goes down and the channel impedance skyrockets, there is an immediate and rapid change of voltage across the MOSFET. As the voltage goes up, energy is taken from the inductive load and dissipated in the MOSFET. The rate of energy absorption determines the rate of change of current, setting the voltage across the inductor.

This voltage is a snubberless, clampless, flyback circuit, does not go unbounded, as the body diode will avalanche at BV_{DSS} . If the energy and the temperature of the device are low enough, there may be no need for additional energy absorbing circuitry.

Figure 16 shows what the load line looks like for a naked (no snubber) MOSFET in a flyback circuit. Turn on (path abc) is benign. Turn off (path cdea) forces the MOSFET outside the DC safe operating area, as it absorbs the magnetic energy stored in the leakage inductance of the transformer. The cross-hatched area is the energy absorbed by the MOSFET.

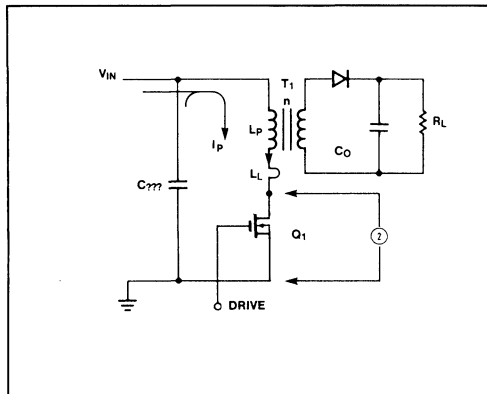


Figure 14. Flyback Power Supply Circuit

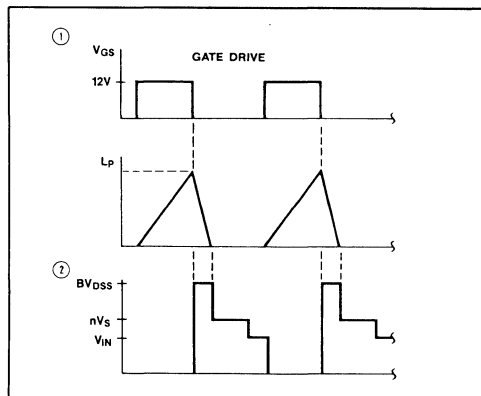


Figure 15. Timing Relationships for Power Supply Circuit

Example for Flyback Power Supply

Application Parameters

(L_{el})	Primary Leakage Inductance	50 μ Hz
(I_p)	Peak Avalanche Current	2 Amps
(D_c)	Maximum Duty Cycle	.2
(f)	Switching Frequency	100 KHz
(V_d)	Input DC Rail Voltage	200 V
(T_c)	Heat Sink Temperature	60 deg. max.

Selected MOSFET—IRF820 Specifications

DC Ratings		Ruggedness Ratings	
BV_{DSS}	500 V	E_{AS}	210 mJ
$R_{ds(on)}$	3 Ω	I_{AS}	2.5 A
I_d	2.5A	L	17 mhy...
$R_{\theta jc}$	3.12 $^{\circ}$ C/W	T_J	100 $^{\circ}$ C

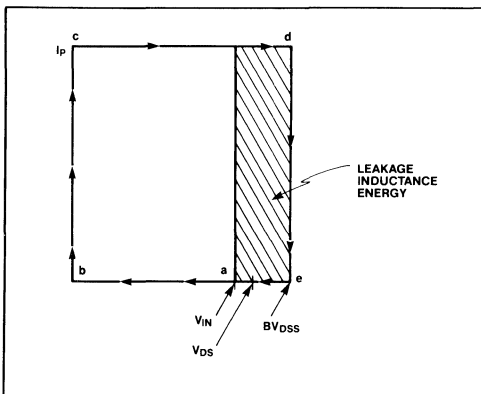


Figure 16. Load Line for MOSFET in a Flyback Circuit

DESIGN RELIABILITY

When comparing the application parameters with the I_{ar} and Inductance ratings of the IRF820, we see that the IRF820 satisfies requirements in these two areas.

Calculating the E_{ar} Stress Level

$$\text{Repetitive Avalanche Energy} = \frac{1}{2} I_p^2 L \\ = \frac{1}{2} (2)^2 (50 \times 10^{-6}) = .1 \text{ mJ}$$

Again the IRF820 satisfies application requirements in terms of E_{ar} . The remaining task is to verify that the junction temperature is below 100°C.

Calculating Junction Temperature T_j

(1)

$$P_T = I_{RMS}^2 R_{DS(ON)} R_{DSN} + \text{Switching Losses} + \text{Avalanche Losses}$$

(2)

$$T_j = T_c + R_{\theta JC} P_T$$

Calculating I_{RMS}

$$I_{RMS} = I_{PK} \sqrt{\frac{T_o}{3T}} = 2 \sqrt{\frac{2}{(3)10}} = .51$$

Calculating $R_{DS(ON)}$ Losses

$$P_{RDS(ON)} = I_{RMS}^2 R_{DS(ON)} R_{DSN} = .8 R_{DSN}$$

Calculating Switching Losses

$$P_{SW} = \frac{V_{DS} (I_p \cdot t_{sw}) f}{2} \\ = \frac{200 (2) \cdot (.5 \times 10^{-6}) 10^5}{2} = 10 \text{ WATTS}$$

Calculating Avalanche Losses

$$P_A = \frac{1}{2} I_p^2 L f = \frac{1}{2} (50 \times 10^{-6}) 10^5 = 10 \text{ WATTS}$$

REWRITING EQUATIONS

(1')

$$P_T = .8 R_{DSN} + 20$$

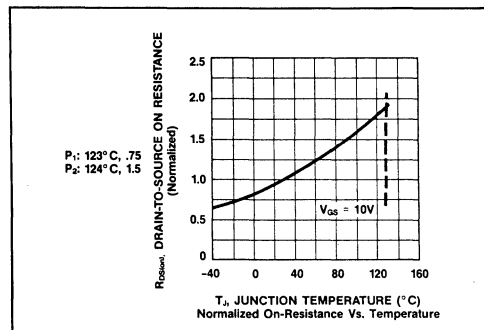
(2')

$$T_j = 60 + (3.12) (P_T)$$

Solving Equations (1') & (2') Graphically

Guess $R_{DSN} = .75$ Implies $T_j = 123^\circ\text{C}$

Guess $R_{DSN} = 1.5$ Implies $T_j = 124^\circ\text{C}$



There is no graphical solution. This implies an unstable thermal situation for the IRF820. We will upsize the MOSFET to an IRF830 and recalculate.

Selected MOSFET Specifications IRF830

DC Ratings		Ruggedness Ratings	
BV_{DS}	500 V	E_{AS}	280 mJ
$R_{DS} (on)$	1.5Ω	I_{AS}	4.5 A
I_d	4.5A	L	150 μhy
$R_{\theta JC}$	1.67°C/W	T_J	100 °C

Recalculate Equations (1') & (2')

(1')

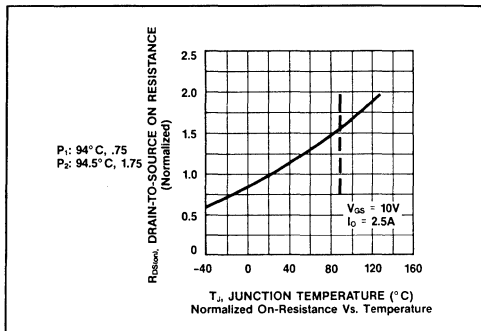
$$P_T = (.51)^2 (1.5) R_{DSN} + 20 = .39 R_{DSN} + 20$$

(2')

$$T_j = 60 + 1.67 (P_T)$$

Guess $R_{DSN} = .75$ Implies $T_j = 93.88^\circ\text{C}$

Guess $R_{DSN} = 1.75$ Implies $T_j = 94.5^\circ\text{C}$



Solution is $T_j = 94.4^\circ\text{C}$. This is a stable solution thermally as well as satisfying the ruggedness requirement that T_j be less than 100°C.

APPLICATION #2 — PUSH PULL POWER SUPPLY

Push-pull power supplies are very popular for high density power applications, owing to the favorable transformer utilization. Careful layout is important, as any stray inductances tend to extend the duty cycle to maintain power to the load.

A typical circuit is shown in Figure 17. Note that the stray inductances between the secondary transformer and the diodes are multiplied by the square of the turns ratio.

As in the case of the flyback, the stress consideration in this circuit involves the leakage inductance between the primary and secondary transformer windings. The MOSFET will not see the full impact of the energy stored in this inductance, since part of the energy is dumped back into the power source,

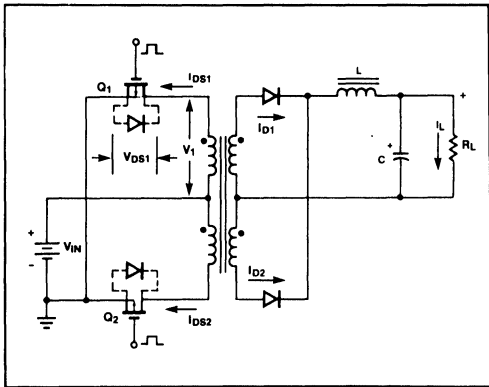


Figure 17. Push Pull Power Supply Circuit

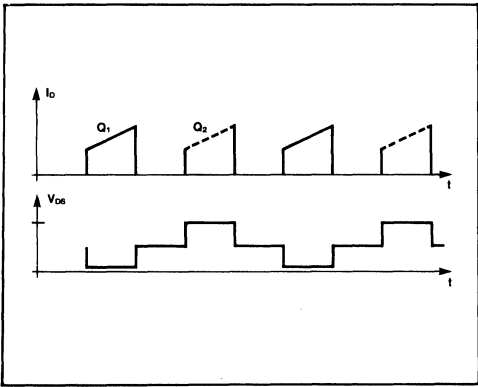
through the body diode of the second MOSFET. The energy absorbed, therefore is determined by the concatenation of first the leakage inductance from primary to secondary transformers, and then the leakage inductance between primary windings.

Assuming transistor Q2 is switching from on to off, the choke L in the secondary will swing one end to a diode drop below ground, thus shorting the secondary. The primary mutual inductance is thus shorted, leaving the MOSFETs to deal with the leakage inductance. If there is no coupling between primary windings, Q2 has to deal with the leakage inductance in the form of avalanche energy.

The bulk of the energy however is clamped by the body diode in Q1. Using the equation $V = L \times di/dt$, where V is input voltage, and knowing the leakage inductance (L), the time it takes for the energy to be removed, or in other words for the current to reach zero, can be approximated. To avoid diode recovery dv/dt problems, it is best to set a minimum dead time. Usually this is not a major issue, but is worthy of a look.

Example for Push Pull Power Supply
Application Parameters

(L δ ₂) Primary to Primary Leakage Inductance	= 10 μ hy.
(L δ ₁) Primary to Secondary Leakage Inductance	= 100 μ hy.
(I _p) Peak Primary Current	= 10 Amperes
(DC) Maximum Duty Cycle	= 45
(f) Switching Frequency	= 70 Khz.
(V _o) Input DC Rail Voltage	= 28 VDC
(T _c) Heat Sink Temperature	= 60°C max.



Selected MOSFET—IRF530 Specifications

DC Ratings		Ruggedness (Avalanche) Rating	
BV _{dss}	100 V	E _{AS}	69 mj
RDS _{con}	.18 Ω	I _{AS}	14 A
I _d	14A	T _j	100 °C
R δ _{jc}	1.67°C/W	L	60 μ hy

When comparing the application parameters with the I_{ar} and L ruggedness ratings of the IRF530, we see that the IRF530 satisfies requirements in these two areas.

Mode 2 Stress Consideration:

With a primary to secondary leakage inductance of 100 μ hy, and peak current of 10 amperes, the energy stored in the core is:

$$\frac{1}{2} I^2 L = \frac{1}{2} (10^2) (10^4) = 5mj$$

Calculating the E_{ar} Stress Level

This energy will be returned to the supply by virtue of the body diode of the alternate transistor. This MOSFET (with body diode conducting) will not suffer from diode recovery dv/dt since the next event turns this MOSFET on and thereby precludes Mode 2 stress. Therefore we only have to deal with Mode 1 stress.

Mode 1 Stress Consideration

With peak current of 10 amps, the leakage inductance (primary to primary) of 10 μ hy, the IRF530 is adequate. We must only verify that the junction temperature is below 100° C.

Calculating Junction Temperature T_j

(1)

$$P_T = I_{RMS}^2 R_{DS(on)} + \frac{R_{DSN}}{\text{Switching Losses}}$$

(2)

$$T_j = T_c + R_{\delta jc} P_T$$

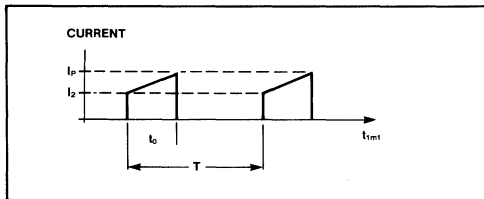
DESIGN RELIABILITY

Referring to figure below, we can calculate the RMS current of the pulsed primary waveform as follows:

Calculating I_{RMS} for Primary Current

$$I_{RMS} = \sqrt{\left(I_{PK}^2 - I_{PK} I_2 + \frac{I_2^2}{3} \right) \frac{T_o}{T}}$$

$$\sqrt{\left(10^2 - 10(8) + \frac{(8)^2}{3} \right) \frac{.45}{1}} = 4.31 \text{ Amps}$$



Assuming a clamped inductive switching waveform of turn-on and turn-off times of 500×10^{-9} seconds, we can calculate the switching losses,

Calculating the Switching Losses

$$P_{SW} = \frac{V_{DS} I_D (ts_1 + ts_2) fs}{6}$$

$$= \frac{(28) (10) (.5+.5) (10^{-6}) (70 \times 10^3)}{6}$$

$$= 3.2 \text{ Watts}$$

Substituting into the above equations, we have,

(1')

$$P_T = (4.31)^2 (.18) R_{DSN} + 3.2$$

(2')

$$T_J = 60 + 1.62 (P_T)$$

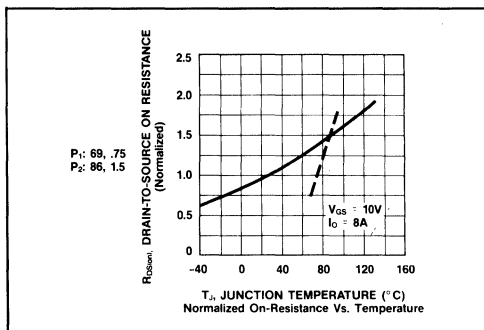
Combining equations,

$$T_J = 60 + 1.62 [(4.31)^2 (.18) R_{DSN} + 3.2]$$

$$= 65.18 + 5.41 R_{DSN}$$

$$\text{Guess } R_{DSN} = .75 \text{ Implies } T_J = 69^\circ \text{C}$$

$$\text{Guess } R_{DSN} = 1.5 \text{ Implies } T_J = 86^\circ \text{C}$$



Plotting these two points shows the device to be operating at a junction temperature of approximately 85°C , therefore from a ruggedness point of view, snubbers are not required.

APPLICATION #3—BUCK REGULATOR

Figure 18 shows a simplified schematic of a buck regulator. This particular topology raises no ruggedness issues for the circuit designer.

There is no exposure to Mode 1 stress, since the switching MOSFET is not working into the primary of an isolation transformer, and there is thus no leakage inductance.

Mode 2 stress need not be a concern, since the body diode of the MOSFET does not conduct over the switching cycle.

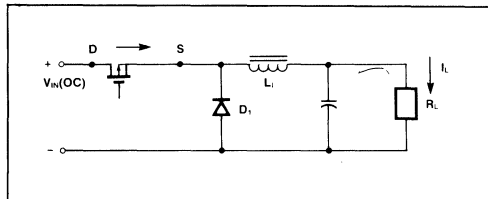


Figure 18. Buck Regulator Circuit

APPLICATION #4 — SWITCHMODE MOTOR CONTROL

The most popular circuit architecture for switchmode motor control is the H-Bridge driver shown in Figure 19. This surprisingly simple circuit is capable of converting a ground-referenced DC source to a polarity-reversing voltage driver as required for either DC or AC motor control. Peak output voltage is limited by the DC rail, less the voltage drop through the bridge. Switching frequencies can vary, but with trends toward lower armature inductances, high frequencies, e.g. 100 kHz, are commonplace.

For switchmode motor control, we must consider dv/dt stress. Relative to the switching time of a PWM cycle, the motor current looks like a constant current source requiring a path during the off (freewheeling) power phase. Unless additional circuitry is added, this path will include the MOSFET body diode, as discussed in Part 1, when the complementary MOSFET is subject to the "reverse recovery dv/dt ," dynamic stress.

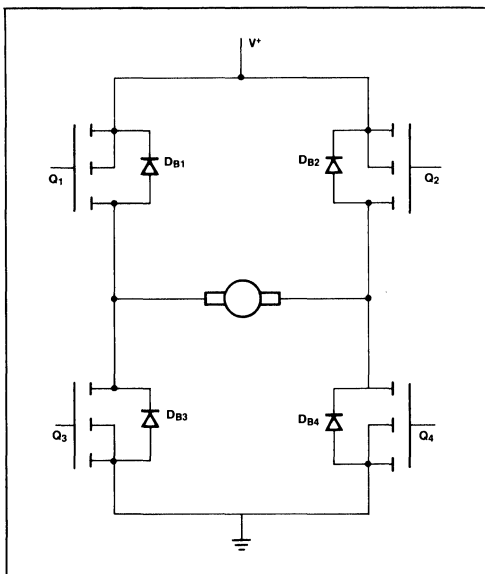


Figure 19. H-Bridge Driver Circuit

Diode recovery dv/dt is a multi-dimensional problem, difficult to characterize for design optimization. Data is available, however, to ensure safe operation by defining the upper limits of the Mode 2 stress parameters. The key parameters with which we must comply to make sure that the PBJT will not be activated during the reverse recovery phase are:

Parameter #1: T_j

This is the junction temperature of the MOSFET. It is controlled by the ambient temperature, heatsinking, and internal power dissipation (gate losses, leakage losses, switching losses, R_{ds} (on) losses, and body diode losses). Determining T_j is a straight-forward calculation.

Parameter #2: di/dt

This is the rate of change of current in the body diode as it goes from forward conduction to reverse conduction. It is influenced by temperature, forward current, circuit inductances and by the turn-on characteristics of the complementary transistor. This is not easily calculated and thus requires circuit measurement and experimentation.

Parameter #3: dv/dt

This is the peak rate of change of voltage across the MOSFET as it recovers from peak reverse current. Similar to di/dt , this parameter requires measurement and experimentation.

Parameter #4: I_{sd}

This is the body diode current during the free-wheeling phase. It is easy to determine, as this is set by the peak load current in the motor or inductor.

EXAMPLE OF MOTOR CONTROL APPLICATION

The example describes the design of H-Bridge motor drives for a .4 KVA motor load, working from a DC rail of 140 volts. The case temperature will be 50°C maximum. Figure 19 shows the H-Bridge driver circuit. Assume a unipolar, PWM drive working at a frequency of 40 kHz, as shown in Figure 20. Because of the 28 ampere peak requirement for the body diode, we will require two devices in parallel. To determine the junction temperature we must calculate the following:

Application Parameters

(I_p)	Peak Motor Current	28 Amperes
(V_d)	Input DC Rail Voltage	140 Vdc
(T_c)	Case Temperature (max)	50°C
(DC)	Maximum Duty Cycle	.71
(fs)	Switching Frequency	40 kHz
(di/dt)	Diode Commutation Rate	to be measured
(do/dt)	Maximum Rate of Change of Drain Voltage	to be measured
(I_{sd})	Body Diode Current (max)	28 Amperes

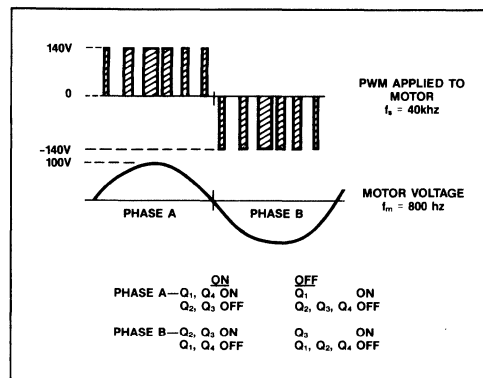


Figure 20. Example of PWM Drive

Because of the 28 Ampere peak requirement for the body diode, we will require two devices in parallel.

Selected MOSFET(s) SPECIFICATION IRF640

DC Ratings		Ruggedness Reverse Recovery du/dt Rating	
V_{ds}	200 V	dv/dt	5 V/ns
R_{DS} (on)	.18Ω	I_{sd}	18 A
I_d	18A	di/dt	150 A/μs
$R_{θJC}$	1°C/W	$T_{J(MAX)}$	150°C

Calculating Junction Temperature T_J

(1)

$$P_T = I_{RMS}^2 R_{DS(ON)} + \text{Body Diode Losses} + \text{Switching Losses}$$

(2)

$$T_J = T_c + R_{\theta JC} [P_T]$$

where:

$$I_{RMS} = \left(\frac{28}{2} \right) \left(\frac{1}{\sqrt{2}} \right) \left(\frac{1}{2} \right) = 4.9 \text{ Amperes}$$

$$R_{DS(ON)} = .12 \Omega$$

Calculating Body Diode Losses

$$P_{BD} = I_{RMS} (V_{SD}) = 4.9 (1.5) = 7.42 \text{ WATTS}$$

Assuming a clamped inductive load type switching (figure 21.), we can calculate the switching losses.

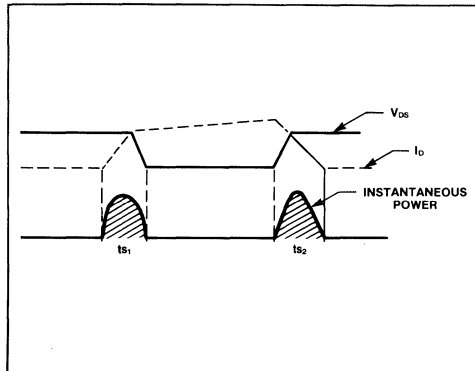


Figure 21. Clamped Inductive Load Switching

Calculating the Switching Losses

$$P_{SW} = \frac{V_{DS} (I_{D1} t_{s1} + I_{D2} t_{s2}) f_s}{2}$$

$$= \frac{(140) (14) (300 \cdot 10^{-9}) (40 \cdot 10^3)}{2}$$

$$= 14 \text{ WATTS}$$

Substituting into above equations, we have,

(1)

$$P_T = (4.9)^2 (.12) R_{DSN} + 7.42 + 14$$

(2')

$$T_J = 50 + (1) P_T$$

Combining equations,

$$T_J = 50 + (4.9)^2 (.12) R_{DSN} + 21.42 = 71.42 + 2.88 R_{DSN}$$

Solving graphically by using the R_{DSN} curve for the IRF640

Guess $R_{DSN} = .75$ Implies $T_J = 73^\circ \text{C}$

Guess $R_{DSN} = 1.5$ Implies $T_J = 75^\circ \text{C}$

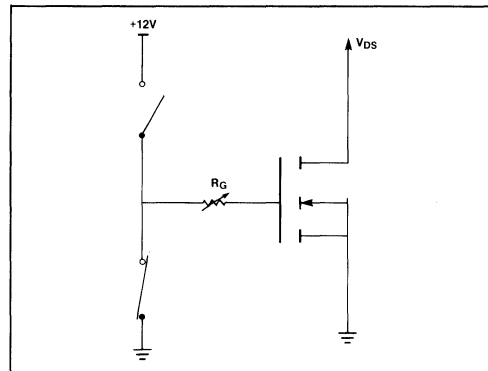
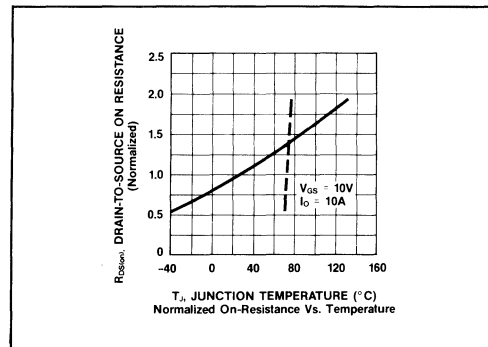


Figure 22. Gate Drive Control

Therefore worst case T_J is approximately 74°C . Thus the junction temperature complies with the ruggedness rating of the MOSFET.

Therefore junction temperature is in a safe and stable zone. In addition, I_{SD} is within the Mode 2 stress limits for the IRF640. The remaining task is to measure di/dt and dv/dt to ensure compliance.

If the dv/dt is measured to be greater than $5v/ns$, it must be reduced. The most straightforward method for reducing the dv/dt is to add series resistance in the gate drive circuit as shown in Figure 22. Proper operation of the H-Bridge requires good electrical symmetry. Therefore as resistance is added to one leg, the same resistance should be added to the other legs. The penalty for slowing the switching speeds is higher losses. Therefore a recheck of switching losses should be examined.

Once the dv/dt level has been adjusted to less than $5v/ns$, the di/dt specification limit of $150 A/ns$ should be checked. If found to be too high, it too can be reduced by adding more gate resistance. If this is not satisfactory because of excessive switching losses, some small inductance (100-400 nhy) could be added to the source connection.

APPENDIX A RUGGEDIZING THE MOSFET

Producing a rugged MOSFET device is a function of:

- Device design;
- Manufacturing techniques;
- Device testing techniques.

DESIGN

In the design cycle, there are several factors that go into making a rugged device. The most important of these is the minimization of R_{be} . In Figure A1, we

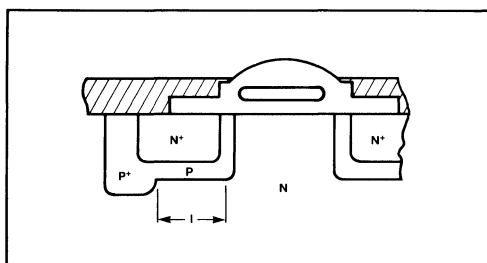


Figure A1. Cross Section of a Ruggedized MOSFET Cell

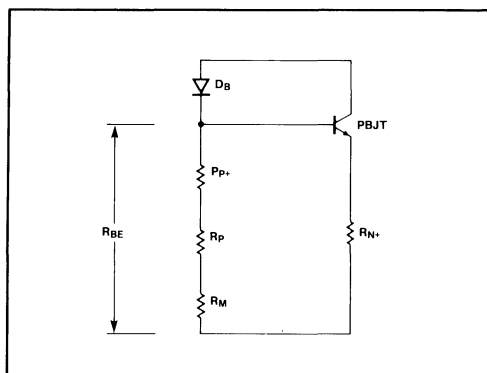


Figure A2. PBJT Base Emitter Circuit

show a cross section of a partial cell. The cross-hatched area represents the source metalization. The body region in this N-channel MOSFET is P doped. The P+ indicates a higher doping concentration and therefore higher conductivity. The N+ region, which forms the emitter region of the PBJT and also serves as part of the MOSFET channel, is shorted to the body region by source metalization.

Looking at the various materials in the cell, we can partition the PBJT base emitter circuit into a number of different resistors, as shown in Figure A2. R_m , the metalization resistance, is negligible, and therefore not important. R_{p+} , on the other hand is one of the major improvements in ruggedization. This reduces R_{be} substantially, and adds an order of magnitude to the ruggedness of the MOSFETs. R_p is determined by the resistivity of the material, the length 'l' of the cell, the thickness and width of the P part of the body region. Increased cell density tends to reduce l and therefore reduce R_p .

Although the resistance of R_{n+} does not affect the point at which the PBJT turns on, increasing the value of R_{n+} introduces feedback into the base circuit, tending to lower the gain of the PBJT circuit. There may be situations where this may prevent catastrophic failures. Increasing R_{n+} has a price, as R_{ds} (on) increases proportionately. Therefore, this is another optimization process on the part of the MOSFET manufacturer.

The deep P+ well has an influence on ruggedness. Since it is heavily doped, the depletion regions are not as deep as those associated with the P region. This tends to make the body diode avalanche, in contrast to the collector base junction of the PBJT.

To improve the reverse recovery time characteristics of the MOSFET, the manufacturer of the device must decide on the resistivity levels of the p and n material. As the resistivity is increased, there is a tendency towards lower stored charge (Q_{rr}) levels, and reduced recovery time. These factors have to be carefully evaluated as the price for these improvements is increased R_{ds} (on) as well as R_{be} .

MANUFACTURING

Good process control and techniques are as important to the ruggedization process as good design. If the manufacturing process is flawed, one weak cell out of the thousands in the component, can render the entire chip weak. Thus poor mask alignment, with the resulting lack of cell definition can offset the optimized cell design. Similarly, doping levels must be

consistently controlled over the entire active area of the chip, or temperature gradients will develop, causing local hot spots.

Samsung's SFETs are now in the fourth generation HDMOS technology. This exclusive HDMOS process employs CMOS local oxidaton and ion implantation techniques to minimize these concerns and provide higher wafer yields.

TESTING

Samsung Semiconductor uses UIS testing on all MOSFETs. This rigorous screening for ruggedness, ensures that devices likely to cause user problems in the system design phases are weeded out before they can hit the field.

APPENDIX B— LIST OF ABBREVIATIONS

BD	Body Diode
BV _{ceo}	Bipolar transistor breakdown voltage with base open
BV _{ces}	Bipolar transistor breakdown voltage with base shorted.
V _{dss}	Maximum DC drain-to-source voltage
BV _{dss}	Drain-to-source breakdown voltage
CSOA	Commutating Safe Operating Area
C _{cb}	Collector to base junction capacitance
DUT	Device Under Test
E _{ar}	Repetitive avalanche energy
E _{as}	Single pulse avalanche energy
I	Current
I _{ar}	Avalanche Current
I _{des}	Zero gate voltage drain current
I _s	Body diode forward current rating
I _{sm}	Peak diode peak reverse recovery current
JEDEC	Joint Electronic Device Engineering Council
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PBJT	Parasitic Bipolar Junction Transistor
PWM	Pulse Width Modulator
Q _{rr}	Reverse recovery charge
R _{be}	Base spreading resistance
SOA	Safe Operating Area
T _j	Junction temperature
UIS	Unclamped Inductive Switching
VDMOS	Vertical double diffused MOSFET
V _{ds}	Voltage drain-to-source
di/dt	Rate of change of drain current
dv/dt	Rate of change of drain voltage
mj	Millijoule
n	Negatively doped
p	Positively doped

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PWM Control IC

Application Note

INTRODUCTION

The KA34063A is a monolithic switching regulator subsystem consisting of many active building blocks necessary for use as dc to dc converters. It represents a significant advancement in the ease of implementing highly efficient and yet simple switching power supplies.

THE LINEAR POWER SUPPLY Vs THE SWITCHING POWER SUPPLY

The linear power supply is already a mature technology, which has been used since the dawn of electronics. Whether this type of power supply incorporates tubes or semiconductors, its construction and operation are essentially the same.

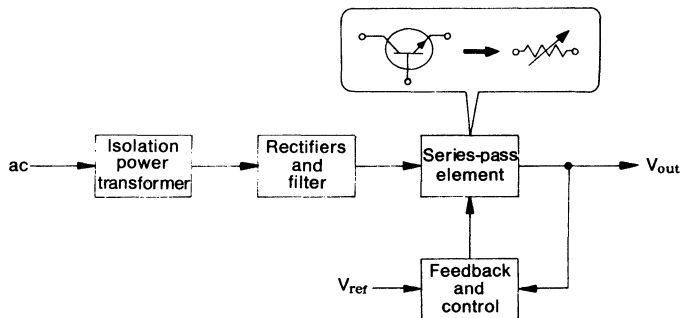


FIGURE 1—1 Block diagram of a series-pass regulated linear power supply

Fig. 1-1 shows the simplified block diagram of a series pass linear regulated power supply. In this type of power supply, a low frequency, 50 or 60Hz transformer is used to step down the ac mains to a lower voltage of the same frequency. This secondary voltage is in turn rectified and filtered, and the resulting dc is fed into a series-pass active element.

By sampling a portion of the output and comparing it to a fixed reference voltage, the series-pass element is used as a form of "variable resistor" to control and regulate the output voltage. However, this mode of operation dissipates a large amount of power in the form of heat, consequently lowering the efficiency of the power supply to 40 or 50 percent. Although the linear power supply in general has a tight regulation band along with very low output noise and ripple, the disadvantages are obvious. As we mentioned, because of its low efficiency, usually bulky and expensive heat sinks and cooling fans are needed, and large isolation power transformers are used to step down the ac input voltage. Hence, this type of power supply tends to be bulky, heavy, and almost unfit for today's compact electronic systems. Other disadvantages of the linear power supply are its relatively narrow input voltage range, normally ± 10 percent, and its very low output hold up time, about 1ms.

The disadvantages of the linear power supply are greatly reduced or eliminated by the regulated switching power supply.

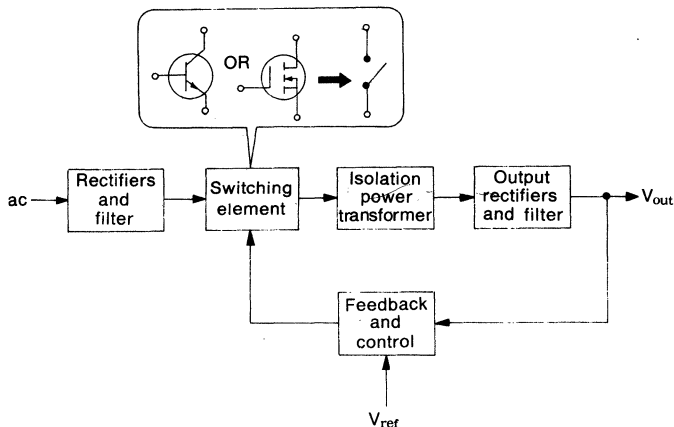


FIGURE 1—2 The basic off-the-line switching regulated power supply.

Fig 1-2 shows a simplified block diagram of a high-frequency off-the line switching power supply. In this scheme, the ac line is directly rectified and filtered to produce a raw high-voltage dc, which in turn is fed into a switching element. The switch is operating at the high frequencies of 20KHz to 1MHz, chopping the dc voltage into a high-frequency square wave. This square wave is fed into the power isolation transformer, stepped down to a predetermined value and then rectified and filtered to produce the required dc output. A portion of this output is monitored and compared against a fixed reference voltage, and the error signal is used to control the on-off times of the switch, thus regulating the output. Since the switch is either on or off, it is dissipating very little energy, resulting in a very high overall power supply efficiency of about 70 to 80 percent. Another advantage is the power transformer size which can be quite small due to high operation frequency. Hence the combination of high efficiency (i.e, no large heat sinks) and relatively small magnetics, results in compact, lightweight power supplies. Coupled with very wide input voltage range, 90 to 260Vac, and very good hold-up time, typically 25ms, the switcher has become the choice for electronic system designers. Of course, there are certain disadvantages associated with the switching power supply, such as higher output noise and ripple, EMI/RFI generation, and higher design complexity. However, with careful design these problems may be greatly reduced or eliminated.

OPERATION PRINCIPAL OF DC to DC CONVERTER

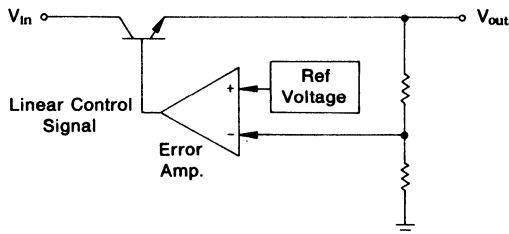


FIGURE 2—1 Step-Down Linear Regulator

In order to understand the difference in operation between linear and switching regulators we must compare the block diagrams of the two step-down regulators shown in Figure 2. The linear regulator consists of a stable reference, a high gain error amplifier, and a variable resistance series-pass element. The error amplifier monitors the output voltage level, compares it to the reference and generates a linear control signal that varies between two extremes, saturation and cutoff. This signal is used to vary the resistance of the series-pass element in a corrective fashion in order to maintain a constant output voltage under varying input voltage and output load conditions.

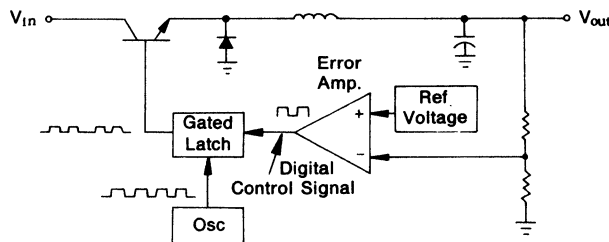


FIGURE 2—2 Step Down Switching Regulator

The switching regulator consists of a stable reference and a high gain error amplifier identical to that of the linear regulator. This system differs in that a free running oscillator and a gated latch have been added. The error amplifier again monitors the output voltage, compares it to the reference level and generates a control signal. If the output voltage is below nominal, the control signal will go to a high state and turn on the gate, thus allowing the oscillator clock pulses to drive the series-pass element alternately from cutoff to satu-

ration. This will continue until the output voltage is pumped up slightly above its nominal value. At this time, the control signal will go low and turn off the gate, termination any further switching of the series-pass element. The output voltage will eventually decrease to below nominal due to the presence of an external load, and will initiate the switching process again. The increase in conversion efficiency is primarily due to the operation of the series-pass element only in the saturated or cutoff state. The voltage drop across the element, when saturated, is small as is the dissipation. When in cutoff, the current through the element and likewise the power dissipation are also small. There are other variations of switching control. The most common are the fixed frequency pulse width modulator and the fixed on-time variable off-time types, where the on-off switching is uninterrupted and regulation is achieved by duty cycle control. Generally speaking, the example given in Figure 2-2 does apply to KA34063A.

GENERAL DESCRIPTION

The KA34063A is a monolithic switching regulator subsystem consisting of many active functions required for dc to dc converters. This device contains a temperature compensated bandgap reference, a dutycycle controlled oscillator with an active current limit circuit, a comparator and a high current output switch. The device was specifically designed to be incorporated in step-up, step-down and voltage-inverting converter application.

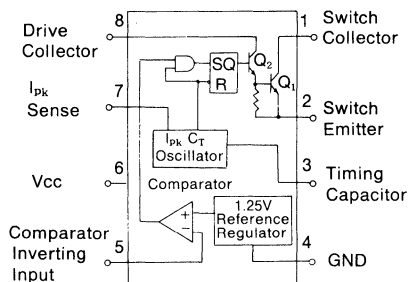


FIGURE 3 KA34063A Block Diagram

The oscillator is composed of a current source and sink which charges and discharges the external timing capacitor C_T between an upper and lower preset threshold. The typical charge and discharge currents are $33\mu A$ and $200\mu A$ respectively, yielding about a 1 to 6 ratio. Thus the ramp-up period is 6 times longer than that of the ramp-down as shown in Figure 4. The upper threshold is equal to the internal reference voltage 1.25 volts and the lower is approximately equal to 0.75V. The oscillator runs continuously at a rate controlled by the selected value of C_T .

During the ramp-up portion of the cycle, a Logic '1' is present at the 'A' input of the AND gate. If the output voltage of the switching regulator is below nominal, a Logic '1' will also be present at the 'B' input. This condition will set the latch and cause the 'Q' output to go

to a Logic '1', enabling the driver and output switch to conduct. When the oscillator reaches its upper threshold, C_T will start to discharge and Logic '0' will be present at the 'A' input of the AND gate. This logic level is also connected to an inverter whose output presents a Logic '1' to the reset input of the latch. This condition will cause 'Q' to go low, disabling the driver and output switch.

The output of the comparator can set the latch only during the ramp-up of C_T and can initiate a partial or full on-cycle of output switch conduction. Once the comparator has set the latch, it cannot reset it. The latch will remain set until C_T begins ramping down. Thus the comparator can initiate output switch conduction, but cannot terminate it and the latch is always reset when C_T begins ramping down. The comparator's output will be at a Logic '0' when the output voltage of the switching regulator is above nominal. Under these conditions, the comparator's output can inhibit a portion of the output switch on-cycle, a complete cycle, a complete cycle plus a portion of one cycle, multiple cycles, or multiple cycles plus a portion of one cycle.

Current limiting is accomplished by monitoring the voltage drop across an external sense resistor placed in series with V_{CC} and the output switch. The voltage drop developed across this resistor is monitored by the I_{pk} Sense pin. When this voltage becomes greater than 300 mV, the current limit circuitry provides an additional current path to charge the timing capacitor C_T . This causes it to rapidly reach the upper oscillator threshold, thereby shortening the time of output switch conduction and thus reducing the amount of energy stored in the inductor. This can be observed as an increase in the slope of the charging portion of the C_T voltage waveform as shown in Figure 5. Operation of the switching regulator in an overload or shorted condition will cause a very short but finite time of output conduction followed by either a normal or extended off-time interval provided by the oscillator ramp-down time of C_T . The extended interval is the result of charging C_T beyond the upper oscillator threshold by overdriving the current limit sense input. This can be caused by operating the switching regulator with a severely overloaded or shorted output or having the input voltage grossly above the nominal design value. Under extreme conditions, the voltage across C_T will approach V_{CC} and can cause a relatively long off-time. This action may be considered a feature since it will reduce the power dissipation of the output switch considerably.

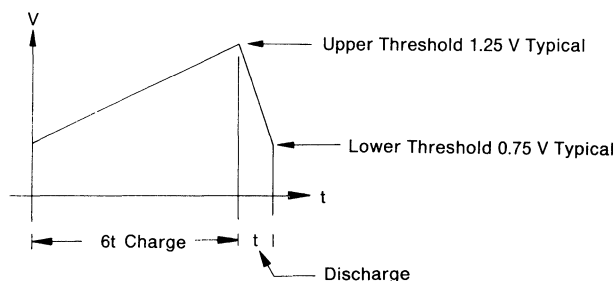


FIGURE 4 C_T Voltage Wave form

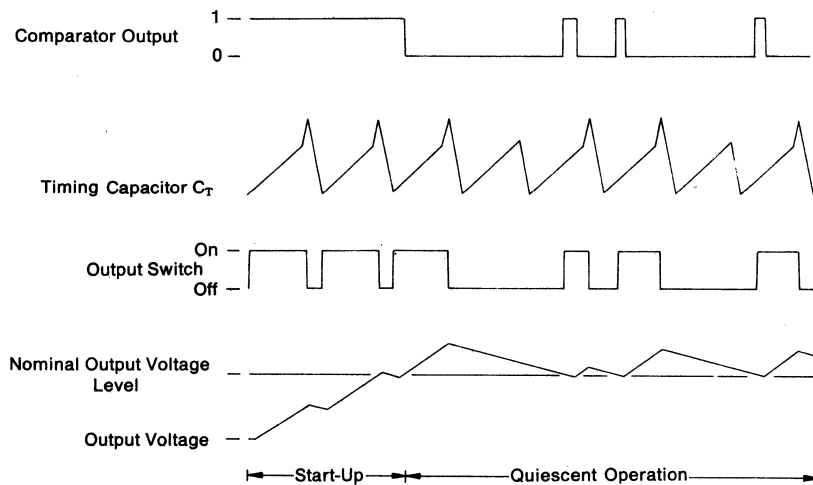


FIGURE 5 Typical Operating Waveforms

STEP-DOWN SWITCHING REGULATOR OPERATION

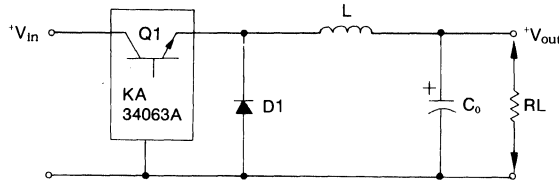


FIGURE 6 Step-Down Regulator ($V_{in} \leq V_{out}$)

Transistor Q_1 interrupts the input voltage and provides a variable duty cycle squarwave to a simple LC filter. The filter averages the squarwaves producing a dc output voltage that can be set to any level less than the input by controlling the percent conduction time of Q_1 to that of the total switching cycle time.

$$\text{Thus, } V_{out} = V_{in} \{t_{on} / (t_{on} + t_{off})\}$$

The KA34063A achieve regulation by varying the on-time and the total switching cycle time.

Assume that the transistor Q_1 is off, the inductor current I_L is zero, and the output voltage V_{out} is at its nominal value. The output voltage across capacitor C_0 will eventually decay below nominal because it is the only component supplying current into the external load R_L . This voltage deficiency is monitored by the switching control circuit and causes it to drive Q_1 into saturation. The inductor current will start to flow from V_{in} through Q_1 and, C_0 in parallel with R_L , and rise at a rate of $\Delta I / \Delta T = V/L$. The voltage across the inductor is equal to $V_{in} - V_{sat} - V_{out}$ and the peak current at any instant is:

$$I_L = \{(V_{in} - V_{sat} - V_{out}) / L\} t$$

At the end of the on-time, Q_1 is turned off. As the magnetic field in the inductor starts to collapse, it generates a reverse voltage that forward biases D_1 and, the peak current will decay at a rate of $\Delta I / \Delta T = V/L$ as energy is supplied to C_0 and R_L . The voltage across the inductor during this period is equal to $V_{out} + V_F$ of D_1 and, the current at any instant is:

$$I_L = I_{L(PK)} - \{(V_{out} + V_F) / L\} t$$

Assume that during quiescent operation the average output voltage is constant and that the system is operating in the discontinuous mode. Then $I_{L(PK)}$ attained during t_{on} must decay to zero during t_{off} and a ratio of t_{on} to t_{off} can be determined.

$$\begin{aligned} \{(V_{in} - V_{sat} - V_{out}) / L\} t_{on} &= \{(V_{out} + V_F) / L\} t_{off} \\ \therefore t_{on} / t_{off} &= (V_{out} + V_F) / (V_{in} - V_{sat} - V_{out}) \end{aligned}$$

Note that the volt-time product of t_{on} must be equal that of t_{off} and the inductance value is not of concern when determining their ratio. If the output voltage is to remain constant, the average current into the inductor must be equal to the output current for a complete cycle. The peak inductor current with respect to output current is:

$$(I_{L(PK)}/2)t_{on} + (I_{L(PK)}/2)t_{off} = (I_{out} \cdot t_{on}) + (I_{out} \cdot t_{off})$$

$$\therefore I_{L(PK)} = 2I_{out}$$

The peak inductor current is also equal to the peak switch current $I_{PK(SWITCH)}$ since the two are in series. The on-time t_{on} is the maximum possible switch-conduction time. It is equal to the time required for C_T to ramp up from its lower to upper threshold. The required value for C_T can be determined by using the minimum oscillator charging current and the typical value for the oscillator voltage swing both taken from the data sheet electrical characteristics table.

$$C_T = I_{chg(min)}(\Delta t/\Delta V)$$

$$\approx 20 \times 10^{-6} \times (t_{on}/0.5)$$

$$= 4.0 \times 10^{-5} t_{on}$$

The off-time t_{off} , is the time that diode D_1 is in conduction and it is determined by the time required for the inductor current to return to zero. The off-time is not related to the ramp-down time of C_T . The cycle time of the LC network is equal to $t_{on(max)} + t_{off}$ and the minimum operating frequency is:

$$f_{min} = 1/(t_{on(max)} + t_{off})$$

A minimum value of inductance can now be calculated for L . The known quantities are the voltage across the inductor and the required peak current for the selected switch conduction time.

$$L_{(min)} = (V_{in} - V_{sat} - V_{out})t_{on}/I_{PK(SWITCH)}$$

This minimum value of inductance was calculated by assuming the onset of continuous conduction operation with a fixed input voltage, maximum output current, and a minimum charge current.

The net charge per cycle delivered to the output filter capacitor C_o , must be zero, $Q^+ = Q^-$, if the output voltage is to remain constant. The ripple voltage can be calculated from the known value of on-time, off-time, peak inductor current, and output capacitor value.

$$V_{RIPPLE(P-P)} = \left(\frac{1}{C_o} \right) \int_0^{t_1} i t dt + \left(\frac{1}{C_o} \right) \int_{t_1}^{t_2} i' t dt$$

Where $i t = (\frac{1}{2} I_{PK} \cdot t)/(t_{on}/2)$, $i' t = (\frac{1}{2} I_{PK} \cdot t)/(t_{off}/2)$

$$= \frac{1}{C_o} \left[\frac{I_{PK}}{t_{on}} \cdot \frac{t^2}{2} \right]_0^{t_1} + \frac{1}{C_o} \left[\frac{I_{PK}}{t_{off}} \cdot \frac{t^2}{2} \right]_{t_1}^{t_2}$$

(Where $t_1 = \frac{t_{on}}{2}$, $t_2 - t_1 = \frac{t_{off}}{2}$)

$$= \frac{I_{PK}(t_{on} + t_{off})}{8C_o}$$

A graphical derivation of the peak-to-peak ripple voltage can be obtained from the capacitor current and voltage waveforms in Figure. 7.

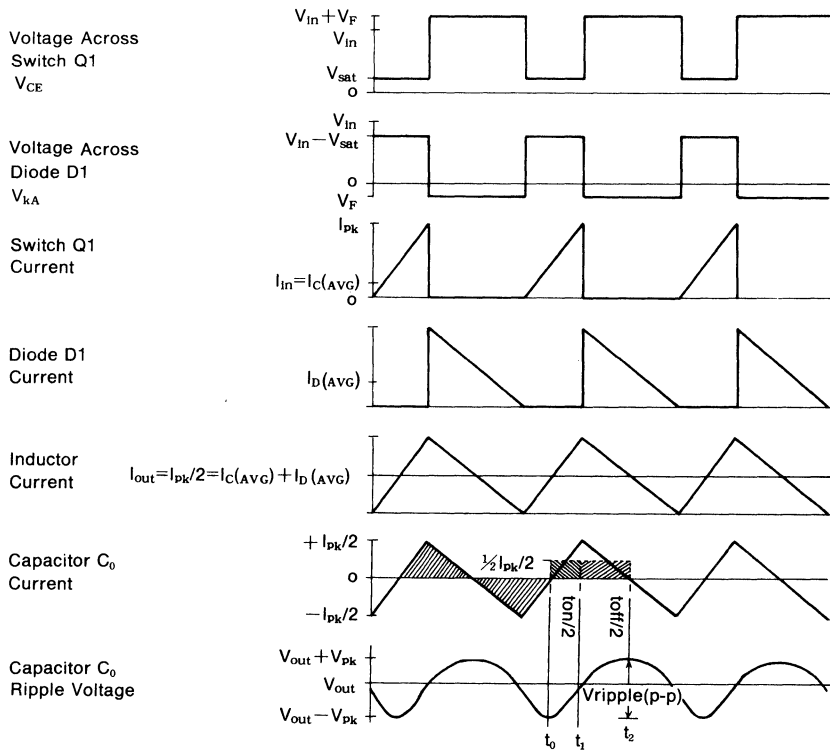


FIGURE 7 Step-Down Switching Regulator Waveforms

The calculation shown account for the ripple voltage contributed by the ripple current into an ideal capacitor. In practice, the calculated value will need to be increased due to the internal equivalent series resistance ESR of the capacitor.

STEP-UP SWITCHING REGULATOR OPERATION

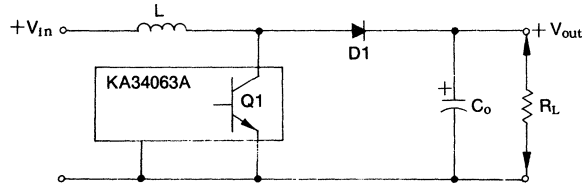


FIGURE 8 Step-Up Regulator ($V_{in} < V_{out}$)

Energy is stored in the inductor during the time that transistor Q_1 is in the 'on' state. Upon turn-off, the energy is transferred in series with V_{in} to the output filter capacitor and load. This configuration allows the output voltage to be set to any value greater than that of the input by the following relationship:

$$V_{out} = V_{in} \left(\frac{t_{on}}{t_{off}} \right) + V_{in} \text{ or } V_{out} = V_{in} \left(\frac{t_{on}}{t_{off}} + 1 \right)$$

An explanation of the step-up converter's operation is as follows: Initially, assuming that transistor Q_1 is off, the inductor current is zero, and the output voltage is at its nominal value. At this time, load current is being supplied only by C_o and it will eventually fall below nominal. This deficiency will be sensed by the control circuit and it will initiate an on-cycle, driving Q_1 into saturation. Current will start to flow from V_{in} through the inductor and Q_1 and rise at a rate of $\Delta I/\Delta T = V/L$. The voltage across the inductor is equal to $V_{in} - V_{sat}$ and the peak current is:

$$I_L = \left(\frac{V_{in} - V_{sat}}{L} \right) t$$

When the on-time is completed, Q_1 will turn off and the magnetic field in the inductor will start to collapse generating a reverse voltage that forward biases D_1 , supplying energy to C_o and R_L . The inductor current will decay at a rate of $\Delta I/\Delta T = V/L$ and the voltage across it is equal to $V_{out} + V_F - V_{in}$. The current at any instant is:

$$I_L = I_{L(pk)} - \left(\frac{V_{out} + V_F - V_{in}}{L} \right) t$$

Assuming that the system is operating in the discontinuous mode, the current through the inductor will reach zero after the t_{on} period is completed. Then $I_{L(pk)}$ attained during t_{on} must decay to zero during t_{off} and a ratio of t_{on} to t_{off} can be written.

$$\left(\frac{V_{in} - V_{sat}}{L} \right) t_{on} = \left(\frac{V_{out} + V_F - V_{in}}{L} \right) t_{off}$$

$$\therefore \frac{t_{on}}{t_{off}} = \frac{V_{out} + V_F - V_{in}}{V_{in} - V_{sat}}$$

The inductor current charges the output filter capacitor through diode D_1 only during t_{off} . If the output voltage is to remain constant, the net charge per cycle delivered to the output filter capacitor must be zero, $Q^+ = Q^-$.

$$I_{\text{chg}} t_{\text{off}} = I_{\text{dischg}} t_{\text{on}}$$

Fig9. shows the step-up switching regulator waveforms.

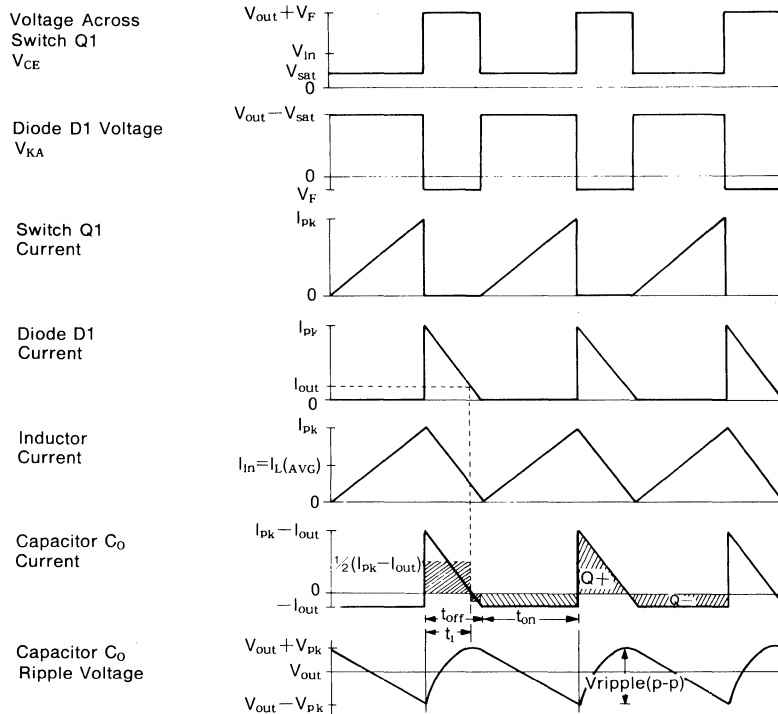


FIGURE 9 Step-Up Switching Regulator Waveforms

By observing the capacitor current and making some substitutions in the above statement, a formula for peak inductor current can be obtained.

$$\left(\frac{I_{L(pk)}}{2} \right) t_{\text{off}} = I_{\text{out}} (t_{\text{on}} + t_{\text{off}})$$

$$I_{L(pk)} = 2I_{\text{out}} \left(\frac{t_{\text{on}}}{t_{\text{off}}} + 1 \right)$$

The peak inductor current is also equal to the peak switch current, since the two are in series. With knowledge of the voltage across the inductor during t_{on} and the required peak current for the selected switch conduction time, a minimum inductance value can be determined.

$$L_{(min)} = \left(\frac{V_{in} - V_{sat}}{I_{pk(switch)}} \right) t_{on(max)}$$

The ripple voltage can be calculated from the known values of on-time, off-time, peak inductor current, output current and output capacitor value. Referring to the capacitor current waveforms in figure. 9, t_1 is defined as the capacitor charging interval.

Solving for t_1 in known terms yields:

$$\frac{I_{pk} - I_{out}}{t_1} = \frac{I_{pk}}{t_{off}}$$

$$\therefore t_1 = \left(\frac{I_{pk} - I_{out}}{I_{pk}} \right) t_{off}$$

The ripple voltage is

$$V_{ripple(p-p)} = \left(\frac{1}{C_o} \right) \int_0^{t_1} \frac{I_{pk} - I_{out}}{t_1} dt$$

$$= \frac{(I_{pk} - I_{out})^2 t_{off}}{2 I_{pk} C_o}$$

A simplified formula that will give an error of less than 5% for a voltage step-up greater than 3 with an ideal capacitor is shown:

$$V_{ripple(p-p)} \approx \left(\frac{I_{out}}{C_o} \right) t_{on}$$

VOLTAGE-INVERTING SWITCHING REGULATOR OPERATION

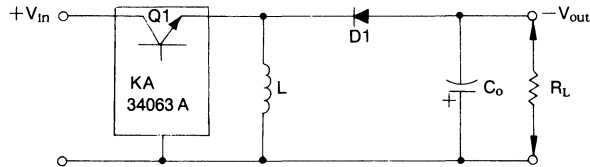


FIGURE 10 Voltage-Inverting Regulator($|V_{out}| \geq V_{in}$)

Energy is stored in the inductor during the conduction time of Q₁. Upon turn off, the energy is transferred to the output filter capacitor and load. Notice that in this configuration the output voltage is derived only from the inductor. This allows the magnitude of the output to be set to any value. It may be less than, equal to, or greater than that of the input and is set by the following relationship:

$$V_{out} = V_{in} \left(\frac{t_{on}}{t_{off}} \right)$$

The voltage-inverting converter operates almost identically to that of the step-up previously discussed. The voltage across the inductor during t_{on} is $V_{in} - V_{sat}$ but during t_{off} , the voltage is equal to the negative magnitude of $V_{out} + V_F$. Remembering that the volt-time product of t_{on} must be equal to that of t_{off} , a ratio of t_{on} to t_{off} can be determined.

$$(V_{in} - V_{sat})t_{on} = (|V_{out}| + V_F)t_{off}$$

$$\therefore \frac{t_{on}}{t_{off}} = \frac{|V_{out}| + V_F}{V_{in} - V_{sat}}$$

The derivations and the formulas for $I_{pk(switch)}$, $L_{(min)}$ and C_o are the same as that of the step-up converter.

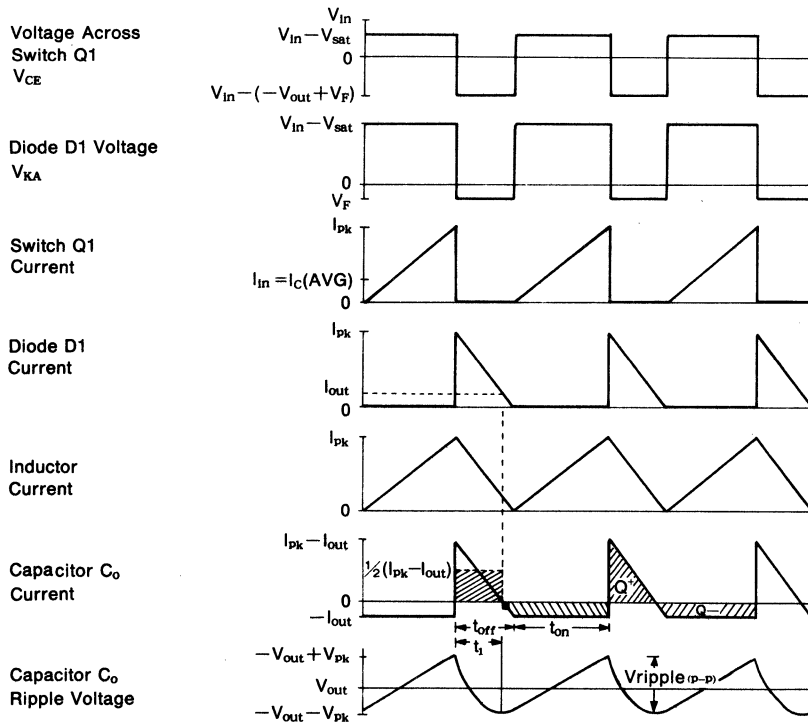


FIGURE 11 Voltage-Inverting Switching Regulator Waveforms

STEP-DOWN SWITCHING REGULATOR DESIGN EXAMPLE

〈Condition〉

$$V_{out} = 5 \text{ V}$$

$$I_{out} = 500 \text{ mA}$$

$$f_{min} = 18 \text{ KHz}$$

$$V_{in} = 25 - 10\% \text{ or } 22.5 \text{ V}$$

$$V_{ripple(p-p)} = 0.5\% V_{out} \text{ or } 25 \text{ mV}_{p-p}$$

$$1. t_{on}/t_{off} = (V_{out} + V_F) / (V_{in(min)} - V_{sat} - V_{out}) \\ = (5 + 0.8) / (22.5 - 0.8 - 5) \approx 0.3$$

$$2. t_{on(max)} + t_{off} = 1/f_{min} \approx 56 \mu\text{sec}$$

$$3. t_{off} \approx 43 \mu\text{sec}, t_{on} \approx 13 \mu\text{sec}$$

$$4. C_T = 4 \times 10^{-5} \times t_{on} \\ = 4 \times 10^{-5} \times 13 \times 10^{-6} = 520 \text{ pF} \Rightarrow \text{use } 470 \text{ pF}$$

$$5. I_{pk}(\text{switch}) = 2 \times I_{out} = 2 \times 0.5 = 1 \text{ A}$$

$$6. L_{(min)} = (V_{in(min)} - V_{sat} - V_{out}) \cdot t_{on(max)} / I_{pk}(\text{switch}) \\ = (22.5 - 0.8 - 5) \cdot 13 \times 10^{-6} / 1 \\ = 217 \mu\text{H} \Rightarrow \text{use } 220 \mu\text{H}$$

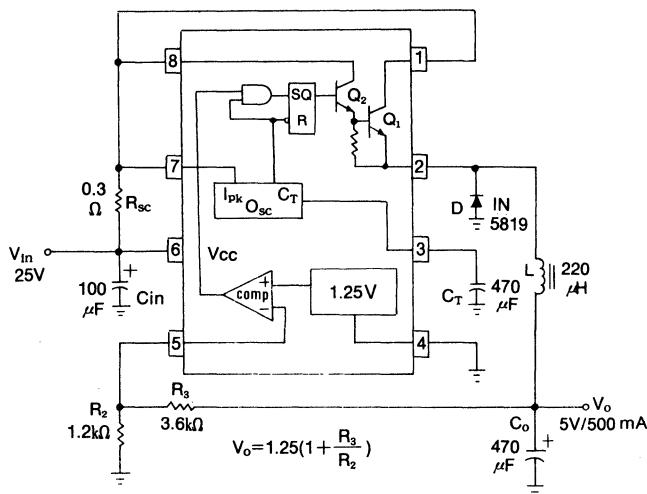
$$7. R_{sc} = 0.3 / I_{PK}(\text{switch}) = 0.3 / 1 = 0.3 \Omega$$

$$8. C_o = I_{PK}(\text{switch}) (t_{on} + t_{off}) / 8 V_{ripple(p-p)} \\ = 280 \mu\text{F} \Rightarrow \text{use } 470 \mu\text{F}$$

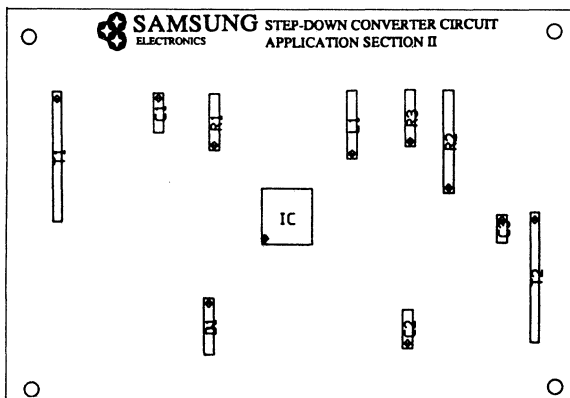
$$9. V_{out} = 1.25 \left(\frac{R_3}{R_2} + 1 \right)$$

If we select $R_3 = 3.6 \text{ k}\Omega$, we can calculate R_2 :

$$R_2 = 3.6 \times 10^3 \times (5 / 1.25 - 1)^{-1} = 1.2 \text{ k}\Omega$$

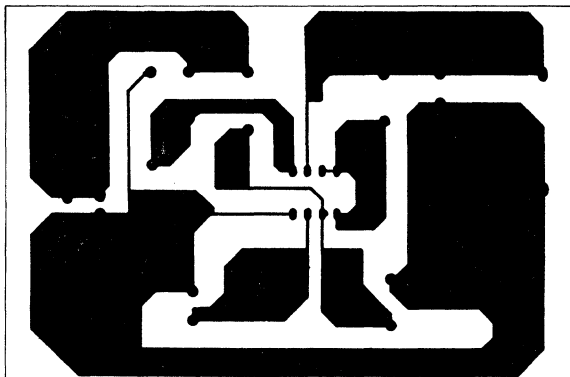


STEP-DOWN Switching Regulator Demo-PCB

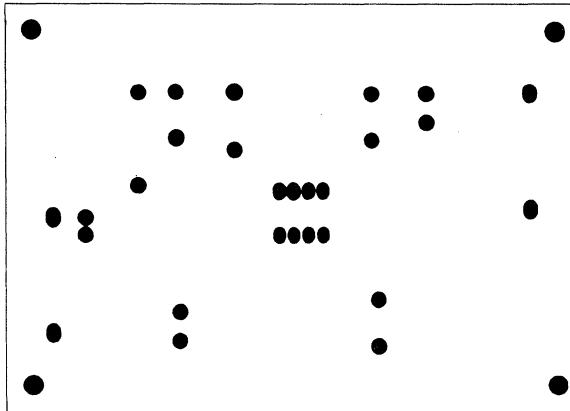


IC : KA 34063AN
 R : Resistor
 C : Capacitor
 D : Diode
 L : Inductor
 T : Tap(Input/Output)

〈Component Side〉



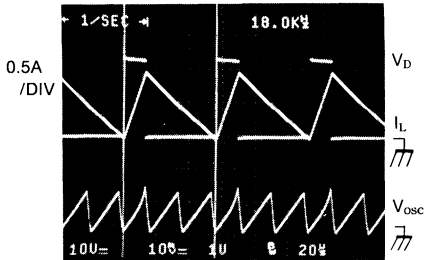
〈Copper Side〉



〈Solder Side〉

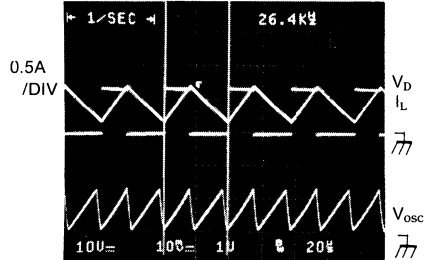
STEP-DOWN APPLICATION WAVEFORMS

V_D , I_L & V_{osc} Waveforms(I)



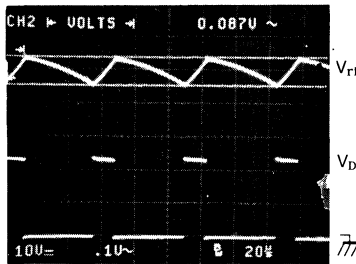
$V_{in}=25V$, $I_o=500mA$

V_D , I_L & V_{osc} Waveforms(II)



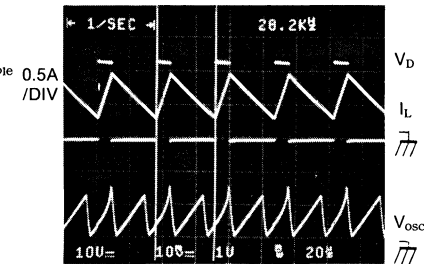
$V_{in}=15V$, $I_o=500mA$

V_{ripple} & V_D Waveforms



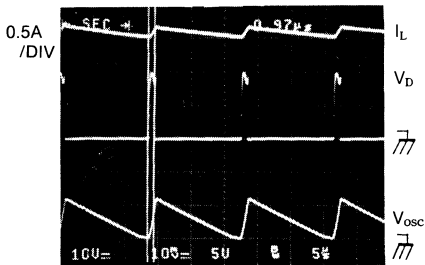
$V_{in}=25V$, $I_o=500mA$

V_D , I_L & V_{osc} Waveforms(III)



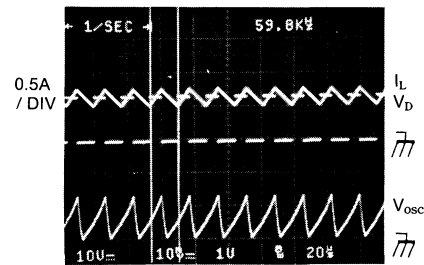
$V_{in}=25V$, $I_o=700mA$

I_L , V_D & V_{osc} Waveforms

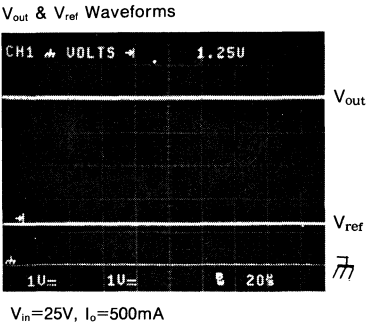
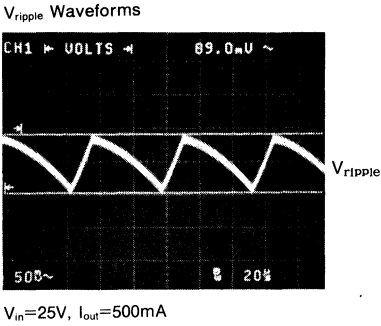
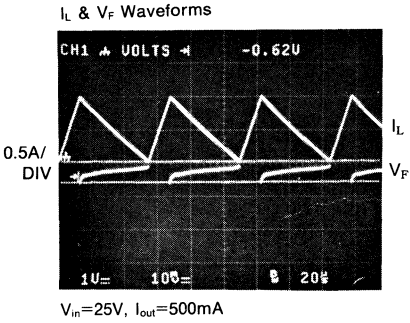


$V_{in}=25V$

V_D , I_L & V_{osc} Waveforms(IV)



$V_{in}=15V$, $I_o=700mA$



STEP-UP SWITCHING REGULATOR DESIGN EXAMPLE

(Condition)

$$V_{out} = 28 \text{ V}$$

$$I_{out} = 175 \text{ mA}$$

$$f_{min} = 23 \text{ KHz}$$

$$V_{in} = 8 \sim 16 \text{ V}$$

$$V_{ripple(p-p)} = 140 \text{ mV}_{p-p}$$

$$1. t_{on}/t_{off} = (V_{out} + V_F - V_{in}) / (V_{in} - V_{sat}) \\ = (28 + 0.8 - 8) / (8 - 0.8) \doteq 2.9$$

$$2. t_{on(max)} + t_{off} = \frac{1}{f_{min}} = \frac{1}{23 \times 10^3} \doteq 43.5 \mu\text{sec}$$

$$3. t_{off} \doteq 11.2 \mu\text{sec}, t_{on(max)} = 43.5 - 11.2 = 32.3 \mu\text{sec}$$

$$4. C_T = 4 \times 10^{-6} t_{on} \\ = 4 \times 10^{-6} \times 32.3 \times 10^{-6} = 1290 \text{ pF} \Rightarrow \text{use } 1300 \text{ pF}$$

$$5. I_{PK(switch)} = 2I_{out}(t_{on}/t_{off} + 1) \\ = 2 \times 175 \times 10^{-3} \times 3.9 \doteq 1.37 \text{ A}$$

$$6. L_{(min)} = (V_{in} - V_{sat}) t_{on(max)} / I_{PK(switch)} \\ = (8 - 0.8) \times 32.3 \times 10^{-6} / 1.37 \doteq 170 \mu\text{H}$$

$$7. R_{sc} = 0.3 / I_{PK(switch)} = 0.3 / 1.37 = 0.22 \Omega$$

$$8. C_o \approx I_{out} \cdot t_{on} / V_{ripple(p-p)} \doteq 40 \mu\text{F} \Rightarrow \text{use } 220 \mu\text{F}$$

$$9. V_{out} = 1.25 \left(\frac{R_2}{R_1} + 1 \right)$$

If we select $R_2 = 47 \text{ k}\Omega$, we can calculate R_1 :

$$R_1 = 47 \times 10^3 \times (28/1.25 - 1)^{-1} = 2.2 \text{ k}\Omega$$

10. The output switch transistor is driven into saturation with a forced gain of 20 at an input voltage of 8V. The required base drive is:

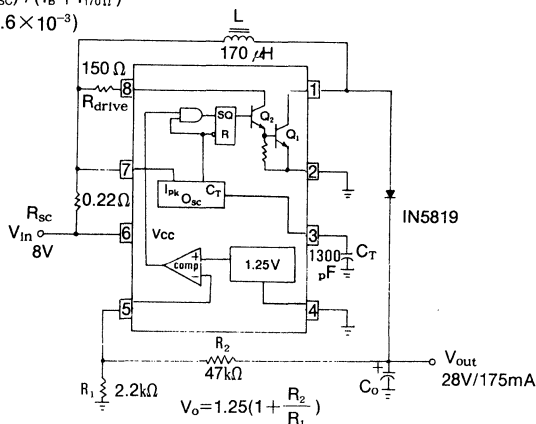
$$I_B = I_{PK(switch)} / \beta_I = 68.5 \text{ mA}$$

The current required to drive the internal 170Ω base-emitter resistor is:

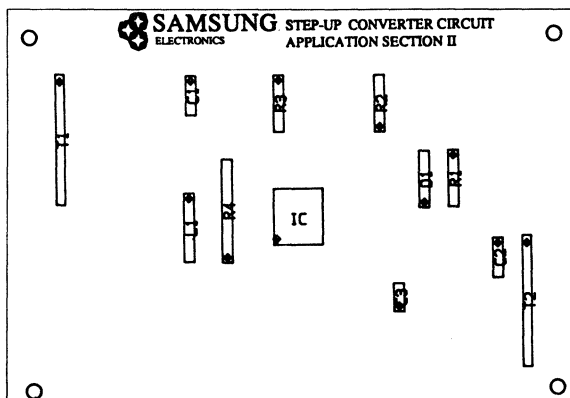
$$I_{170 \Omega} = V_{BE(switch)} / 170 = 4.1 \text{ mA}$$

The driver collector current is equal to sum of $68.5 \text{ mA} + 4.1 \text{ mA} = 72.6 \text{ mA}$

$$R_{driver} = (V_{in} - V_{sat(driver)} - V_{RSC}) / (I_B + I_{170 \Omega}) \\ = (8 - 0.3 - 0.2) / (72.6 \times 10^{-3}) \\ \doteq 103 \Omega \Rightarrow \text{use } 150 \Omega$$

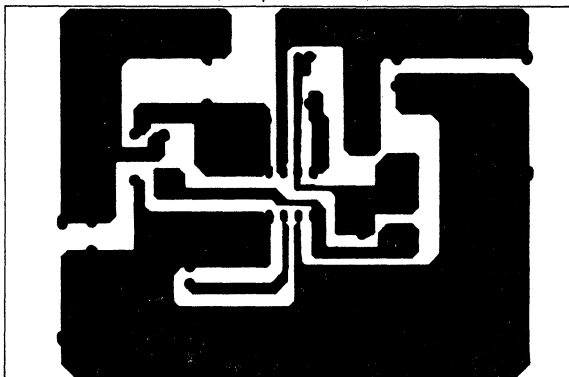


STEP-UP Switching Regulator Demo — PCB

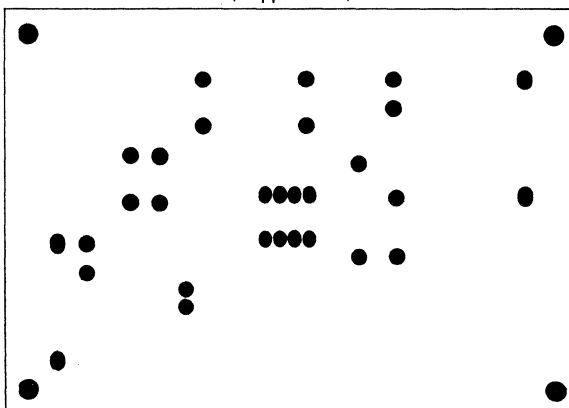


IC : KA 34063AN
 R : Resistor
 C : Capacitor
 D : Diode
 L : Inductor
 T : Tap(Input/Output)

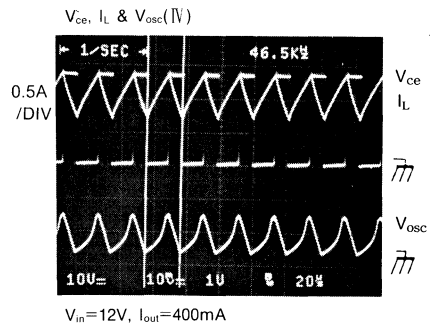
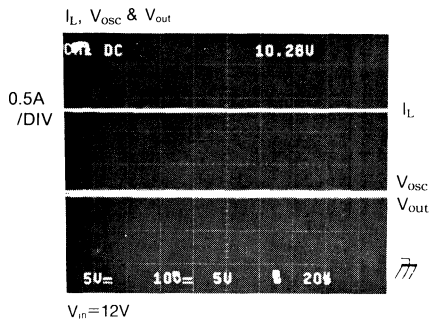
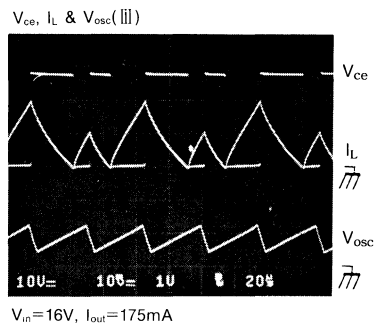
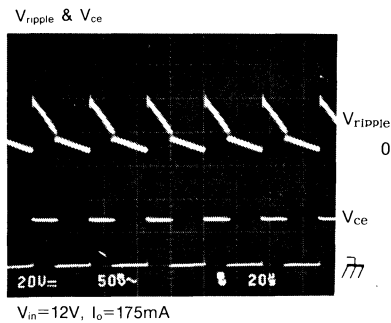
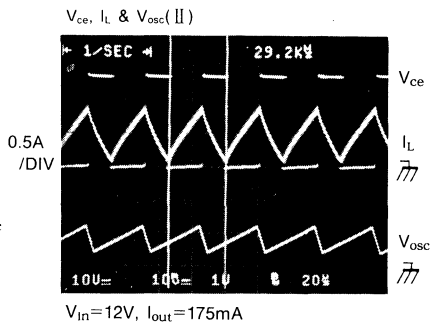
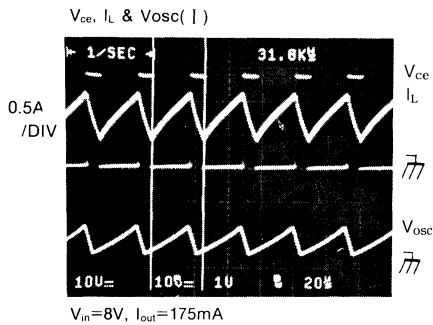
〈Component Side〉

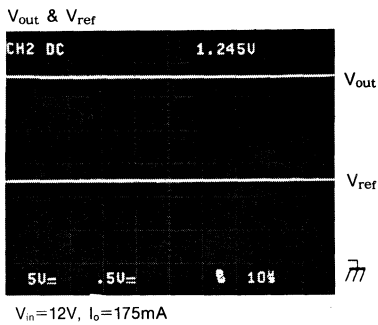
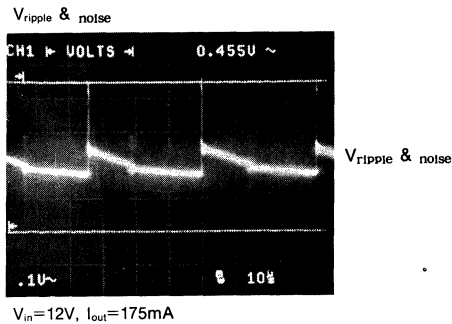
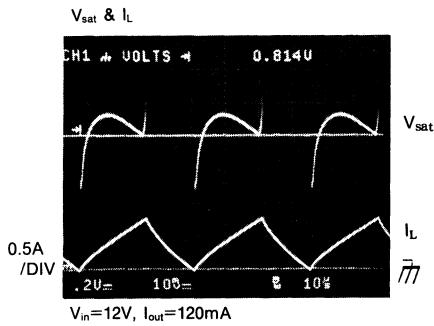


〈Copper Side〉



STEP-UP APPLICATION WAVEFORMS





VOLTAGE-INVERTING REGULATOR DESIGN EXAMPLE

〈Condition〉

$$V_{out} = -12 \text{ V}$$

$$I_{out} = 100 \text{ mA}$$

$$f_{min} = 50 \text{ KHz}$$

$$V_{in} = 5.4 \sim 7 \text{ V}$$

$$V_{ripple(p-p)} = 60 \text{ mV}$$

$$1. t_{on}/t_{off} = (|V_{out}| + V_F)/(V_{in} - V_{sat}) \doteq 2.8$$

$$2. t_{on(max)} + t_{off} = \frac{1}{f_{min}} = \frac{1}{50 \times 10^3} = 20 \mu\text{sec}$$

$$3. t_{off} \doteq 5.3 \mu\text{sec}, t_{on(max)} = 14.7 \mu\text{sec}$$

$$4. C_T = 4 \times 10^{-5} \times t_{on} \\ = 4 \times 10^{-5} \times 14.7 \times 10^{-6} \doteq 590 \text{ pF} \Rightarrow \text{use } 560 \text{ pF}$$

$$5. I_{pk(switch)} = 2 \cdot I_{out} \cdot (t_{on}/t_{off} + 1) \\ = 2 \times 100 \times 10^{-3} \times 3.8 = 760 \text{ mA}$$

$$6. L_{(min)} = (V_{in(min)} - V_{sat}) \cdot t_{on(max)} / I_{pk(switch)} \\ = (5.4 - 0.8) \times 14.7 \times 10^{-6} / 760 \times 10^{-3} \doteq 88 \mu\text{H}$$

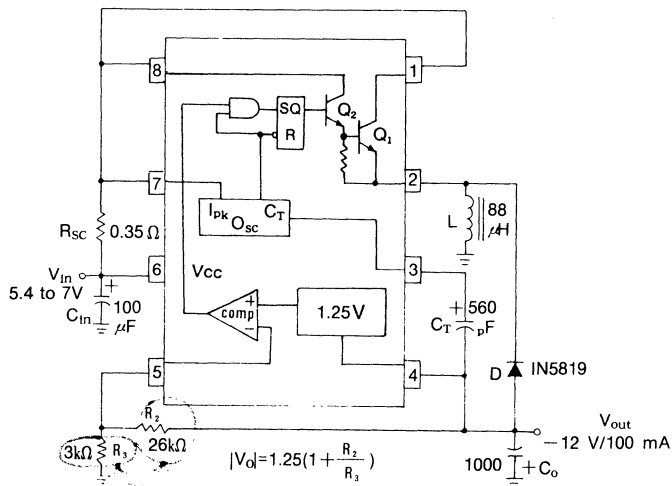
$$7. R_{sc} = 0.3 / I_{pk(switch)} = 0.3 / 760 \times 10^{-3} \doteq 0.39 \Omega \Rightarrow \text{use } 0.35 \Omega$$

$$8. C_o \approx I_{out} \cdot t_{on} / V_{ripple(p-p)} \doteq 25 \mu\text{F} \Rightarrow \text{use } 1000 \mu\text{F}$$

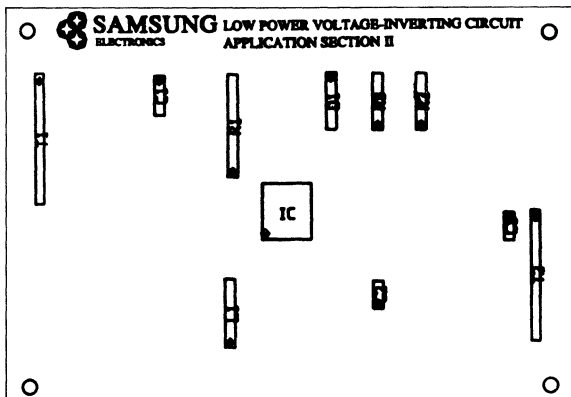
$$9. V_{out} = 1.25 \left(\frac{R_2}{R_3} + 1 \right)$$

If we select $R_3 = 3 \text{ k}\Omega$, we can calculate R_2 :

$$R_2 = \left(\frac{V_{out}}{1.25} - 1 \right) \times R_3 = 25.8 \text{ k}\Omega \Rightarrow \text{use } 26 \text{ k}\Omega$$



INVERTING Switching Regulator Demo—PCB



IC : KA 34063AN

R : Resistor

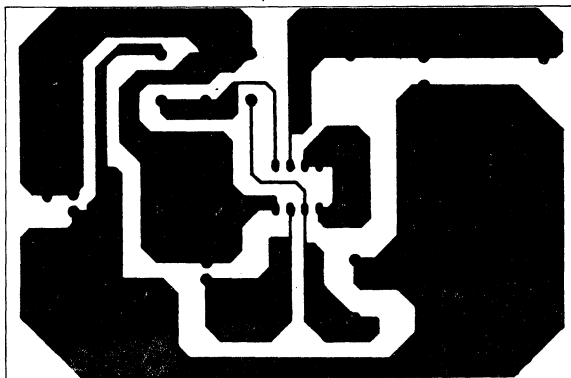
C : Capacitor

D : Diode

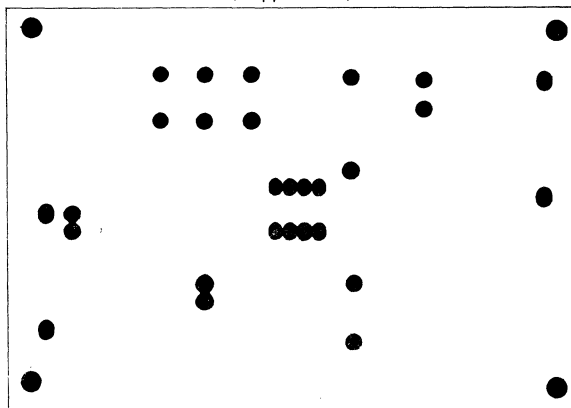
L : Inductor

T : Tap(Input/Output)

〈Component Side〉

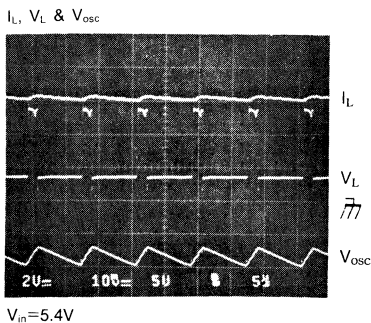
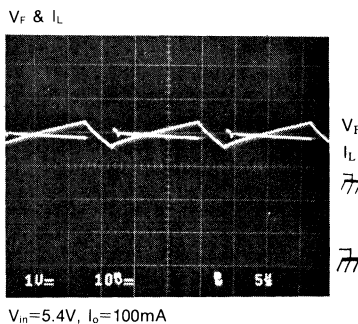
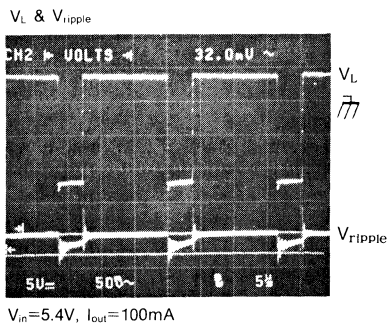
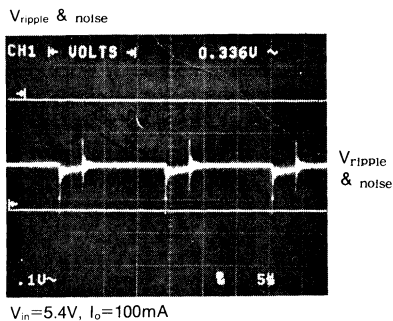
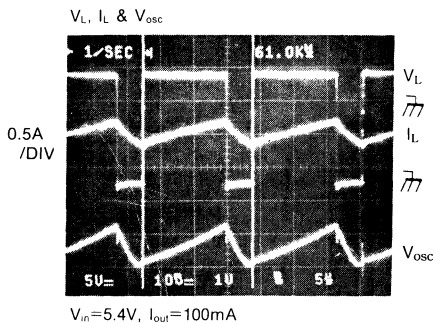


〈Copper Side〉



〈Solder Side〉

VOLTAGE—INVERTING APPLICATION WAVEFORMS



Design Formula Table

Calculation	Step-Down	Step-Up	Voltage-Inverting
$\frac{t_{on}}{t_{off}}$	$\frac{V_{out} + V_F}{V_{in(min)} - V_{sat} - V_{out}}$	$\frac{V_{out} + V_F - V_{in(min)}}{V_{in(min)} - V_{sat}}$	$\frac{ V_{out} + V_F}{V_{in(min)} - V_{sat}}$
$(t_{on} + t_{off})_{max}$	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$
C_T	$4 \times 10^{-5} t_{on}$	$4 \times 10^{-5} t_{on}$	$4 \times 10^{-5} t_{on}$
$I_{pk}(switch)$	$2 I_{out(max)}$	$2 I_{out(max)} \left(\frac{t_{on} + t_{off}}{t_{off}} \right)$	$2 I_{out(max)} \left(\frac{t_{on} + t_{off}}{t_{off}} \right)$
R_{SC}	$0.3/I_{pk}(switch)$	$0.3/I_{pk}(switch)$	$0.3/I_{pk}(switch)$
$L_{(min)}$	$\left(\frac{V_{in(max)} - V_{sat} - V_{out}}{I_{pk}(switch)} \right) t_{on(max)}$	$\left(\frac{V_{in(min)} - V_{sat}}{I_{pk}(switch)} \right) t_{on(max)}$	$\left(\frac{V_{in(min)} - V_{sat}}{I_{pk}(switch)} \right) t_{on(max)}$
C_o	$\frac{I_{pk}(switch)(t_{on} + t_{off})}{8V_{ripple(p-p)}}$	$\frac{I_{out} t_{on}}{V_{ripple(p-p)}}$	$\frac{I_{out} t_{on}}{V_{ripple(p-p)}}$

V_{sat} —Saturation Voltage of the output switch.

V_F —Forward Voltage drop of the rectifier.

The following power supply characteristics must be chosen:

V_{in} —Nominal input voltage, if this voltage is not constant, then use $V_{in(max)}$ for step-down and $V_{in(min)}$ for step-up converter.

V_{out} —Desired output voltage, $V_{out} = 1.25 \left(1 + \frac{R_2}{R_1} \right)$

I_{out} —Desired output current.

f_{min} —Minimum desired output switching frequency at the selected values for V_{in} and I_o .

$V_{ripple(p-p)}$ —Desired peak-to-peak output ripple voltage. In practice, the calculated value will need to be increased due to the capacitor's equivalent series resistance and board layout.

The ripple voltage should be kept to a low value since it will directly effect the line and load regulation.

• ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_{cc}	40	Vdc
Comparator Input Voltage Range	V_{IR}	-0.3~40	Vdc
Switch Collector Voltage	$V_{C(sw)}$	40	Vdc
Switch Emitter Voltage	$V_{E(sw)}$	40	Vdc
Switch Collector To Emitter Voltage	$V_{CE(sw)}$	40	Vdc
Driver Collector Voltage	$V_{C(driver)}$	40	Vdc
Switch Current	I_{sw}	1.5	A

• ELECTRICAL CHARACTERISTICS

(Vcc=5.0V, Ta=T low to T high unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillator						
Charging Current	I _{chg}	5.0≤V _{cc} ≤40V, Ta=25℃	24	33	42	μA
Discharge Current	I _{dischg}	5.0≤V _{cc} ≤40V, Ta=25℃	140	200	260	μA
Frequency	f _{osc}	V _{pin5} =0V, C _T =1.0nF, Ta=25℃	24	33	42	KHz
Discharge To Charge Current Ratio	I _{dischg} / I _{chg}	I _{pk} (sense)=V _{cc} , Ta=25℃	5.2	6.2	7.5	—
Current Limit Sense Voltage	V _{ipk} (sense)	I _{chg} =I _{dischg} Ta=25℃	250	300	350	mV
Output Switch(Note 2)						
Saturation Voltage I	V _{ce} (sat)	I _{sw} =1.0A, V _{c(driver)} =V _{c(sw)}	—	1.0	1.3	V
Saturation Voltage II	V _{ce} (sat)	I _{sw} =1.0A, R _{pin8} =82Ω to V _{cc}	—	0.45	0.7	V
DC Current Gain	h _{FE}	I _{sw} =1.0A, V _{CE} =5.0V, Ta=25℃	50	120	—	—
Collector off State Current	I _c (off)	V _{CE} =40V	—	0.01	100	μA
Comparator						
Threshold Voltage	V _{th}	Ta=25℃	1.225	1.25	1.275	V
		Ta=T _{low} to T _{high}	1.21	—	1.29	
Threshold Voltage Line Regulation	Regline	3.0V≤V _{cc} ≤40V	—	1.4	5.0	mV
Input Bias Current	I _b	V _{in} =0V	—	−40	−400	nA
Total Device						
Supply Current	I _{cc}	5.0≤V _{cc} ≤40°V C _r =0.001μF I _{pk} (sense)=V _{cc} V _{pin5} >V _{th} pin2=GND	—	2.4	4.0	mA

①T low=0℃, T high=+70℃

②Output switch tests are performed under pulsed conditions to minimize power dissipation.

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PWM SWITCHING REGULATOR DEVICES

Application Note

PWM SWITCHING REGULATOR DEVICES

INTRODUCTION

The basic function of every regulator is to convert an AC or DC input voltage into a stable DC output voltage and then maintain this output voltage over a specified wide range of load conditions. Typically, the voltage regulator contains the following components:

- Reference circuit which provides a known stable reference voltage.
- Sampling element to sample the output voltage level.
- Comparator for comparing the output voltage sample to the reference and generating an error signal.
- Control circuit that will translate the input voltage to the desired output level over variable load conditions as fed back by the error signal.

SAMPLING ELEMENT

The function of a sampling element is to monitor the output voltage and translate it into a level which is equal to the reference voltage for a desired output voltage. The variations in the output voltage cause the feedback voltage to change it to a value which may be lesser or greater than the reference voltage. This small voltage is the error voltage that directs the regulator to respond and make appropriate correction in the output voltage if the output voltage has changed from its defined level.

COMPARATOR

The function of the comparator is to monitor the feedback voltage for comparison with the reference voltage. Also, the comparator provides gain for the detected error signal level and so it is called error amplifier. The output of the comparator is actually an amplified error signal and it is translated to the output by the control circuit for maintaining a certain output level.

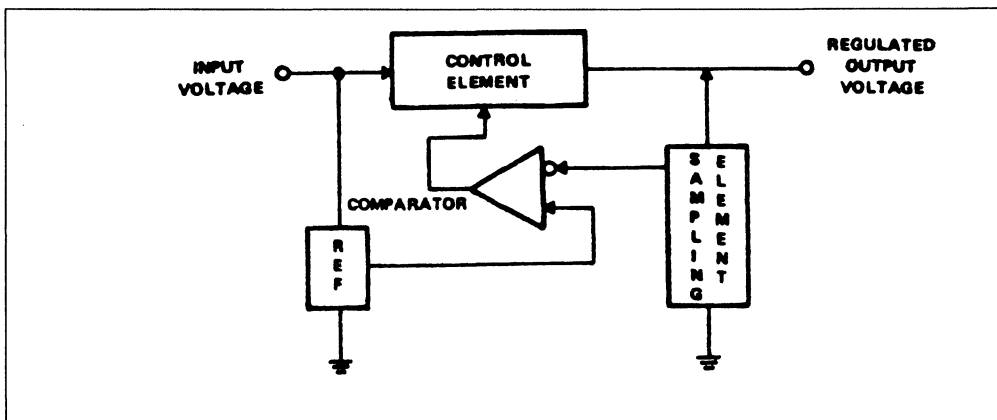


Figure 1. Basic Regulator

REFERENCE ELEMENT

The reference element is the main component of voltage regulators, because the output voltage is either equal to or a multiple of the reference. Any variations in the input voltage will be interpreted as an error in the output voltage by the comparator and causes the comparator to change the output voltage accordingly. Therefore, the reference voltage must be highly stable for all variations in the output voltage and junction temperature.

CONTROL CIRCUIT

The control circuit depends on the regulator type, because the design of the control circuit determines whether the regulator is series type, shunt type, or a switching type. Figure 2 shows basic configurations of the control circuit. The control circuit translates the error voltage to the output and it influences the performance of the regulator because it affects the input-output differential, circuit efficiency and power dissipation.

PWM SWITCHING REGULATOR DEVICES

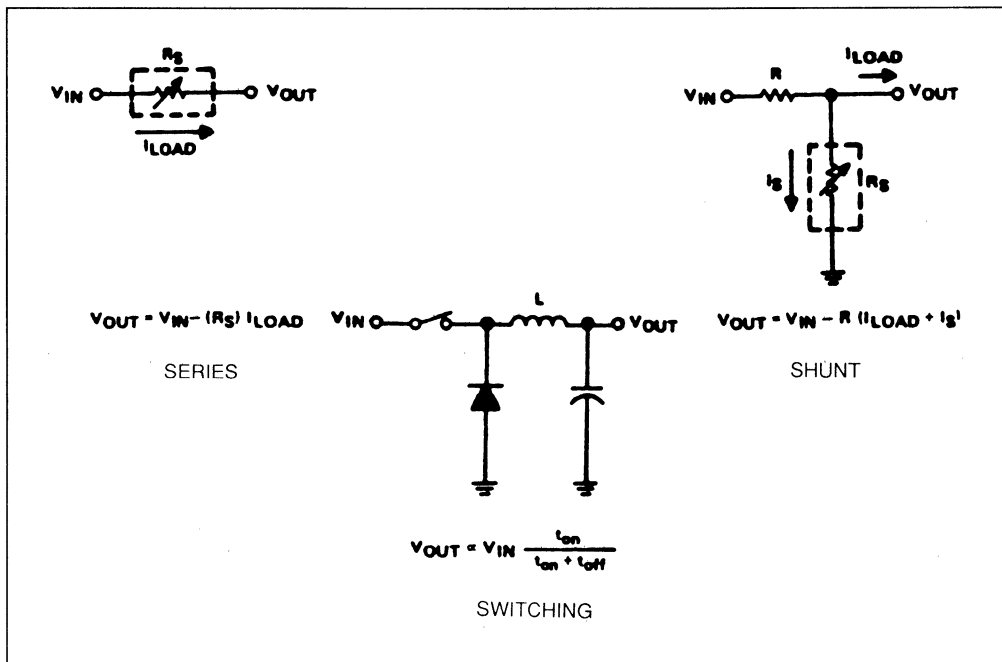


Figure 2. Control Element Configuration

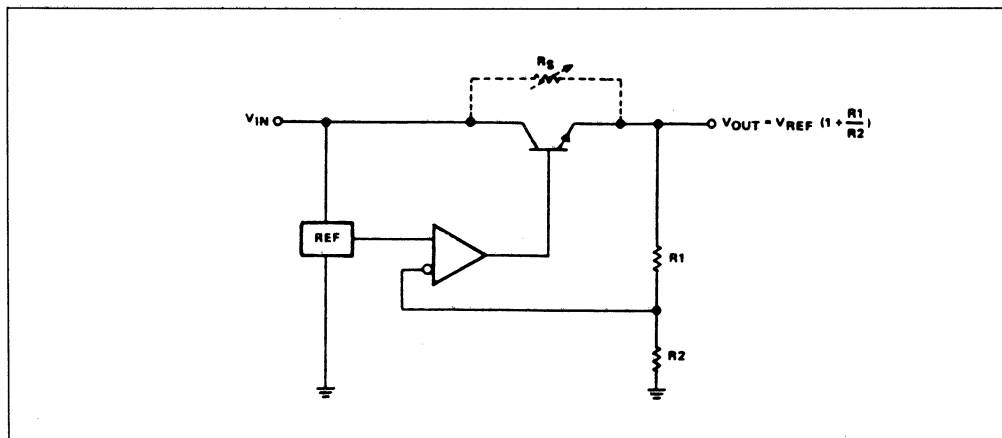


Figure 3. Basic Series Regulator

PWM SWITCHING REGULATOR DEVICES

The voltage regulators can be designed using many different circuit implementations, but the three basic methods are:

- Series Regulator
- Shunt Regulator
- Switching Regulator

Series Regulator

The output voltage is regulated by modulating a series element which acts as a variable resistor. A transistor is employed as a series element as shown in figure 3. Any change in the output voltage

changes the equivalent resistance of the series transistor accordingly. The product of this resistance and the load current produce differential voltage that will compensate for the change in the input voltage.

The output voltage V_{OUT} is equal to:

$$\begin{aligned} V_{OUT} &= V_{IN} - V_D \\ V_D &= I_L R_S \\ V_{OUT} &= V_{IN} - I_L R_S \end{aligned} \quad \begin{aligned} V_D &= \text{Differential Voltage} \\ V_L &= \text{Load Current} \end{aligned}$$

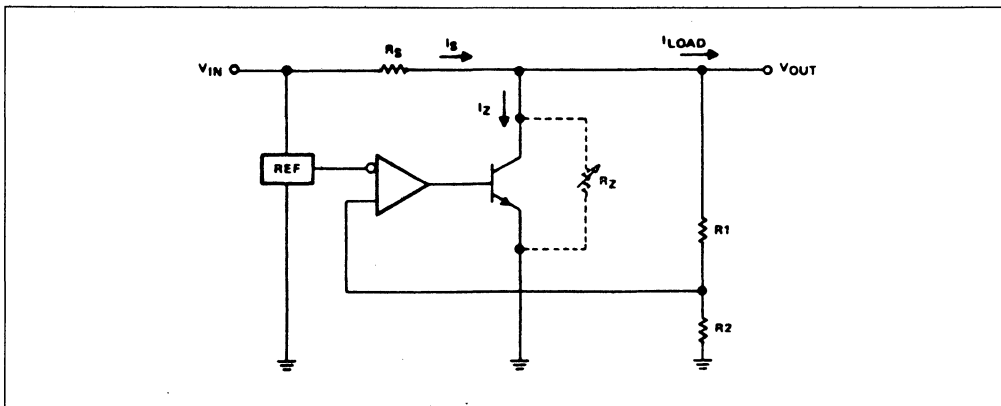


Figure 4. Basic Shunt Regulator

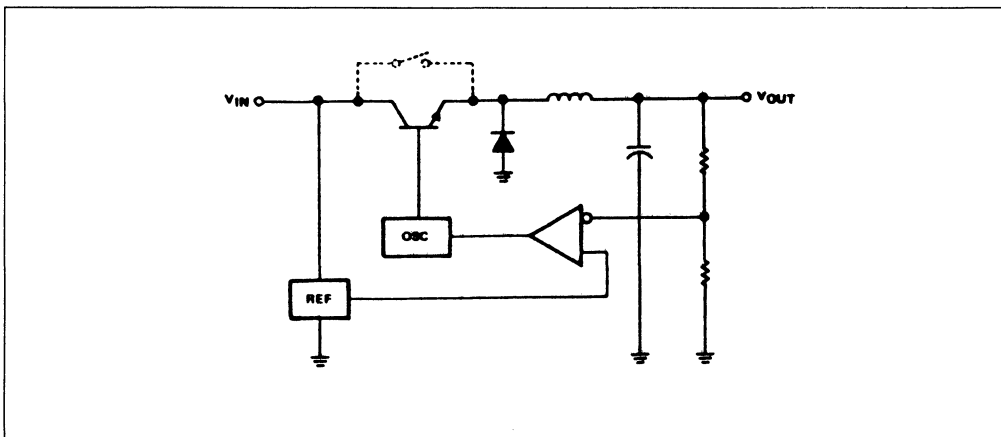


Figure 5. Basic Switching Regulator
(Step-down Configuration)

PWM SWITCHING REGULATOR DEVICES

Change in R_s for a changing input voltage will be:

$$\text{and } \Delta R_s = \frac{V_{IN}}{I_L}$$

Change in R_s for a changing load current will be:

$$\Delta R_s = \frac{\Delta I_L R_s}{I_L + \Delta I_L}$$

Series regulators provide an inexpensive means for obtaining regulated voltage. However, the disadvantage of this method is that in applications requiring very high load currents, the voltage drop across the series element is very high, resulting in power loss.

Shunt Regulator

Shunt regulator employs a shunt element and changes in the input voltage or load conditions result in changes in the shunt current requirement. Figure 4 shows basic configuration of shunt regulator.

The output voltage V_{OUT} in this case will be:

$$\begin{aligned} V_{OUT} &= V_{IN} - I_S R_s \\ I_S &= I_L + I_Z \\ V_{OUT} &= V_{IN} - R_s (I_L + I_Z) \end{aligned}$$

Change in I_Z for a changing load current will be:

$$\text{and } \Delta I_Z = \Delta I_L$$

Change in I_Z for a changing input and voltage will be:

$$\Delta I_Z = \frac{V_{IN}}{R}$$

$$\Delta I_Z = \frac{V_{OUT}}{\Delta R_Z}$$

This type of regulator is not very efficient, but is less sensitive to input voltage transients and the load current transients are not reflected back to the source. Because of its configuration, the shunt regulator is short circuit proof inherently.

Switching Regulator

The switching regulator employs an active switch as its control element. The switch is a high frequency inverter whose function is to chop the rectified input voltage at a varying duty cycle. An LC filter is normally used and its function is to average the voltage appearing at its input and deliver this voltage to the output load. The transistor in the basic circuit (Figure 5) is either in ON STATE (saturation) or OFF STATE, so the power losses in the control circuit are minimum. This is the primary reason this type of power supply is particularly useful in applications where the difference between the input and output voltage is very high.

Figure 6 shows different modes of the control element. From this figure it can be seen that the control circuit is subjected to a high current at a very low voltage or a high differential voltage at a very low

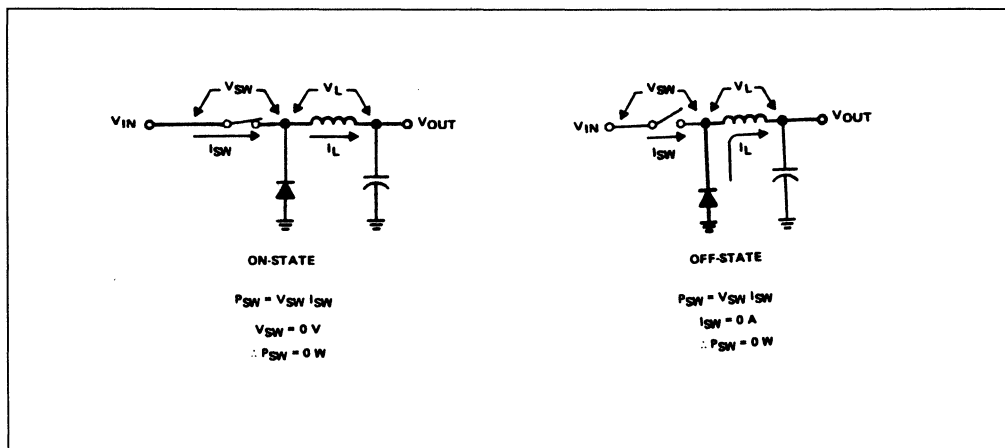


Figure 6. Modes of Control Element.

PWM SWITCHING REGULATOR DEVICES

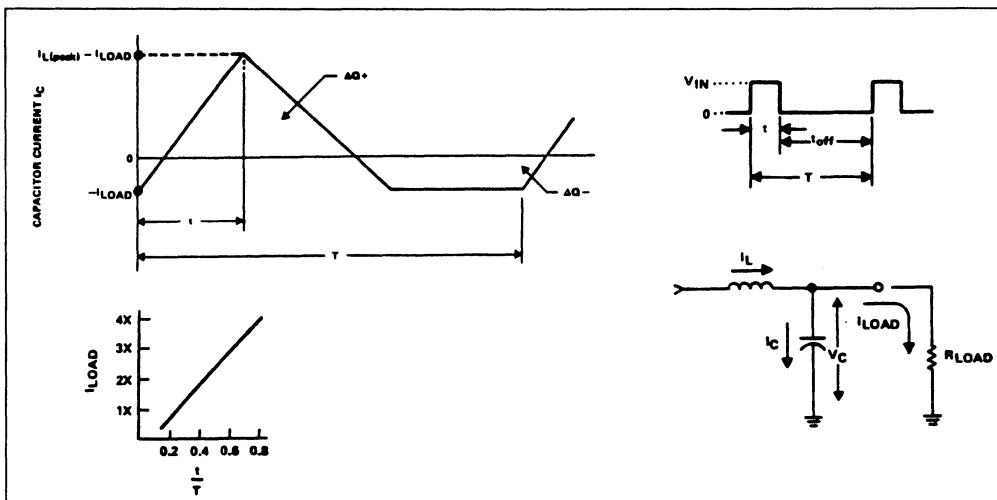


Figure 7. Waveform on Capacitance

current. In both cases, the power dissipation in this control circuit is minimum. The changes in the load current or input voltage can be compensated for by varying the on/off ratio (duty cycle) of the switch.

If the output voltage should remain constant, then the net change in the capacitor must remain constant. In other words, the charge delivered to the capacitor must be dissipated by the load.

$$\begin{aligned} I_C &= I_L - I_{LOAD} \\ I_C &= I_{LOAD} \text{ for } I_L = 0 \\ I_C &= I_{L(peak)} - I_{LOAD} \text{ for } I_L = I_{L(peak)} \end{aligned}$$

The charge delivered to the capacitor and the charge dissipated in the load are equal to the area covered under the capacitor current waveform.

$$\Delta Q_+ = \frac{1}{2} \frac{(I_{L(peak)} - I_{LOAD})^2}{I_{L(peak)}} t \frac{V_{IN}}{V_C}$$

$$\Delta Q_- = I_{LOAD} \left[T \frac{1}{2} t \frac{V_{IN}}{V_C} - \frac{1}{2} t \left(\frac{I_{L(peak)} - I_{LOAD}}{I_{L(peak)}} \right) \left(\frac{V_{IN}}{V_C} \right) \right]$$

If Q_+ is set equal to Q_- , the relation of I_{LOAD} for $Q = 0$ can be determined by:

$$I_{LOAD} = \frac{1}{2} I_{L(peak)} \left(\frac{V_{IN}}{V_C} \right) \left(\frac{t}{T} \right)$$

As can be seen above, the duty cycle t/T can be varied to compensate the input voltage variations or load variation.

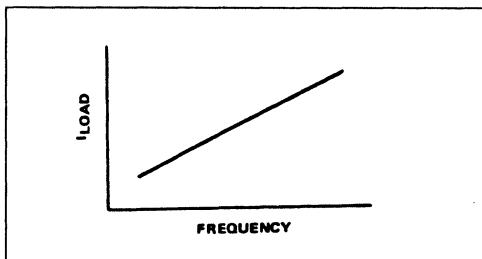


Figure 8. Fixed On-Time

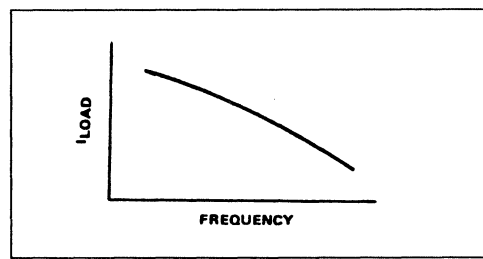


Figure 9. Fixed Off-Time

PWM SWITCHING REGULATOR DEVICES

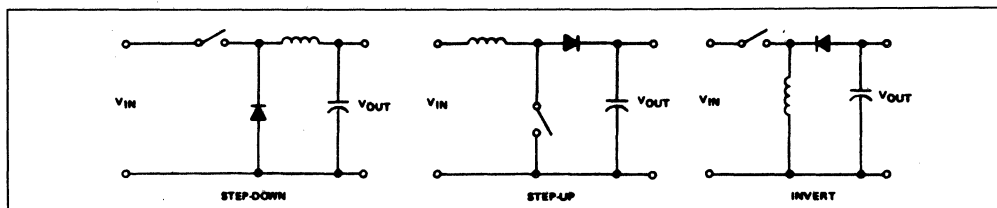


Figure 10. Single-Ended Transformer Coupled Circuits

The duty cycle can be varied by:

- Maintaining a constant on-time, and varying the frequency
- Maintaining a constant off-time, and varying the frequency
- Maintaining a constant frequency and varying the on/off time

The value of inductor can be calculated from

$$L = \frac{V}{I} t$$

where: L = inductance (in microhenry)
V = differential voltage (in Volts)
I = inductor current required (defined by load in Amps).
t = On-time (in microseconds)

Fixed On-Time Variable Frequency

In this technique, the time the input voltage is applied to the LC filter is kept constant and the duty cycle is varied by varying the frequency $1/T$. This is a relatively easier method and suitable for applications where voltage conversions are required for step-down, step-up, or invert type of power supply.

Figure 8 shows variations in frequency with the load current in this method.

Fixed Off-Time Variable Frequency

In this method, the average DC voltage is varied by changing the on-time (t) of the switch while maintain-

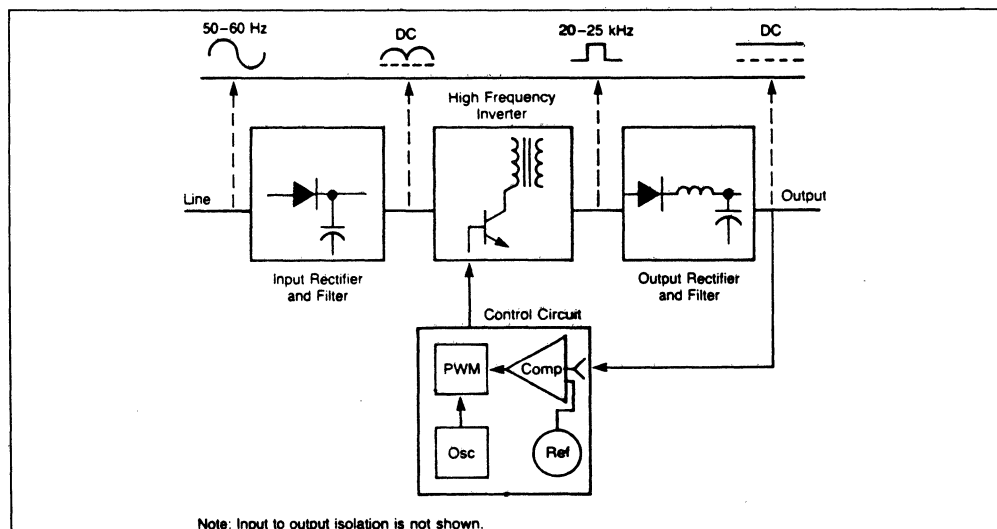


Figure 11. Basic Blocks of Switching Regulator

PWM SWITCHING REGULATOR DEVICES

ing a fixed off-time. In fixed-off time process, as the load current increases, the on-time is also increased, thereby decreasing the operating frequency. (see Figure 9). This method allows a design of the voltage regulator with predefined minimum frequency under full load condition and also allows the DC current to be established under the increased load condition. This will help reduce the ripple current while maintaining the average current. Care should be taken to ensure that the saturation characteristics of the inductor are not exceeded because the maximum current that can flow through the inductor under transient load current is not well defined.

Fixed-Frequency, Variable Duty Cycle

In fixed-frequency regulators, the duty cycle of the pulse train is varied for changing the average power. The fixed-frequency switching regulators are most suited in the systems having transformer-coupled output stages, since the fixed frequency concept allows it to take full advantage of the magnetic properties of the transformers. Transformer-coupled systems offer an ideal choice for power supply designs having single or multiple voltage conversions.

The fixed-frequency regulators are used extensively in the mainframe power supply control circuits. In systems with single-ended output stages, the fixed-frequency method also establishes DC current through the inductor for increased load conditions to maintain the required current transfer with minimum ripple current.

Basic Circuit of the Switching Power Supply

Figure 11 shows the basic configuration of the

switching power supply. The main component in this circuit is the high frequency inverter whose function is to chop the rectified input voltage. The rest of the circuit will support this switching function.

The input line voltage is rectified by the input rectifier circuit and then filtered. The function of regulating this voltage is performed by the control circuit. The control circuit closes the loop from the output to the inverter. Most of these control circuits contain an oscillator that generates fixed frequency and then uses a pulse width modulation method for controlling the output voltage. When the load is reduced, the output voltage increases sending signal to the control circuit. The control circuit then delivers shorter pulses to the inverter. If the load is increased, the output voltage decreases sending a signal to the control circuit so it delivers longer pulses to the inverter.

The inverter section contains a transformer which provides electrical isolation between the line and load. Transformer makes designs of an inverter section versatile and allows several different configurations of switching regulators such as: Step-up (boost), step-down (buck), flyback, push-pull and half-bridge converters. Figure 12 shows step-down and step-up configurations.

Step Down (buck) Converter

The buck type of circuit interrupts the line voltage and provides variable pulse width square wave to the LC filter. The regulation of this type converter is achieved by varying the duty cycle.

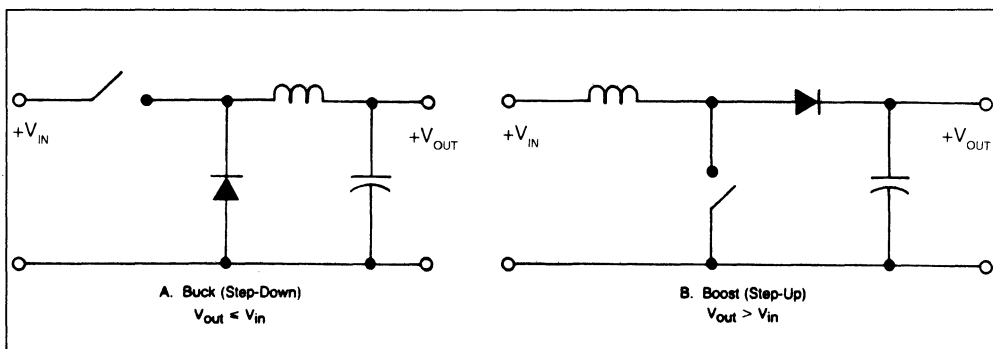


Figure 12. Buck and Boost Converters

PWM SWITCHING REGULATOR DEVICES

The output voltage in this case may be approximated as:

$$V_{OUT} = V_{IN} \times \text{duty cycle}$$

The drop in the output section (IR), diode and transistor saturation voltages can be compensated by adjusting the transformer turns ratio.

Step Up (boost) Converter

In step up configuration, the energy is first stored in the choke and then this surplus energy is delivered from the input line to the load. In this configuration, the choke works as a storage element that delivers a fixed amount of power to the load.

$$P_{OUT} = -L_f f_o$$

where I = Peak Choke Current
fo = Operating Frequency
L = Inductance

The value of load resistor can be calculated as follows:

$$V_{OUT} = \sqrt{P_o R_L}$$

where R_L = Load Resistance

$$V_{OUT} = \sqrt{\frac{L_f R_L}{2}}$$

The choke current is proportional to the On Time of Duty Cycle of the switch. The regulation for fixed loads is controlled by the duty cycle variation as before. The difference between the buck converter and boost converter is that the output of the boost converter depends on the load and hence the loop gain varies with the load.

Flyback Converter

This type of converter stores energy in the primary winding and dumps it into the secondary windings (shown in Figure 13). The flyback converter is relatively less expensive to design because the filter chokes are not required in the output stage. The

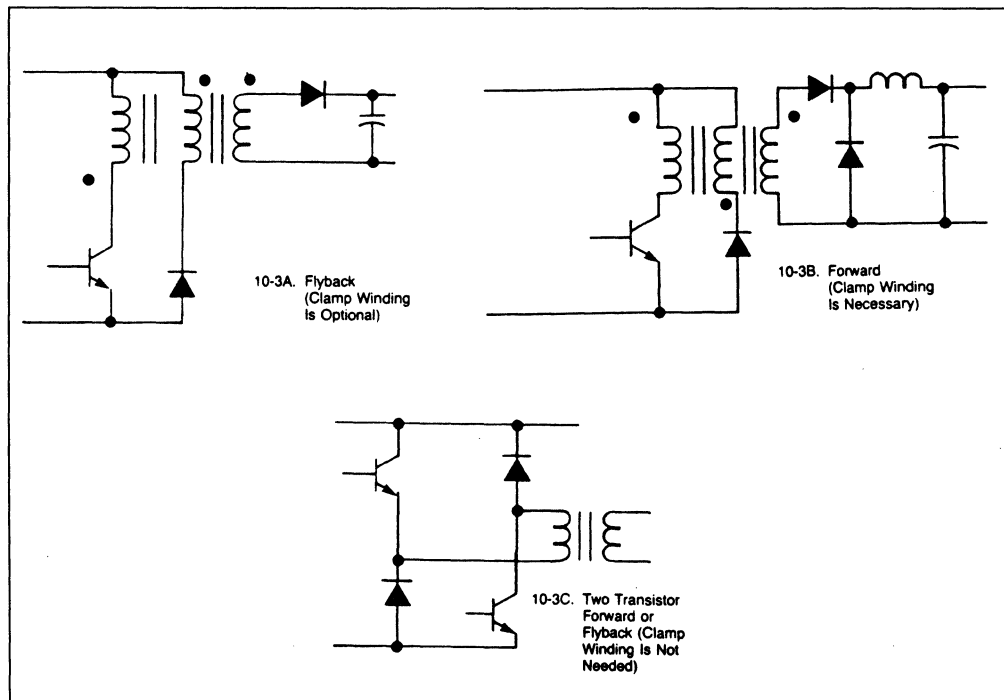


Figure 13. Flyback Converter

PWM SWITCHING REGULATOR DEVICES

output capacitors receive charge from the current source and not the voltage. The disadvantage is that the flyback converter will have more ripple. However, this type of converter offers better regulation in applications requiring multiple output voltages because it provides better cross regulation security than other converters. When the load changes on one winding, it has very little effect on other output voltage of others.

Normally a flyback converter designed to operate from the line (110/220 Vac) employs 1500 Volt transistors which are used for horizontal deflection in TV circuits. These transistors must be able to block twice the peak line voltage and the transients of about 1KV. Converters with these transistors can operate at frequencies up to 50KHz without any problems. Turn-on time for these bipolar transistors is slower, therefore MOSFETs must be used for operations at higher frequencies.

The flyback converter has one advantage over boost converters in that it can operate in a continuous mode. As stated before, in boost regulators the energy is dumped from the choke to the load before the switching transistor is turned on again. If, however, the transistor is turned on during the time the energy is being dumped, the circuit is operating in continuous mode. In this case, the transistor will require half of the peak current to deliver the same power to the load. Generally, the inductance must be increased by 10 times to reduce the peak current to half. The inductance can be increased by reducing the gap in the transformer and/or by increasing the core size. Figure 14 shows the waveforms of the transistor operating in continuous and discontinuous

modes. In the continuous mode of operation, the transistor must be able to turn on from higher voltage levels (typically 50 to 600 volts), because there is no longer any dead time for flyback voltage to settle back to the input voltage level.

Push-Pull Converters

The push-pull converter design is used for applications requiring low voltage converters such as 12V DC from 110V DC power supply. This type of converters are free running and mostly operating from low voltages where transformer saturation problems do not occur. The applications for push-pull converters are found in DC to DC converters. Figure 15 shows a basic push-pull type converter.

Control Circuits

Many different control circuits are available for switching mode power supplies. The basic function of regulating output voltage is performed by the PWM pulse width modulation section of all these devices. In this section, the DC feedback signal is compared to a fixed frequency sawtooth waveform. As a result of this a pulse train with variable pulse train is obtained. This pulse train can be fed to a buffer which can then be used to drive the power switching transistor.

The KA3525AN is a regulator pulse width modulator used in all types of switching power supplies. The on-chip features reduce external components and make it convenient to use.

The KA3842 is a current mode pulse width modulator controller and is specifically designed for off-line and DC-to-DC converter applications.

The KA34063AN is a monolithic switching regulator subsystem used in a DC-to-DC converter.

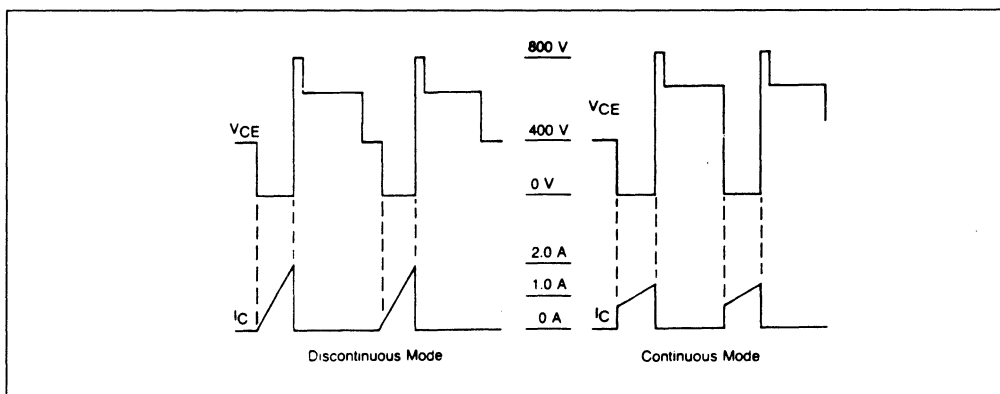


Figure 14. Flyback Transistor Waveforms

PWM SWITCHING REGULATOR DEVICES

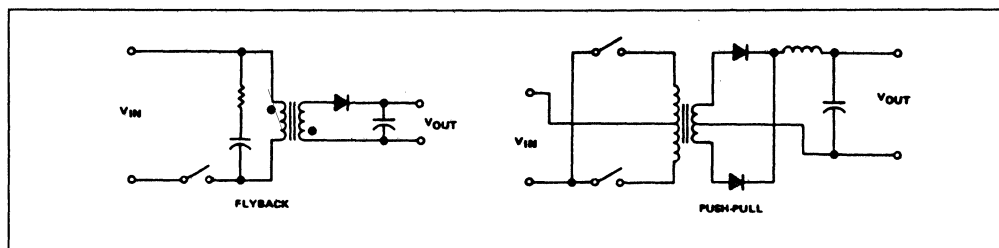


Figure 15. Transformer Coupled Circuits

PART NUMBER	FEATURES
KA3525AN	• 8.0 to 35V Operation • $5.1V \pm 1.0\%$ Trimmed Reference • 100Hz to 500KHz Oscillator Range • Separate Oscillator Sync Pin • Adjustable Dead Time Control • Input Undervoltage Lockout with Hysteresis • Latching PWM to Prevent Multiple PULses • Pulse-by-Pulse Shutdown • Dual Source/Sink Output Drivers • Internal Soft-Start • 16-Pin DIP Package
KA3842	• Automatic Feed Forward Compensation • Optimized for Off-Line Converter • Double PULse Suppression • Current Mode Operation to 500KHz • High Gain Totempole Output • Internally Trimmed Bandgap Reference • Undervoltage Lockout with Hysteresis • Low Startup Current • 8-Pin DIP and 14-Pin SOP Package
KA34063AN	• Operation From 3.0 to 40V Input • Short Circuit Current Limiting • Low Standby Current • Output Switch Current of 1.5A • Output Voltage Adjustable • Frequency of Operation from 100Hz to 100KHz

Table 1. Features of PWMs From Samsung

DATA CONVERTERS

System Design Guide

DATA CONVERTERS

OBTAINING THE BEST PERFORMANCE FROM A/D AND D/A CONVERTERS

The KSV3110 data converter was developed for use in all applications which require high-speed data conversion, i.e., TV circuits, VCRs or MAC converters. When using high speed analog and digital circuits on the same board, proper component selection, and the printed circuit board layout considerations become predominant factors for obtaining noise free performance from such circuits.

Because A/D and D/A converters are partly analog and partly digital devices, the analog signals are subject to degradation from power supply noise, ground loops, radiated pickup and magnetic coupling. This type of mixed circuitry often contain harmonics of waveforms and hence, require special solutions to avoid excessive noise from the system.

Ground Plane

When designing circuits with high speed logic devices, it is always a good practice to use the ground plane under signal traces to minimize radiated noise and crosstalks. When using flash A/D and high speed D/A converters, better performance can be achieved by separating this ground plane into two separate areas designated as digital ground area and analog ground area. Both areas should be separated by at least 1/8" from each other. The digital ground plane should cover all areas under digital logic including signal traces leading up to the A/D and D/A converters but leaving all pins of these parts. The analog ground plane area should include all ground pins on the device. These ground plane areas should be connected at a single point on the PC board.

Power Plane

For PC boards with many high speed devices, it is better to include a power plane layer to minimize the voltage drops and improve noise margins. To improve DC performance, the power plane should be separated into two areas which lay on top of the analog and digital ground plane areas. The digital area of power plane should supply power to the digital logic and digital section of the device. The analog area of the power planes should supply power to the analog section of the device. It is very important that no portion of the digital or analog power plane overlay each other. This will prevent plane-to-plane noise coupling. Also, like ground planes, both power planes should be tied together at one single point on the PC board.

The return connections for the power and ground from the PC board to the power supply should be made to the digital power and ground areas to minimize the DC current flowing through the path connecting digital and analog sections together.

Digital Signal Lines

The digital input signals of a D/A converter and the digital output signals of an A/D converter should be kept away as much as possible from the analog signals and other reference inputs. These signals should run over the digital ground and power plane areas of the PC board. The distances between the interconnects should be as small as possible to minimize the undershoot, ringing and datafeed through noise. Also, the clock lines must not be running too long so they do not pick up noise. In some applications, termination resistors may be required at the inputs of the D/A converter to reduce noise. The termination resistors should be the carbon film type.

Analog Signal Lines

The traces carrying analog input signals to the A/D converters on the PC board should be further away from the traces carrying digital outputs from the converters. Also, the input signals should run over the analog power and ground plane areas. The coupling of high frequency digital signals into the analog lines by mutual or stray capacitance can produce errors that are more significant than having poor grounding.

The D/A converter should be located as close as possible to its output connectors to minimize the noise pickup on the analog output traces. This will also help minimize reflections due to impedance mismatch. The D/A converter reference circuitry should be kept close to the D/A converter to avoid stray pickup.

Normally, the video converter contains circuitry for rejecting the power supply noise, but the rejection decreases with the increase in frequency. For example, if a 0.01 μ F compensation capacitor is used, the power supply rejection on D/A converter flattens out to 10dB at frequencies around 1KHz. If a converter is powered from the 20KHz switching power supply where the noise level is 100mV at 20KHz, then the noise level at the output of this converter will be 10mV. The noise at the output of the D/A converter is comprised of the quantization error, power supply noise and various

noises caused by the ground loops, radiated pickup, magnetic coupling, data under shoot or ringing as stated before. This noise can be eliminated by using a low pass filter at the output of the converter. A 4.2MHz low-pass filter is shown in Figure 1.

Decoupling Capacitors

A PC board with a four layer structure where power and ground planes are inside the board and the signals are on the top and bottom of the board, will provide good high frequency decoupling because of the distributed capacitance between the power and ground planes. In addition, 0.1 μ F ceramic capacitor per every three or four devices should take care of the low frequency decoupling. A ceramic capacitor of .0.1 to .1 μ F near the power supply pin of the device can be used for bypassing the analog power and ground plane areas.

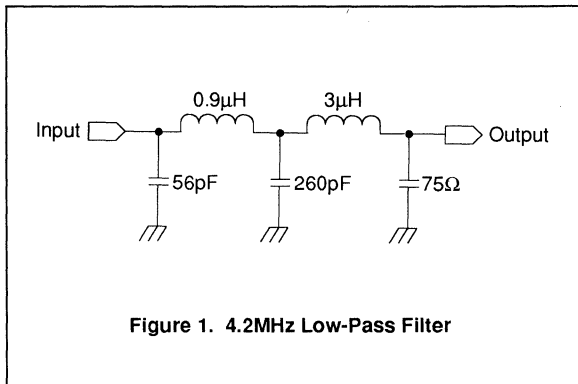


Figure 1. 4.2MHz Low-Pass Filter

Bypass Capacitors

The bypass capacitors are necessary, but when using high speed devices such as KSV3110 at a sampling rate of 10MHz, the influence of bypass capacitors on noise characteristic is most significant. For example, a

0.1 μ F capacitor with leads over 1/4" length, will behave as an oscillator at 10MHz of frequency. It may appear inductive beyond this frequency, therefore, the bypass capacitors used on a PC board must have the shortest possible leads. The ceramic chip capacitors are very good by bypassing, but they may not survive a wide temperature range. Another choice is a radial lead ceramic capacitor.

However, any bypass capacitor selected must be used in conjunction with ground and power planes described previously.

There is no single method of bypassing that is suitable for all possible applications. However, the effectiveness of the decoupling will be determined by the bypass capacitor along with the distributed inductance of the power supply plane.

FLASH CONVERTERS

KSV3110 High-Speed A/D-D/A Converter
KSV3208 High-Speed A/D Converter

Application Note

FLASH CONVERTERS

GENERAL DESCRIPTION

Digitizing analog signals containing high frequency components with accuracy requires ultrahigh speed A/D converters. Such converter is essential in RADAR data transmission, high speed digital data transmission, image processing and digital television. In TV for example, high speed conversion will enhance images, correct time base errors, synchronize and store frames, and reduce noise. Analog-to-digital and digital-to-analog converters also play an important role in the field of microcomputers when they are used in control and measurement applications.

All these applications require much faster data conversion technique and one such technique is called flash conversion (or parallel conversion) technique.

The flash converter offers very high performance and has an ability to perform data conversions (from analog to digital or vice versa) at extremely high speed. The crucial parts in this type of converters are comparators. They not only determine the speed of the converter but also the accuracy. Also, the switches must be very fast and be able to withstand the reference voltage. Generally, the number of comparators in an n -bit converter will be $2^n - 1$. In flash conversion, the analog input is compared against 2^n graded voltage levels, using the same number of comparators (shown in figure 1). The comparator output logic levels are processed by a priority encoder, which converts the output to a binary code. The whole conversion occurs simultaneously, so it is the fastest means of conversion, however, it requires a large number of comparators having very high accuracy and a large number of gates.

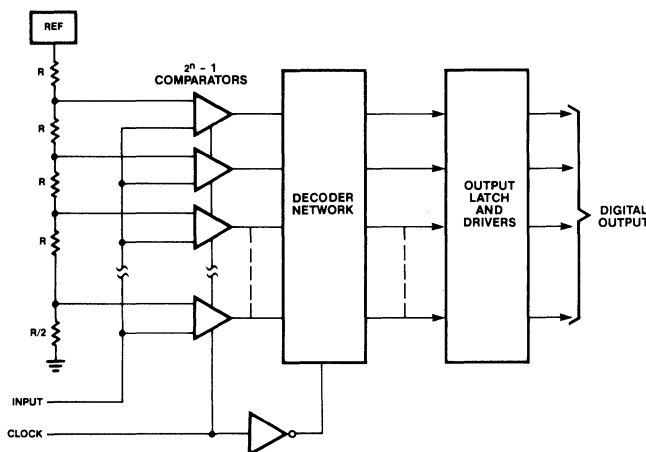


Figure 1. Flash (Parallel) A/D Converter

FLASH CONVERTERS

Like other converters, parallel type of A/D converter also contains a quantizer circuit followed by a decoder circuit, but the difference is that both functions are separate in this type of converter. The quantizer in such A/D converters is defined by its parallel function. Figure 2 shows the transfer function for a 4-bit parallel type of converter. The output in this figure is divided into 16 different states or 2^n levels, where n is the number of bits. There are $2^n - 1$ analog transition points along the horizontal axis representing voltage levels that define the edges between adjacent output stages or codes. These are also called analog decision points. These decision points are set precisely in a quantizer in order to divide the analog voltage range into the correct quantized values.

The quantizer in this case assigns one output code to a small range or band of analog input values. The size of such band is a quantum Q which is given by:

$$Q = \frac{\text{FSR}}{2^n} \quad \text{where FSR = Full Scale Analog Range} \\ n = \text{number of bits}$$

In figure x, the full-scale-range is 2.0 volts, therefore;

$$Q = \frac{2.0}{2^4} = \frac{2.0}{16} = 0.125 \text{ mV}$$

The voltages 0.125, 0.25, 0.375, 0.5, 0.625, 0.75, and 0.825, are the center points of each output code generated by the A/D converter (shown in figure 2).

The transfer function shown in figure 2, is of an ideal quantizer of an A/D converter, however, in practice, the A/D converter will have errors like offset or linearity for example. (see App. Note on "Glossary of Data Conversion").

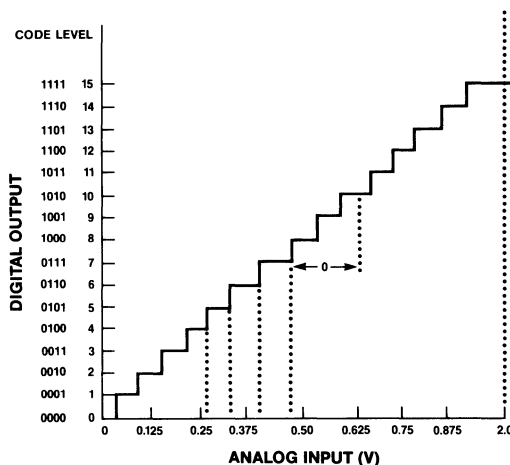


Figure 2. The Quantizer Transfer Function for a 4-Bit Parallel A/D Converter

FLASH CONVERTERS

KSV3110 Flash A/D and D/A Converter on a Single Chip

The KSV3110 is a VLSI circuit designed using Samsung's CI (Collector Implanted) technology. It consists of a high-speed flash-type 8-bit A/D converter and a high-speed 10-bit low glitch D/A converter. Also, various auxiliary circuits like, reference voltage generator, pre-amplifier, and input clamping circuit are integrated on the same chip (Figure 3).

The KSV3110 has been developed for all applications involving high-speed data conversion. The KSV3110 is very useful for industrial applications in conjunction with image processing. It is also used for decoding Television signals in Pay-TV converters or MAC converters used for direct satellite broadcasting.

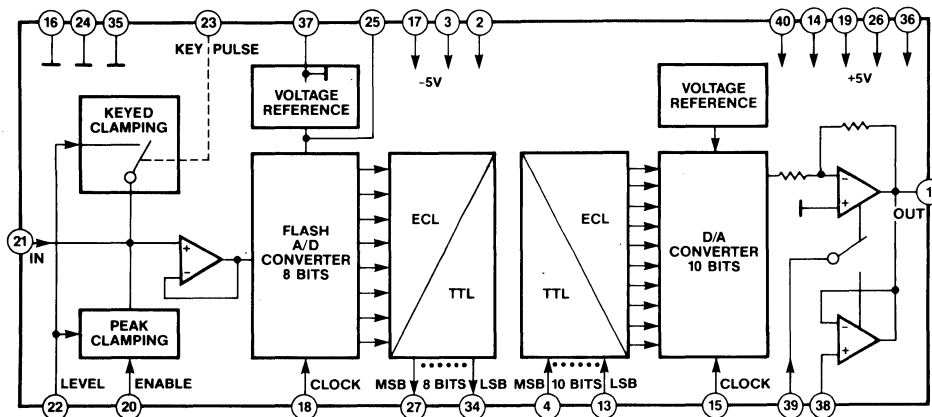


Figure 3. KSV3110 Block Diagram

The on-chip A/D converter has an accuracy of 8-bits, but the on-chip D/A converter is available with an accuracy of either 7, 8, 9 or 10-bits. The KSV3110 comes in a 40-pin DIP plastic package.

In many applications, only A/D converter is required. The KSV3208 from Samsung contains a flash A/D converter for those who do not require D/A converter in their systems. Essentially, the KSV3208 contains the A/D converter section of the KSV3110.

FLASH CONVERTERS

KSV3208 Flash A/D Converter

The KSV3208, is a VLSI circuit similar to the KSV3110, designed using the same CI (Collector Implanted) technology. Like KSV3110, the KSV3208 also contains various auxiliary circuits such as; reference voltage generator, pre-amplifier, and input clamping circuit (Figure 4).

The KSV3208 has been developed for use in all applications requiring high-speed A/D converter. The applications involve low-cost video digitizing, Radar data conversion, data acquisition and medical imaging. Other promising applications are in the field of industrial electronics, in conjunction with image processing.

The reference voltage for A/D converter of the KSV3110 and KSV3208 is generated internally, but this voltage with the ground for the reference voltage circuitry are connected to the pins so that an external filter capacitor can be used. All inputs and outputs of these devices are TTL compatible.

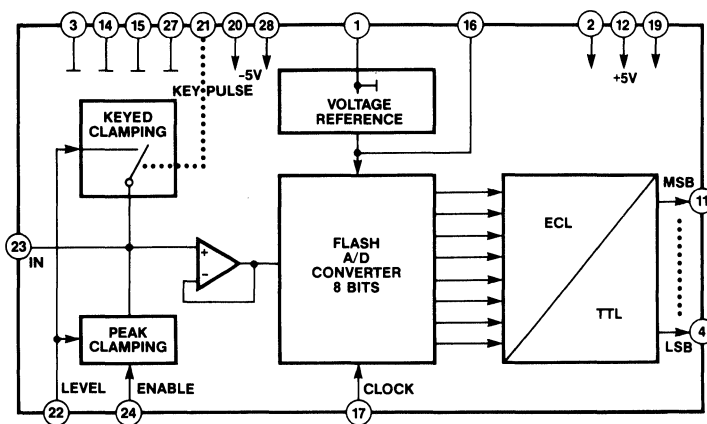


Figure 4. KSV3208 Block Diagram

FUNCTIONAL DESCRIPTION

A/D Converter

The A/D converter on the KSV3110 and KSV3208 contains the following basic functions:

- Analog section
- Digital section
- Data output section and
- Auxiliary section

Analog Section

The analog section consists of the comparator array, reference resistor string and voltage reference. The input voltage to the A/D is compared with 2^n separate reference voltage points by a voltage equivalent to one LSB where n is the number of data outputs, or the resolution of A/D converter in bits.

The comparator reference voltage points are tapped from the reference resistor string which is driven by a voltage reference circuit.

FLASH CONVERTERS

Digital Section

In this section, the output from the 2^n comparators is encoded into an n-bit binary word for high speed operation. The emitter coupled logic (ECL) is used for encoding. The encoded n-bit data is latched in the output data latches.

Data Output Section

This section consists of output data latch, and logic level converter (e.g. ECL-to-TTL). The output latches of the converter hold data valid while the conversion is taking place. These latches are updated by the sampling clock signal.

The latched outputs of the ECL logic are converted into TTL level by the ECL-to-TTL logic converter circuit, so the outputs can easily interface with the external TTL devices.

Auxiliary Section

The auxiliary section contains the voltage reference circuit, pre-amplifier as buffer, and clamping circuit for peak or keyed clamping. All these functions will help reduce the size of the external components thereby reducing the overall system costs. Also, they will provide more stable features because of the identical characteristics.

Reference Voltage Generator

The reference voltage generator will operate from 2.0 Volts supply. The reference voltage generator is designed using the bandgap reference circuit, that will provide higher accuracy for the temperature coefficient characteristic.

Pre-amplifier

The input impedance of the A/D converter is 10 MOhms at the input frequency of 1 KHz and 100 KOhms at the input frequency of 10 MHz. In many instances, for using an A/D converter in a system, it becomes necessary to match the impedance of an external circuitry to the input impedance of the converter. The on-chip pre-amplifier on the KSV3110 and KSV3208 will take care of the impedance matching requirement. This pre-amplifier is used as a voltage follower (unity gain amplifier) so that it will not affect the gain of an input signal.

Clamping Circuit

The purpose of this clamping circuit is to provide an appropriate signal levels for the input of the A/D converter (see figure 5). The two basic methods for using this section are:

1. Peak clamping and
2. Keyed clamping

Peak clamping

The amplitude of an analog signal for A/D converter should be 0V to 2 Volts. In several applications, the analog signal consists of different amplitude levels. It is necessary to shift the amplitude of such signal to match the input conditions required by the A/D converter. This signal conditioning can be achieved by the clamping circuit given in figure 6.

Keyed Clamping

This feature can be tailored by the user for clamping the analog input signal, according to the requirements. When using this method, the peak clamping function described above, must be disabled. The user can now provide key pulses to pin 23 of the KSV3110 and adjust the voltage levels of the analog input signal in correspondance with the key pulses shown in the figure 7.

If the amplitude of an analog signal is between 0V and 2 Volts, then the clamping is not required. In this case, the clamping circuit on KSV3110 should be disabled by connecting pins 22 and 23 to the ground and leaving pin 20 with no connection.

FLASH CONVERTERS

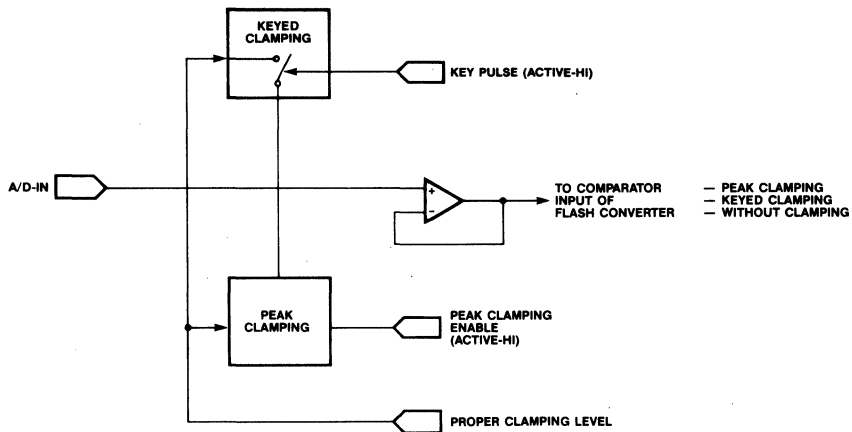
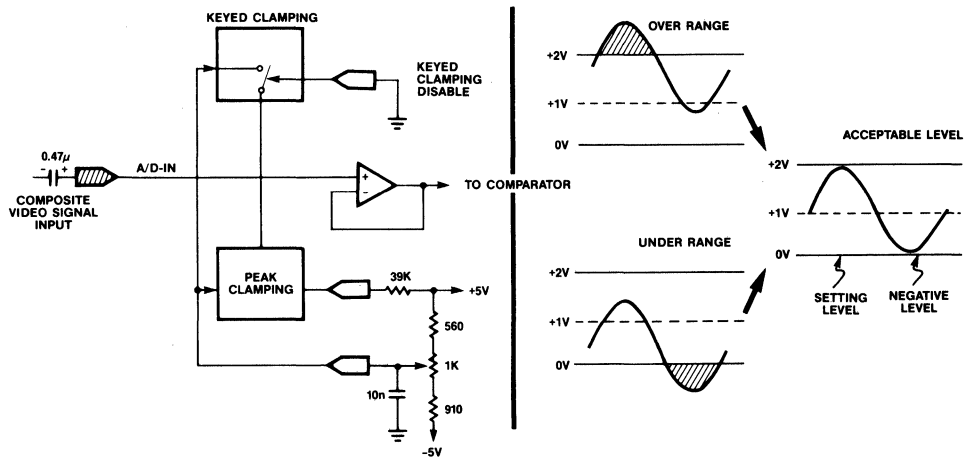


Figure 5. KSV3208, KSV3110 Clamping Circuit for A/D Input



Input signal is clamped automatically to the negative peak value

Figure 6. Operating with Peak Clamping

FLASH CONVERTERS

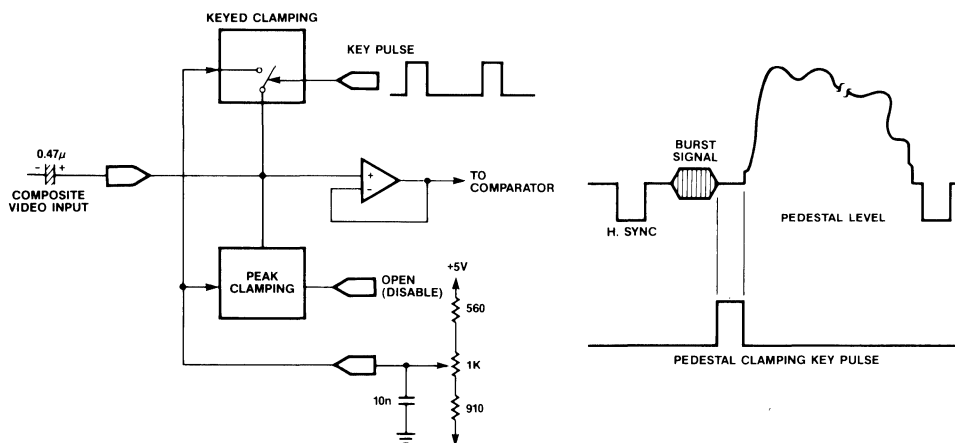


Figure 7. Operating Keyed Clamping

D/A Converter

The D/A converter on the KSV3110 contains the following major function blocks:

- Data input section
- Decoding section
- Analog output section
- Output signal switchover circuit

Data Input Section

This section includes logic level converters, and data input register. The TTL data input to this section will be converted to the ECL logic level before entering into the register, since this register operates with the ECL voltage levels in order to obtain the desired conversion speed. The primary function of the input register is to hold the data constant during conversion. The register must assure precise matching of propagation delays to keep glitches to the minimum.

Decoding Section

The decoding section can be divided in two parts: first one generates very accurate currents and the second one causes these currents to be switched according to the contents of the input register. This section is the heart of the D/A converter and is called "switching network".

Analog Output Section

Normally, the output of the switching network is in the form of current which must to be converted into voltage for interfacing with the external world. A typical value of an output impedance for the D/A converter is 15 Ohms.

The output of the D/A section of KSV3110 contains two output op-amps, one of which is used to convert the output current into the output voltage. This amplifier has very low offset voltage and offset voltage drift, high slew rate and fast settling time. Also it requires very small bias current (which should be smaller than 1 LSB current).

FLASH CONVERTERS

Output Signal Switchover Circuit

The switchover circuit is unique to this product and is not found in other compatible products. The output switch over circuit consists of two amplifiers and an analog switch as shown in figure 8. They are designed to allow an external analog signal to be multiplexed with an internally converted analog signal which is an output of the D/A converter. When using this feature, the external analog signal should be supplied to pin 38. In this case, the output at pin 1 will be either of the two signals and the selection can be made by applying proper logic level to pin 39. A low on pin 39 will select the internally converted analog signal and a high on pin 39, will select the external signal (from pin 38) as an output at pin 1.

The advantage of this feature is obvious in video applications, where, the horizontal and vertical sync pulses are combined with a video signal to obtain the stabilized composite video signal as shown in figure 9. The slew rate of the amplifier for an external signal is 5.16 Volts/microsecond, when the frequency of the external input signal is 15.7 KHz, which is the frequency of the horizontal sync pulse.

The timing diagrams for the KSV3110 and KSV3208 are illustrated in figures 10 and 11.

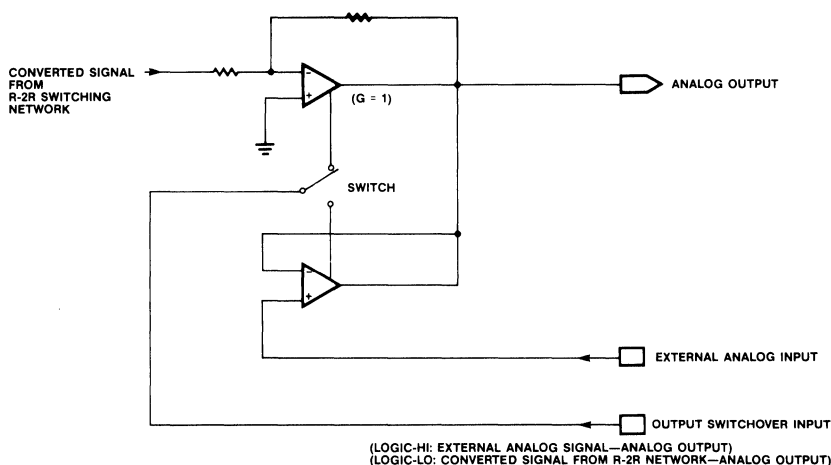
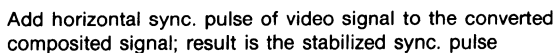


Figure 8. KSV3110-DA Output Signal Switchover Circuit

3

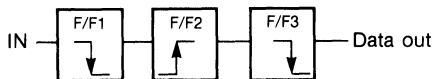


The diagram shows the timing relationship between the A/D clock, the analog input, and the digital output. The A/D clock is a periodic square wave. The analog input is a continuous signal. The digital output is a sequence of data words: DATA N-1, DATA N, and DATA N+1. The timing parameters are defined as follows:

- t_{AD} : Aperture time, the time interval during which the analog input is sampled.
- t_W : Transfer time A/D, the time interval between the end of the aperture time and the start of the digital output delay.
- t_{DV} : Digital output delay, the time interval between the start of the transfer time and the start of the digital output delay.

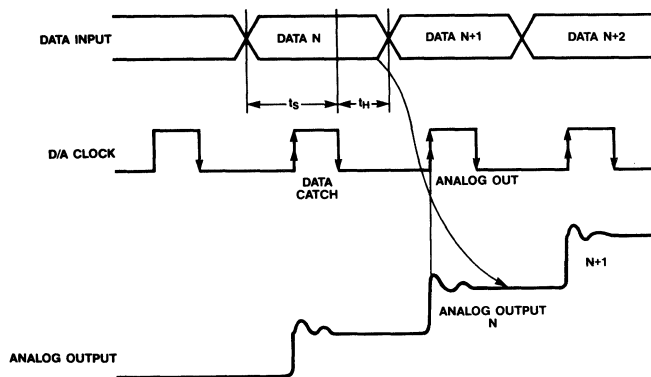
Falling edge (negative) sampling
After 1 clock, negative triggering data out

3-stage latch is used in A/D section.



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FLASH CONVERTERS



Digital data capture: Negative triggering
 Analog output; Positive triggering after 1/2 period

2-stage latch is used
 in D/A section.

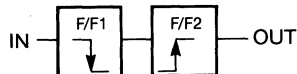
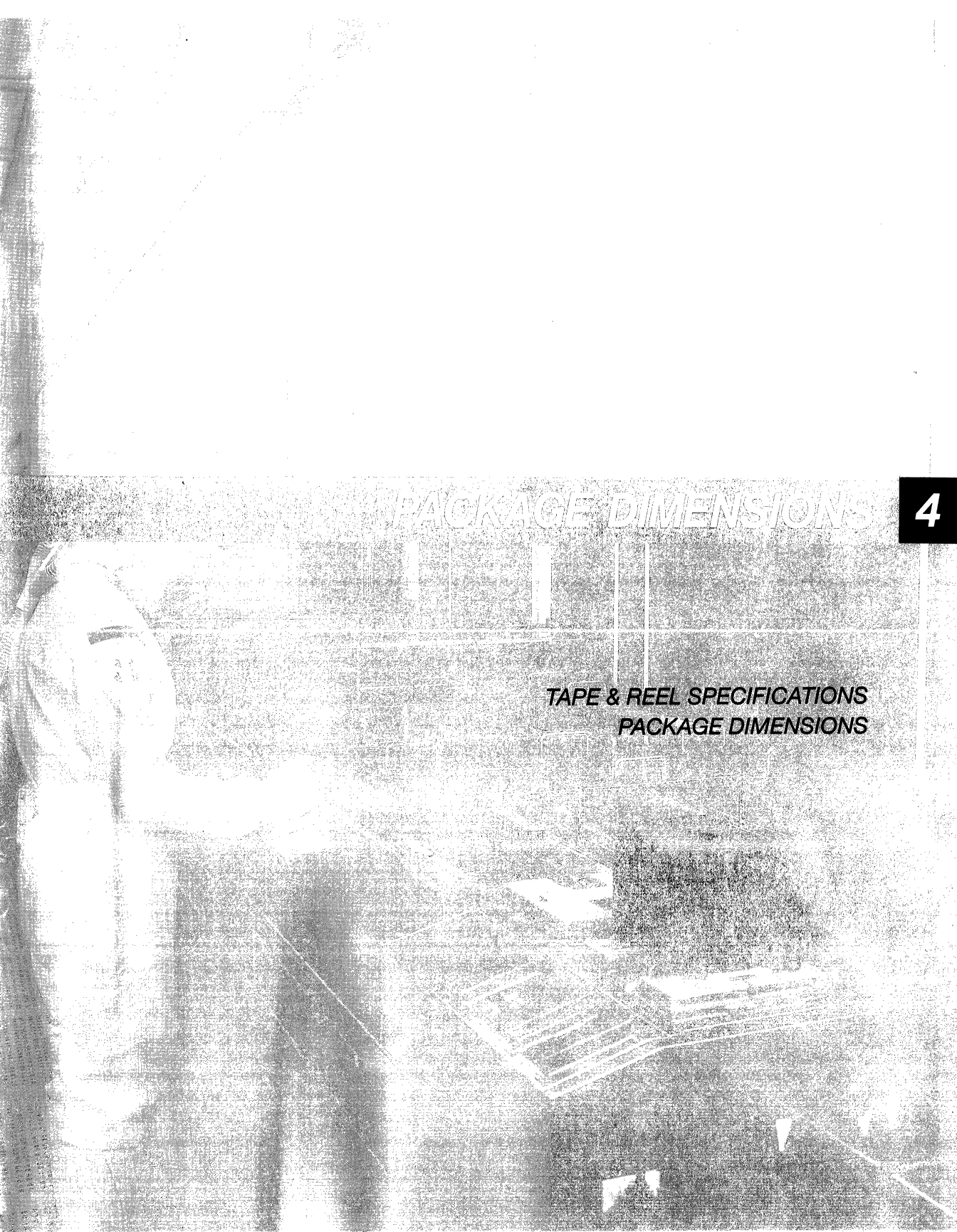


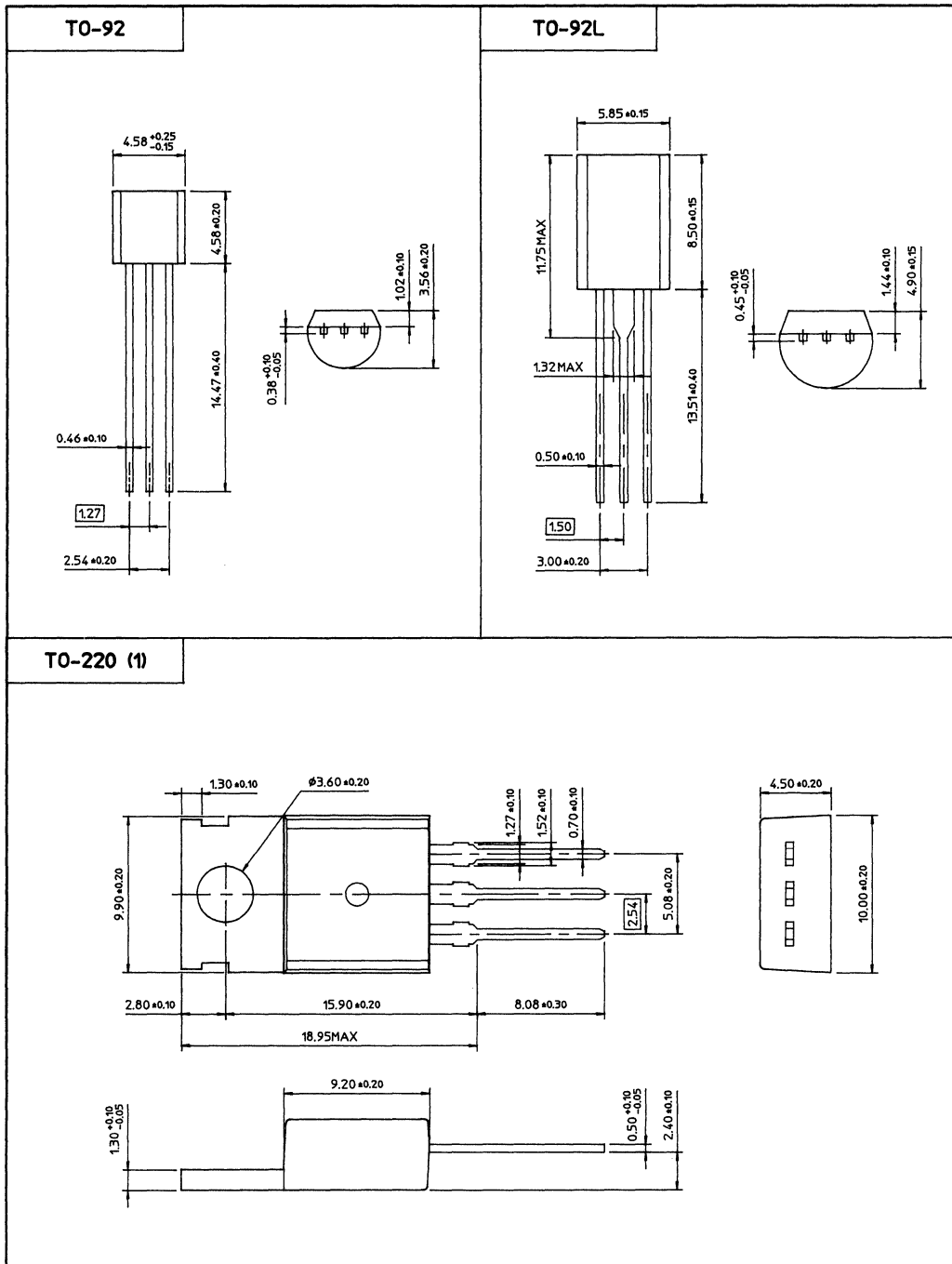
Figure 11. KSV3110 Timing Diagram (D/A)

PACKAGE DIMENSIONS

4

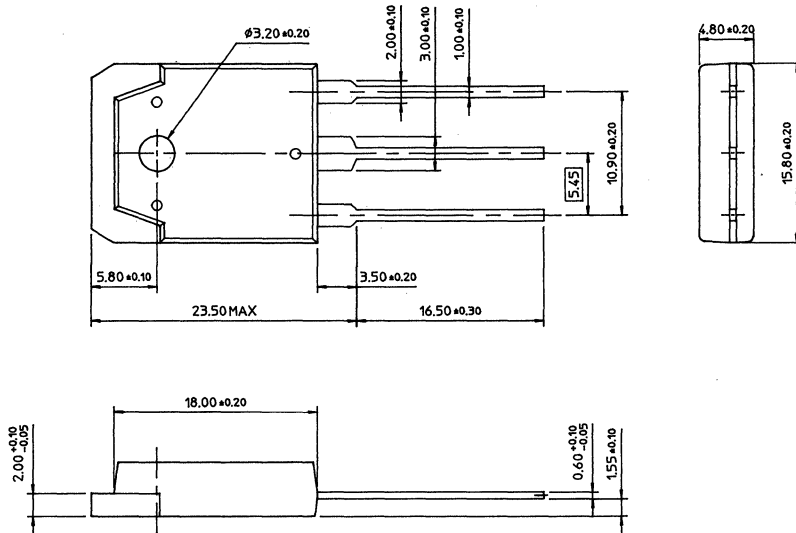
TAPE & REEL SPECIFICATIONS
PACKAGE DIMENSIONS



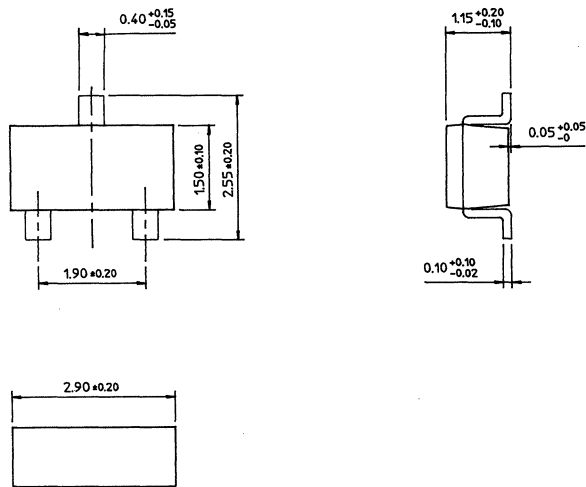


Dimensions in Millimeters

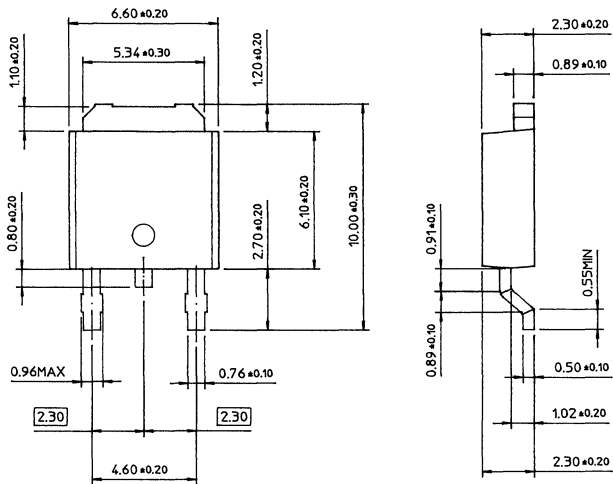
T0-3P (1)



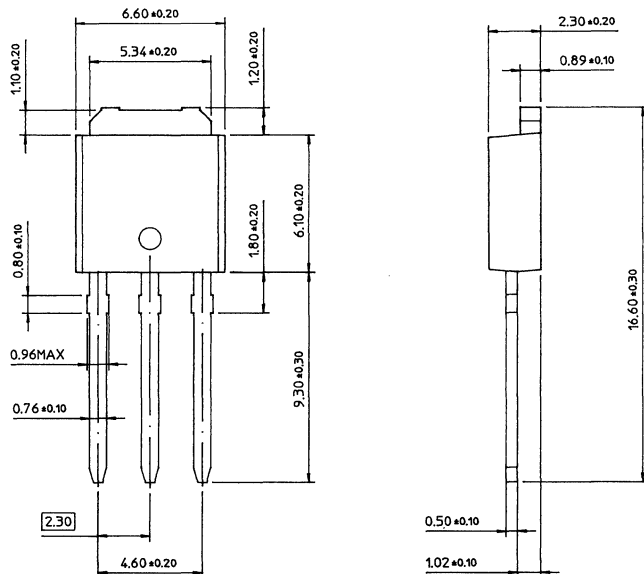
SOT-23



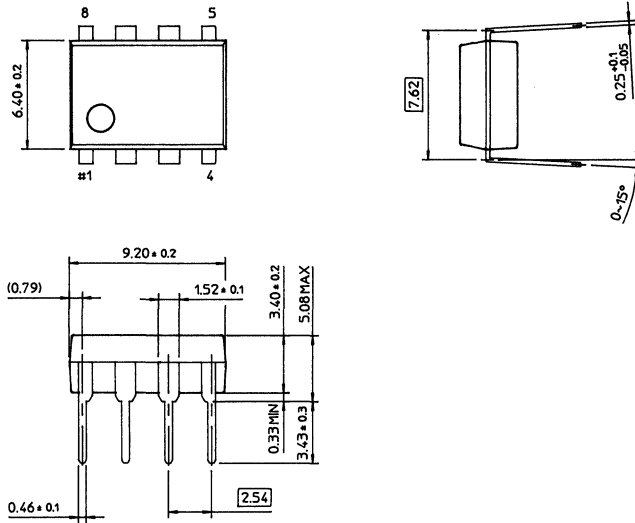
D-PAK



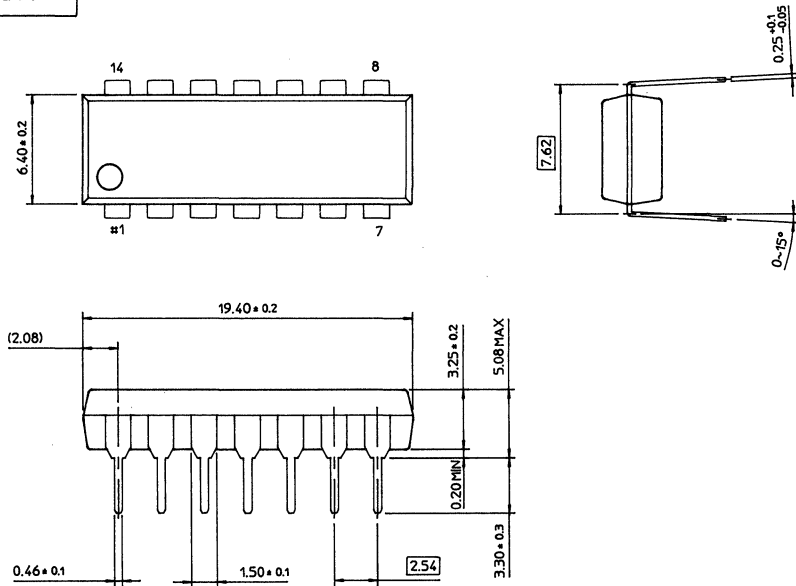
I-PAK



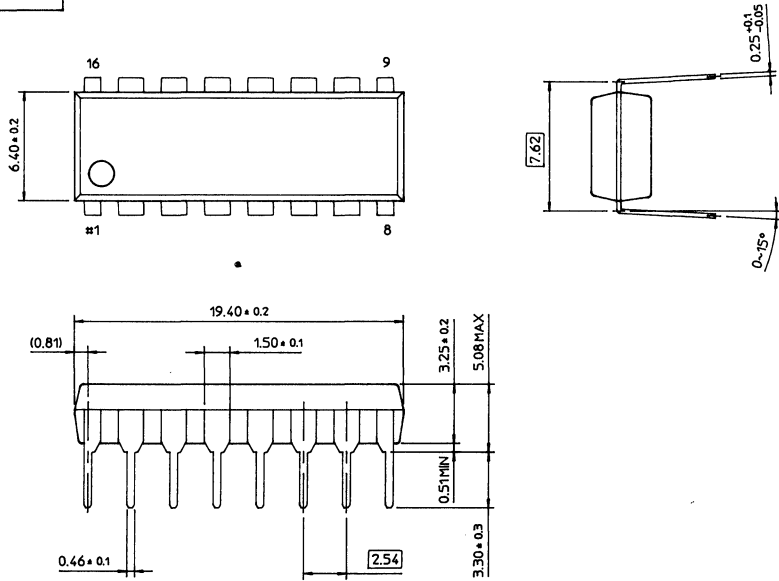
8-DIP-300



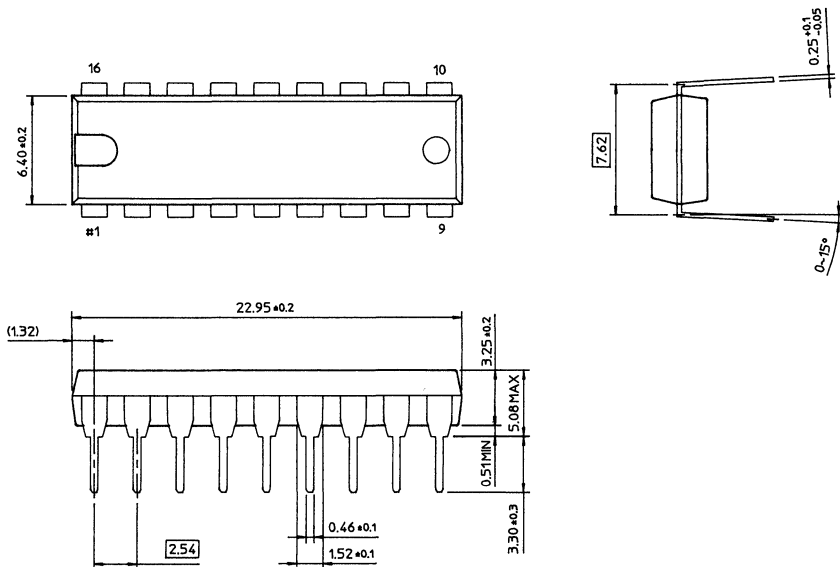
14-DIP-300



16-DIP-300A

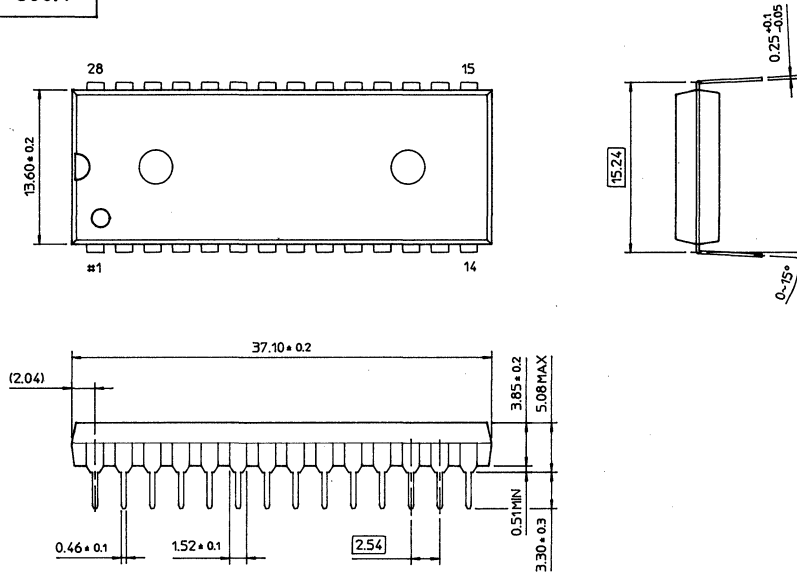


18-DIP-300A

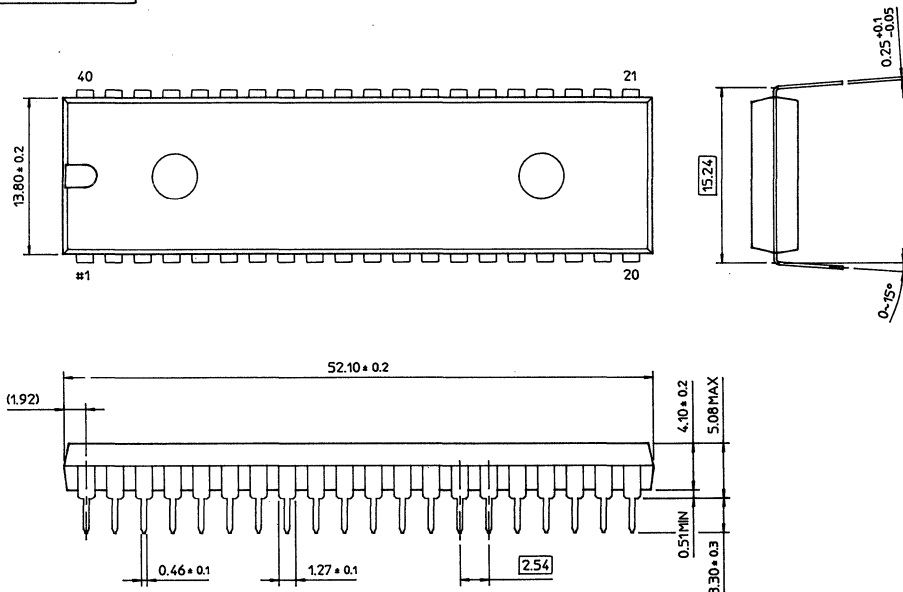


Dimensions in Millimeters

28-DIP-600A



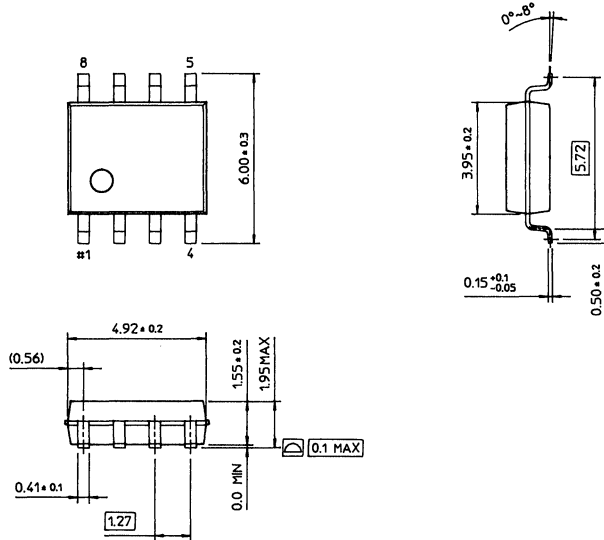
40-DIP-600A



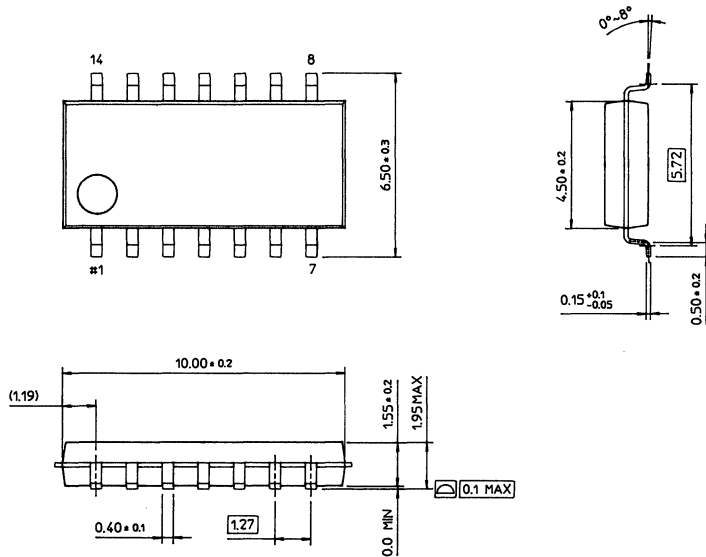
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8-SOP-225

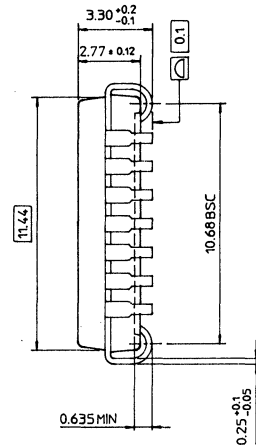
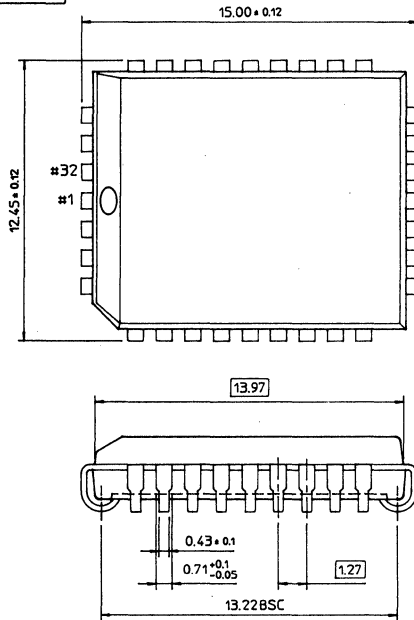


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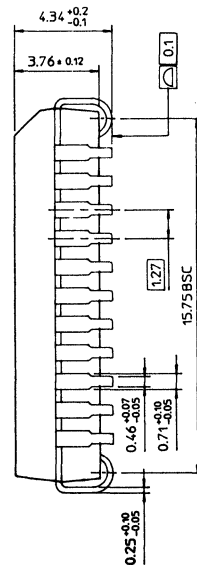
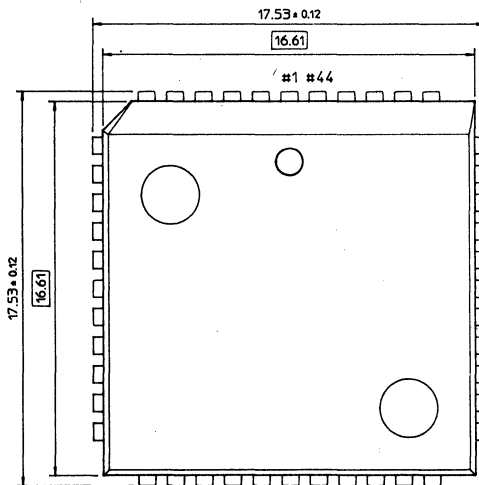


Dimensions in Millimeters

32-PLCC-REC.



44-PLCC-SQ.

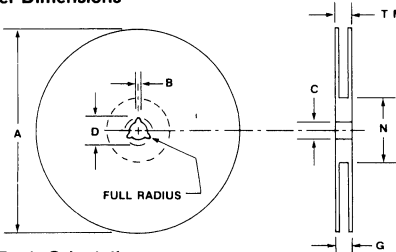


PACKAGE DIMENSIONS

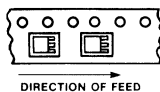
TAPE AND REEL SPECIFICATIONS

Samsung Tape & Reel specifications conform to the EIA-481 specification, Revision A.

Reel Dimensions



D-Pack Orientation



Unit: mm

Symbol	Tape Size			
	8 mm	12 mm	16 mm	24 mm
B1	4.2	8.2	12.1	20.1
D1	1.2	1.5	1.5	1.5
R (Min)	25	30	40	50
W	8.0±0.3	12.0±0.3	16.0±0.3	24.0±0.3
F	3.5±0.05	5.5±0.05	7.5±0.05	11.5±0.05
K (Max)	2.4	4.5	6.5	6.5
P ₂	2.0±0.05	2.0±0.05	2.0±0.1	2.0±0.1
P	4.0±0.1	8.0±0.1	8.0±0.1	2.0/16.0/20.0 12.0±0.1
E	1.75±0.1	1.75±0.1	1.75±0.1	1.75±0.1
P ₀	4.0±0.1	4.0±0.1	4.0±0.1	4.0±0.1
t (Max)	0.4	0.4	0.4	0.4
D	1.5±0.1	1.5±0.1	1.5±0.1	1.5±0.1

Note 1: A0 B0 K0 are determined by component size. The clearance between the component and the cavity must be within 0.05 min. to 0.90 max. for 16mm tape and 0.05 min. to 1.00 max. for 24mm tape. The component cannot rotate more than 20°C within the determined cavity.

Note 2: Tape and components shall pass around radius "R" without damage.

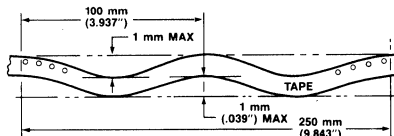
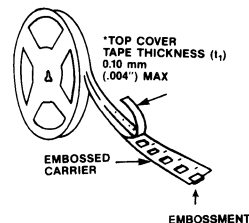
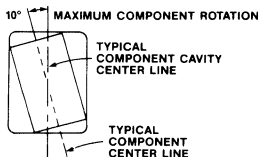
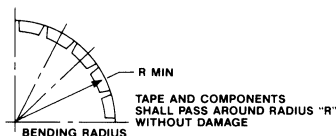
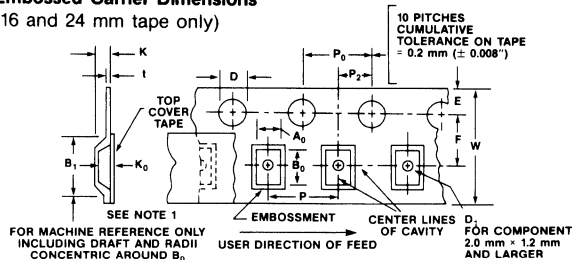
Note 3: For D-Pack: A₀ = 10.8 ± 0.1
B₀ = 7.5 ± 0.1
P = 12.0 ± 0.1

Unit: mm

Tape Size	A Max	B Min	C	D Min	N Min	G	T Max
8mm	330	1.5	13.0±0.2	20.2	50	8.2±0.1	15.0
12mm	330	1.5	13.0±0.2	20.2	50	12.4±0.2	22.0
16mm	360	1.5	13.0±0.2	20.2	50	16.4±0.2	26.0
24mm	360	1.5	13.0±0.2	20.2	50	24.4±0.2	34.0

Embossed Carrier Dimensions

(16 and 24 mm tape only)



CAMBER (TOP VIEW)
ALLOWABLE CAMBER TO BE 1 mm 100 mm NONACCUMULATIVE OVER 250 mm

Pin Count	Tape Width (mm)	Quantity/Reel
SO-8	12	3000
SO-14	16	3000
SO-16	16	3000
SO-20	24	1000
SO-24	24	1000
SO-28	24	1000
D-PACK	16	2000

This image shows a blank page with some very faint, sparse horizontal lines and minor dark specks, likely due to scanning noise or dust on the original paper. There is no legible text or structured data present.



SALES OFFICES and MANUFACTURER'S REPRESENTATIVES

5

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Fax: (408) 954-7883

North Central

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Suite 210
Itasca, IL 60143-2636
Tel: (708) 775-1050
Fax: (708) 775-1058

North East

20 Mall Road
Suite 410
Burlington, MA 01803
Tel: (617) 273-4888
Fax: (617) 273-9363

Southwest

16253 Laguna Canyon Road
Suite 100
Irvine, CA 92718
Tel: (714) 753-7530
Fax: (714) 753-7544

South Central

15851 Dallas Parkway
Suite 840
Dallas, TX 75248-3307
Tel: (214) 770-7970
Fax: (214) 770-7971

Southeast

802 Greenvally Road
Suite 204
Greensboro, NC 27408
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Aurora, CO 80011

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 Miami, FL 33014-9317

ALL AMERICAN (800) 327-6237
 5009 Hiatus Road FAX: (305) 749-9229
 Sunrise, FL 33351

JACO (407) 241-7943
 1060 Holland Drive FAX: (407) 241-7950
 Suite 3K

Boca Raton, FL 33487
RM ELECTRONICS (407) 767-8005
 581 East St. Rte. 434 FAX: (407) 767-8165
 Longwood, FL 32750

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 2200 N. Stronington Ave., FAX: (708) 843-2320
 Suite 210

Hoffman Estates, IL 60195
QPS (708) 884-6620
 101 E. Commerce Dr. FAX: (708) 884-7573
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 1415 Magnavox Way FAX: (219) 436-1977
 Suite 130
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 Marion, IA 52302 FAX: (319) 377-1539

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 Lenexa, KS 66215 FAX: (913) 888-4848

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 4012 Dupont Circle FAX: (502) 893-2435
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 9357 General Drive FAX: (313) 459-0232
 Suite 116
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 Suite 315
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 Suite 131 FAX: (314) 298-8660
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 Cicero, NY 13039

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 7353 Victor-Pittsford Road FAX: (716) 924-4946
 Victor, NY 14564

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 2978 Findley Avenue FAX: (614) 262-0384
 Columbus, OH 43202

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 Brunswick, OH 44212

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 Plymouth Meeting, PA 19462

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 Calle Cruz #2 FAX: (809) 892-3366
 Bajos, San German
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 555 Republic Drive FAX: (214) 423-8556
 Suite 105
 Plano, TX 75074

VIELOCK ASSOCIATES TEL: (512) 345-8498
 9430 Research Blvd. FAX: (512) 346-4037
 Echelon Bldg. 2, Suite 330
 Austin, TX 78759

VIELOCK ASSOCIATES TEL: (713) 974-3287
 10700 Richmond Avenue FAX: (713) 974-3289
 Suite 108
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 Suite 280 FAX: (801) 288-2505
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 Redmond, WA 98052

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DAVIX INTERNATIONAL LTD. TEL: (414) 255-1600
 N91 W17194 Appleton Avenue FAX: (414) 255-1863
 Menomonee Falls, WI 53051

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